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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4078fbd100e

- Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
- Three SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
- Three enhanced I^2C-bus interfaces, one with a true open-drain output supporting the full I^2C-bus specification and Fast-mode Plus with data rates of 1 Mbit/s, two with standard port pins. Enhancements include multiple address recognition and monitor mode.
- I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- CAN controller with two channels.

- Digital peripherals:
  - SD/MMC memory card interface.
  - Up to 165 General Purpose I/O (GPIO) pins depending on the packaging, with configurable pull-up/down resistors, open-drain mode, and repeater mode. All GPIOs are located on an AHB bus for fast access and support Cortex-M4 bit-banding. GPIOs can be accessed by the General Purpose DMA Controller. Any pin of ports 0 and 2 can be used to generate an interrupt.
  - Two external interrupt inputs configurable as edge/level sensitive. All pins on port 0 and port 2 can be used as edge sensitive interrupt sources.
  - Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input. Specific timer events can be selected to generate DMA requests.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - Two standard PWM/timer blocks with external count input option.
  - One motor control PWM with support for three-phase motor control.
  - Real-Time Clock (RTC) with a separate power domain. The RTC is clocked by a dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers, allowing system status to be stored when the rest of the chip is powered off. Battery power can be supplied from a standard 3 V lithium button cell. The RTC will continue working when the battery voltage drops to as low as 2.1 V. An RTC interrupt can wake up the CPU from any reduced power mode.
  - Event Recorder that can capture the clock value when an event occurs on any of three inputs. The event identification and the time it occurred are stored in registers. The Event Recorder is located in the RTC power domain and can therefore operate as long as there is RTC power.
  - Windowed Watchdog Timer (WWDT). Windowed operation, dedicated internal oscillator, watchdog warning interrupt, and safety features.
  - CRC Engine block can calculate a CRC on supplied data using one of three standard polynomials. The CRC engine can be used in conjunction with the DMA controller to generate a CRC without CPU involvement in the data transfer.
- Analog peripherals:
  - 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 400 kHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.

Table 2. Ordering options *…continued*

Type number	Flash (kB)	SRAM (kB)	EEPROM (B)	EMC bus width (bit)	LCD	Ethernet	USB	CAN	UART	QEI	SD/MMC	Comparator	FPU	Package
LPC4078FBD144	512	96	4032	8	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4078FBD100	512	96	4032	-	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP100
LPC4078FBD80	512	96	4032	-	no	yes	H/O/D	2	5	yes	no	yes	yes	LQFP80
LPC4076														
LPC4076FET180	256	80	2048	16	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180
LPC4076FBD144	256	80	2048	8	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4074														
LPC4074FBD144	128	40	2048	-	no	no	D	2	4	no	no	no	no	LQFP144
LPC4074FBD80	128	40	2048	-	no	no	D	2	4	no	no	no	no	LQFP80
LPC4072														
LPC4072FET80	64	24	2048	-	no	no	D	2	4	no	no	no	no	TFBGA80
LPC4072FBD80	64	24	2048	-	no	no	D	2	4	no	no	no	no	LQFP80

6. Pinning information

6.1 Pinning

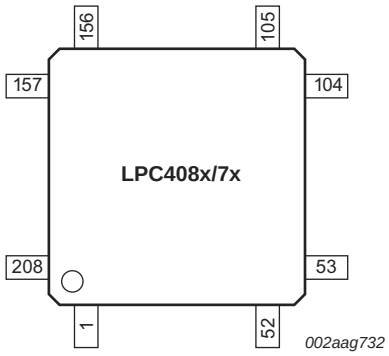

Fig 2. Pin configuration (LQFP208)

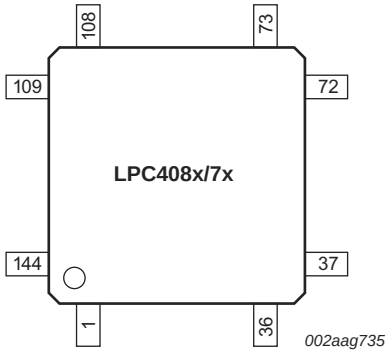

Fig 3. Pin configuration (LQFP144)

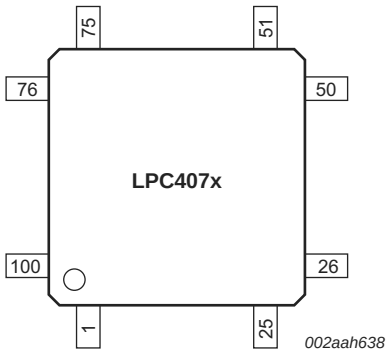

Fig 4. Pin configuration (LQFP100)

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[7]	136	G16	G11	95	66	51	D9	[3]	I; PU	I/O	**P2[7] —** General purpose digital input/output pin.
										I	**CAN_RD2 —** CAN2 receiver input.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**$\overline{\text{SPIFI\_CS}}$ —** Chip select output for SPIFI.
										O	**LCD_VD[1] —** LCD data.
										O	**LCD_VD[5] —** LCD data.
P2[8]	134	H15	G14	93	65	50	E9	[3]	I; PU	I/O	**P2[8] —** General purpose digital input/output pin.
										O	**CAN_TD2 —** CAN2 transmitter output.
										O	**U2_TXD —** Transmitter output for UART2.
										I	**U1_CTS —** Clear to Send input for UART1.
										O	**ENET_MDC —** Ethernet MIIM clock.
										-	**R —** Function reserved.
										O	**LCD_VD[2] —** LCD data.
										O	**LCD_VD[6] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[15]	99	P13	-	-	-	-	-	[3]	I; PU	I/O	**P2[15] —** General purpose digital input/output pin.
										O	**EMC_CS3 —** LOW active Chip Select 3 signal.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
P2[16]	87	R11	P9	-	-	-	-	[3]	I; PU	I/O	**P2[16] —** General purpose digital input/output pin.
										O	**EMC_CAS —** LOW active SDRAM Column Address Strobe.
P2[17]	95	R13	P11	-	-	-	-	[3]	I; PU	I/O	**P2[17] —** General purpose digital input/output pin.
										O	**EMC_RAS —** LOW active SDRAM Row Address Strobe.
P2[18]	59	U3	P3	-	-	-	-	[6]	I; PU	I/O	**P2[18] —** General purpose digital input/output pin.
										O	**EMC_CLK[0] —** SDRAM clock 0.
P2[19]	67	R7	N5	-	-	-	-	[6]	I; PU	I/O	**P2[19] —** General purpose digital input/output pin.
										O	**EMC_CLK[1] —** SDRAM clock 1.
P2[20]	73	T8	P6	-	-	-	-	[3]	I; PU	I/O	**P2[20] —** General purpose digital input/output pin.
										O	**EMC_DYCS0 —** SDRAM chip select 0.
P2[21]	81	U11	N8	-	-	-	-	[3]	I; PU	I/O	**P2[21] —** General purpose digital input/output pin.
										O	**EMC_DYCS1 —** SDRAM chip select 1.
P2[22]	85	U12	-	-	-	-	-	[3]	I; PU	I/O	**P2[22] —** General purpose digital input/output pin.
										O	**EMC_DYCS2 —** SDRAM chip select 2.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P2[23]	64	U5	-	-	-	-	-	[3]	I; PU	I/O	**P2[23] —** General purpose digital input/output pin.
										O	**EMC_DYCS3 —** SDRAM chip select 3.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P3[9]	199	C5	A4	-	-	-	-	[3]	I; PU	I/O	**P3[9] —** General purpose digital input/output pin.
										I/O	**EMC_D[9] —** External memory data line 9.
P3[10]	205	B2	B3	-	-	-	-	[3]	I; PU	I/O	**P3[10] —** General purpose digital input/output pin.
										I/O	**EMC_D[10] —** External memory data line 10.
P3[11]	208	D5	B2	-	-	-	-	[3]	I; PU	I/O	**P3[11] —** General purpose digital input/output pin.
										I/O	**EMC_D[11] —** External memory data line 11.
P3[12]	1	D4	A1	-	-	-	-	[3]	I; PU	I/O	**P3[12] —** General purpose digital input/output pin.
										I/O	**EMC_D[12] —** External memory data line 12.
P3[13]	7	C1	C1	-	-	-	-	[3]	I; PU	I/O	**P3[13] —** General purpose digital input/output pin.
										I/O	**EMC_D[13] —** External memory data line 13.
P3[14]	21	H2	F1	-	-	-	-	[3]	I; PU	I/O	**P3[14] —** General purpose digital input/output pin.
										I/O	**EMC_D[14] —** External memory data line 14.
P3[15]	28	M1	G4	-	-	-	-	[3]	I; PU	I/O	**P3[15] —** General purpose digital input/output pin.
										I/O	**EMC_D[15] —** External memory data line 15.
P3[16]	137	F17	-	-	-	-	-	[3]	I; PU	I/O	**P3[16] —** General purpose digital input/output pin.
										I/O	**EMC_D[16] —** External memory data line 16.
										O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
										O	**U1_TXD —** Transmitter output for UART1.
P3[17]	143	F15	-	-	-	-	-	[3]	I; PU	I/O	**P3[17] —** General purpose digital input/output pin.
										I/O	**EMC_D[17] —** External memory data line 17.
										O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
										I	**U1_RXD —** Receiver input for UART1.
P3[18]	151	C15	-	-	-	-	-	[3]	I; PU	I/O	**P3[18] —** General purpose digital input/output pin.
										I/O	**EMC_D[18] —** External memory data line 18.
										O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
										I	**U1_CTS —** Clear to Send input for UART1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P3[25]	56	U2	M3	39	27	-	-	[3]	I; PU	I/O	**P3[25] —** General purpose digital input/output pin.
										I/O	**EMC_D[25] —** External memory data line 25.
										O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
										O	**T0_MAT0 —** Match output for Timer 0, channel 0.
P3[26]	55	T3	K7	38	26	-	-	[3]	I; PU	I/O	**P3[26] —** General purpose digital input/output pin.
										I/O	**EMC_D[26] —** External memory data line 26.
										O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
										O	**T0_MAT1 —** Match output for Timer 0, channel 1.
										I	**STCLK —** System tick timer clock input. The maximum STCLK frequency is 1/4 of the ARM processor clock frequency CCLK.
P3[27]	203	A1	-	-	-	-	-	[3]	I; PU	I/O	**P3[27] —** General purpose digital input/output pin.
										I/O	**EMC_D[27] —** External memory data line 27.
										O	**PWM1[4] —** Pulse Width Modulator 1, output 4.
										I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
P3[28]	5	D2	-	-	-	-	-	[3]	I; PU	I/O	**P3[28] —** General purpose digital input/output pin.
										I/O	**EMC_D[28] —** External memory data line 28.
										O	**PWM1[5] —** Pulse Width Modulator 1, output 5.
										I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
P3[29]	11	F3	-	-	-	-	-	[3]	I; PU	I/O	**P3[29] —** General purpose digital input/output pin.
										I/O	**EMC_D[29] —** External memory data line 29.
										O	**PWM1[6] —** Pulse Width Modulator 1, output 6.
										O	**T1_MAT0 —** Match output for Timer 1, channel 0.

7.10 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupts being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

7.11 External Memory Controller (EMC)

Remark: The EMC is available for parts LPC4088/78/76. Supported memory size and type and EMC bus width vary for different packages (see Table 2). The EMC pin configuration for each part is shown in Table 5.

Table 5. External memory controller pin configuration

Parts	Data bus pins	Address bus pins	Control pins	
			SRAM	**SDRAM**
LPC4088FBD208 LPC4088FET208 LPC4078FBD208 LPC4078FET208	EMC_D[31:0]	EMC_A[25:0]	$\overline{\text{EMC\_BLS}}$[3:0], $\overline{\text{EMC\_CS}}$[3:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC4088FET180 LPC4078FET180 LPC4076FET180	EMC_D[15:0]	EMC_A[19:0]	$\overline{\text{EMC\_BLS}}$[1:0], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC4088FBD144 LPC4078FBD144 LPC4076FBD144	EMC_D[7:0]	EMC_A[15:0]	$\overline{\text{EMC\_BLS}}$[3:2], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	not available

The LPC408x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

7.16.3 USB OTG controller

USB OTG is a supplement to the *USB 2.0 Specification* that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I^2C interface to implement OTG dual-role device functionality. The dedicated I^2C interface controls an external OTG transceiver.

7.16.3.1 Features

- Fully compliant with On-The-Go supplement to the *USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

7.17 SD/MMC card interface

Remark: The SD/MMC card interface is available on parts LPC4088/78/76.

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

7.17.1 Features

- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.
- Conforms to *Multimedia Card Specification v2.11*.
- Conforms to *Secure Digital Memory Card Physical Layer Specification, v0.96.*
- Can be used as a multimedia card bus or a secure digital memory card bus host. The SD/MMC can be connected to several multimedia cards or a single secure digital memory card.
- DMA supported through the GPDMA controller.

7.18 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC408x/7x use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.

The I^2S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I^2S connection has one master, which is always the master, and one slave. The I^2S interface on the LPC408x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.26.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I^2S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S input and I^2S output.

7.27 CAN controller and acceptance filters

The LPC408x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.27.1 Features

- Dual-channel CAN controller and bus.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.

11. Dynamic characteristics

11.1 Flash memory

Table 13. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 14. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			200	375	400	kHz
N_{endu}	endurance			100000	500000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	64 bytes	[1]	-	1.8	-	ms
t_{prog}	programming time	64 bytes	[1]	-	1.1	-	ms

[1] EEPROM clock frequency = 375 kHz. Programming/erase times increase with decreasing EEPROM clock frequency.

11.2 External memory interface

Table 15. Dynamic characteristics: Static external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		3.3	4.3	6.1	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[3]	2.4 + $T_{cy(clk)}$ × WAITOEN	3.1 + $T_{cy(clk)}$ × WAITOEN	4.2 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[3]	2.7	3.5	4.9	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.2	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 3.8	ns

[2] Parameters specified for 40 % of $V_{DD(3V3)}$ for rising edges and 60 % of $V_{DD(3V3)}$ for falling edges.

[3] $T_{cy(clk)}$ = 1/EMC_CLK (see *LPC408x/7x User manual*).

[4] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[5] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[6] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

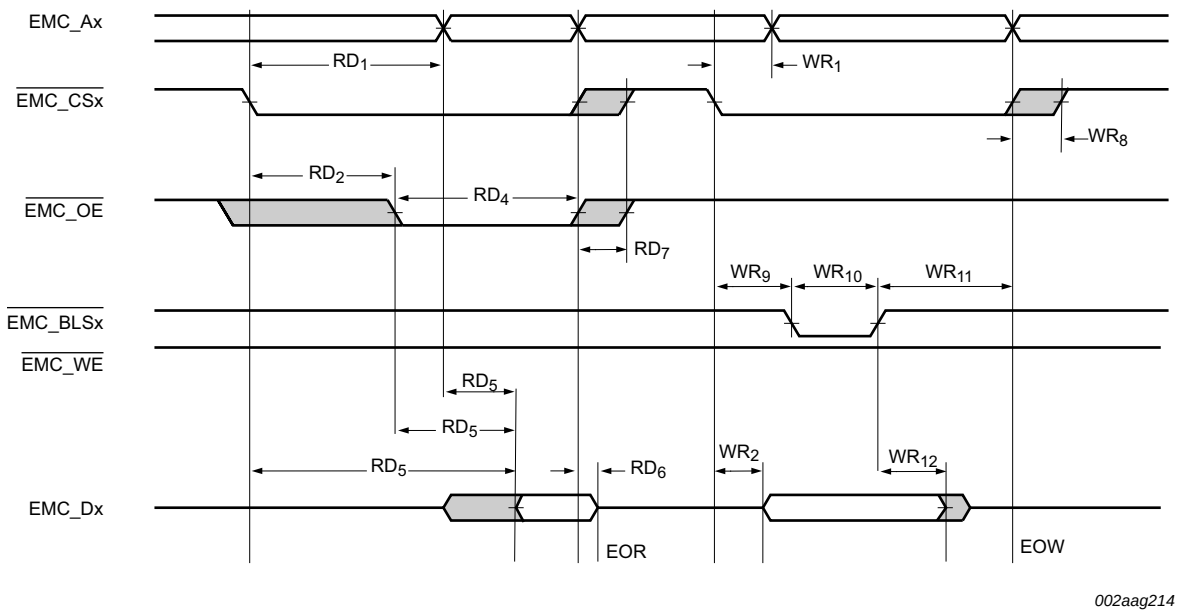

Fig 19. External static memory read/write access (PB = 0)

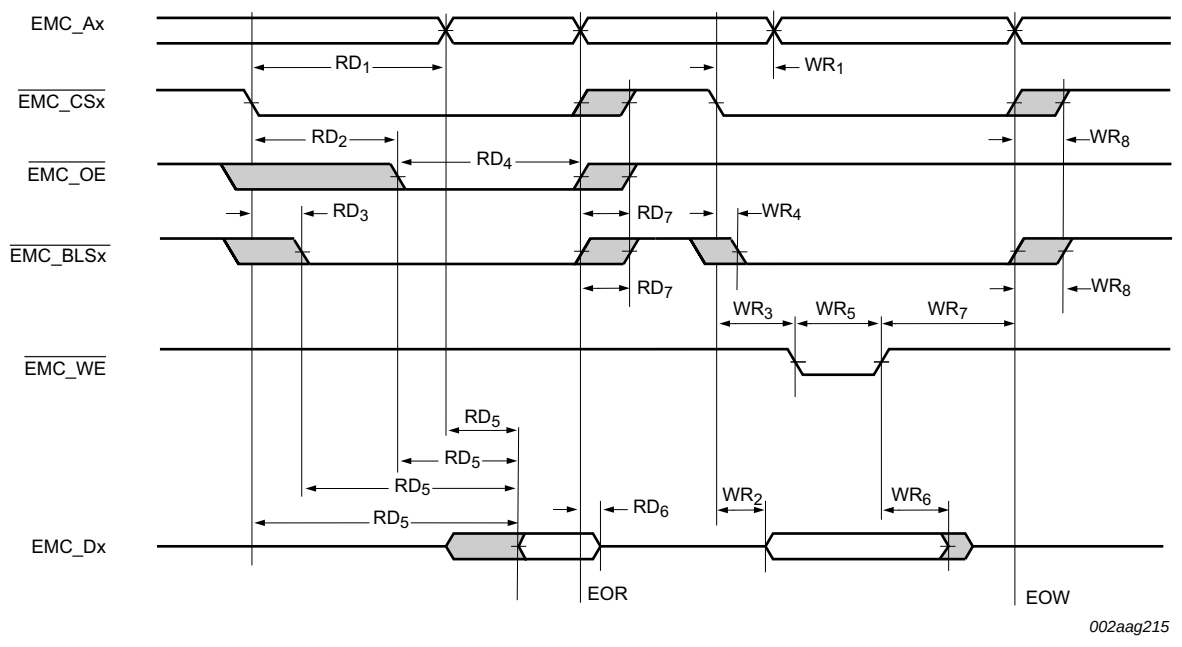

Fig 20. External static memory read/write access (PB =1)

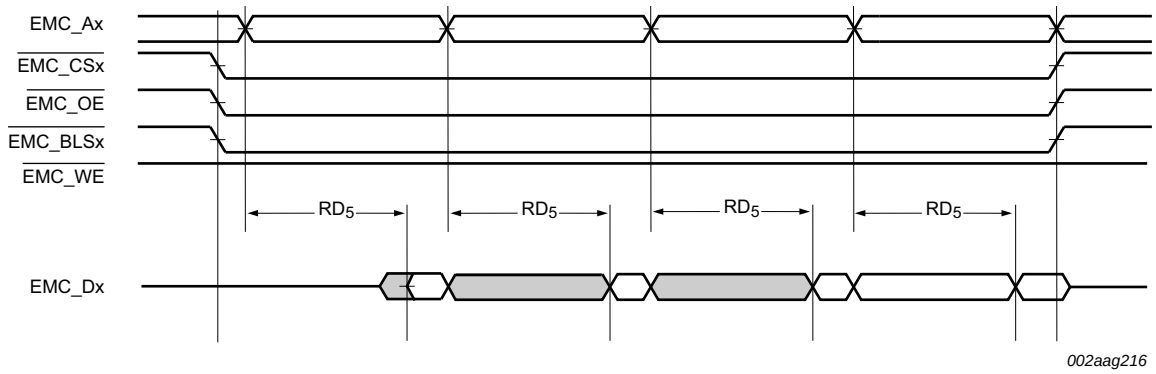

Fig 21. External static memory burst read cycle

Table 16. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time	[2]	-	$t_{clkndly}$ + 3.5	$t_{clk0dly}$ + 5.0	ns
$t_{h(S)}$	chip select hold time	[2]	$t_{clkndly}$ - 1.0	$t_{clkndly}$ - 1.2	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.6	$t_{clkndly}$ + 5.0	ns
$t_{h(RAS)}$	row address strobe hold time	[2]	$t_{clkndly}$ - 0.8	$t_{clkndly}$ - 0.9	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.4	$t_{clkndly}$ + 4.9	ns
$t_{h(CAS)}$	column address strobe hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 1.0	-	ns
$t_{d(WV)}$	write valid delay time	[2]	-	$t_{clkndly}$ + 4.1	$t_{clkndly}$ + 6.0	ns
$t_{h(W)}$	write hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 0.7		ns
$t_{d(AV)}$	address valid delay time	[2]	-	$t_{clkndly}$ + 4.6	$t_{clkndly}$ + 6.8	ns
$t_{h(A)}$	address hold time	[2]	$t_{clkndly}$ - 1.1	$t_{clkndly}$ - 1.2	-	ns
Read cycle parameters when EMC_CLKOUT0 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly}	4.5 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly}	-2.9 + t_{fbdly}	-	ns
Read cycle parameters when EMC_CLKOUT1 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	4.5 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-2.9 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time	[2]	-	$t_{clkndly}$+ 5.4	$t_{clkndly}$+ 7.8	ns
$t_{h(Q)}$	data output hold time	[2]	$t_{clkndly}$ − 0.4	$t_{clkndly}$	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] $t_{clkndly}$ represents $t_{clk0dly}$ when EMC_CLKOUT0 clocks SDRAM. $t_{clkndly}$represents $t_{clk1dly}$ when EMC_CLKOUT1 clocks SDRAM.

Table 17. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1 $t_{clk0dly}$ = 0 and $t_{clk1dly}$ = 0						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	t_{cmddly} + 6.8	t_{cmddly} + 10.4	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.2	t_{cmddly} + 2.1	-	ns

11.6 SSP interface

Table 22. Dynamic characteristics: SSP pins in SPI mode

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
SSP master						
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	30	-	ns
		when only transmitting		30	-	ns
t_{DS}	data set-up time	in SPI mode	[2]	14.8	-	ns
t_{DH}	data hold time	in SPI mode	[2]	2	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	6.3	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	−2.4	-	ns
SSP slave						
$T_{cy(clk)}$	clock cycle time		[3]	100	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	14.8	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	2	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	$3*T_{cy(PCLK)} + 6.3$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	−2.4	-	ns

[1] The minimum clock cycle time, and therefore the maximum frequency of the SSP in master mode, is limited by the pin electronics to the value given. The SSP block should not be configured to generate a clock faster than that. At and below the maximum frequency, $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] T_{amb} = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$. The maximum clock rate in slave mode is 1/12th of the PCLK rate.

[4] T_{amb} = 25 °C; $V_{DD(3V3)}$ = 3.3 V.

Table 28. 12-bit ADC characteristics *…continued*

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{c(ADC)}$	ADC conversion frequency	single conversion mode		-	-	400	kSamples/s
		burst mode		-	-	375	kSamples/s
C_{ia}	analog input capacitance			-	-	5	pF
R_{vsi}	voltage source interface resistance		[10]	-	-	1	kΩ
8-bit resolution[11]							
E_D	differential linearity error		[2][3][4]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	±1	-	LSB
E_O	offset error		[2][6]	-	±1	-	LSB
E_G	gain error		[2][7]	-	±1	-	LSB
E_T	absolute error		[2][8]	-	-	< ±1.5	LSB
$f_{clk(ADC)}$	ADC clock frequency			-	-	36	MHz
$f_{c(ADC)}$	ADC conversion frequency		[9]	-	-	1.16	MSamples/s
C_{ia}	analog input capacitance			-	-	5	pF
R_{vsi}	voltage source interface resistance		[10]	-	-	1	kΩ

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 32.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 32.

[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 32.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 32.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 32.

[9] In single-conversion mode.

[10] See Figure 33.

[11] 8-bit resolution is achieved by ignoring the lower four bits of the ADC conversion result.

16. Abbreviations

Table 36. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
GPS	Global Positioning System
HVAC	Heating, Venting, and Air Conditioning
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLC	Programmable Logic Controller
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCM	Tightly Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC408X_7X v.2	20130703	Product data sheet	-	LPC408X_7X v.1.1
	• Added LQFP100 and TFBGA80. • Table 3: – Removed overbar from NMI. – Added minimum reset pulse width of 50 ns to $\overline{\text{RESET}}$ pin. – Updated Table note 14 for RTCX pins (32 kHz crystal must be used to operate RTC). – Added boundary scan information to description for $\overline{\text{RESET}}$ pin. • Table 11: – Updated typ numbers for $I_{DD(REG)(3V3)}$ and I_{BAT}. – Added max values for deep sleep, power down, and deep PD for I_{BAT}. • Table 15, Table note 3: Changed $T_{cy(clk)}$ = 1/CCLK to $T_{cy(clk)}$ = 1/EMC_CLK. • Table 21: Removed reference to $\overline{\text{RESET}}$ pin from Table note 1. • Table 22: – Removed $T_{cy(PCLK)}$ spec; already given by the maximum chip frequency. – Changed min clock cycle time for SSP slave from 120 to 100. – Updated Table note 1 and Table note 3. • Section 7.24.1 “Features”: Changed max speed for SSP master from 60 to 33. • Updated EMC timing specs to C_L = 30 pF in Table 15, Table 16, Table 17, and Table 18. • SOT570-2 obsolete; replaced with SOT570-3.			
LPC408X_7X v.1.1	20121114	Product data sheet	-	LPC408X_7X v.1
Modifications:	• Changed data sheet status to Product.			
LPC408X_7X v.1	20120917	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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