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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4078fbd144-551

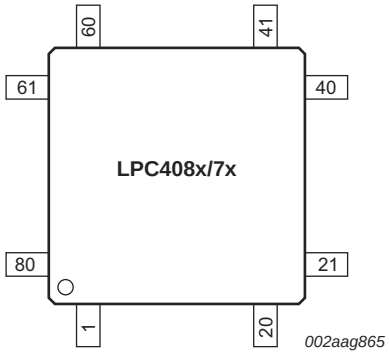


Fig 5. Pin configuration (LQFP80)

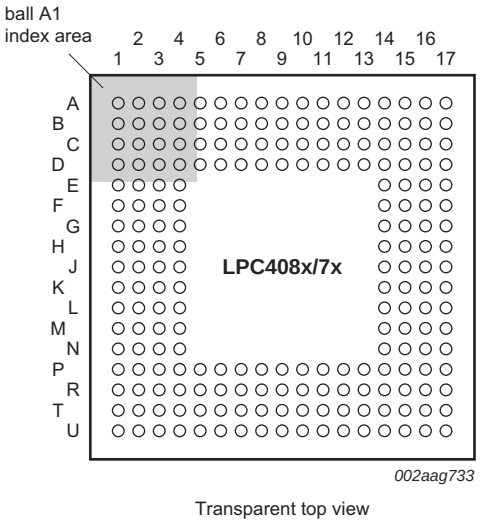


Fig 6. Pin configuration (TFBGA208)

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[14]	184	A7	D8	128	89	70	C6	[3]	I; PU	I/O	**P1[14] —** General purpose digital input/output pin.
										I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I	**CMP0_IN[0] —** Comparator 0, input 0.
P1[15]	182	A8	A8	126	88	69	B6	[3]	I; PU	I/O	**P1[15] —** General purpose digital input/output pin.
										I	**ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
										-	**R —** Function reserved.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
P1[16]	180	D10	B8	125	87	-	-	[3]	I; PU	I/O	**P1[16] —** General purpose digital input/output pin.
										O	**ENET_MDC —** Ethernet MIIM clock.
										O	**I2S_TX_MCLK —** I2S transmit master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[1] —** Comparator 0, input 1.
P1[17]	178	A9	C9	123	86	-	-	[3]	I; PU	I/O	**P1[17] —** General purpose digital input/output pin.
										I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
										O	**I2S_RX_MCLK —** I2S receive master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[2] —** Comparator 0, input 2.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[18]	66	P7	L5	46	32	25	K4	[3]	I; PU	I/O	**P1[18] —** General purpose digital input/output pin.
										O	**USB_UP_LED1 —** It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
										I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
										-	**R —** Function reserved.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P1[19]	68	U6	P5	47	33	26	J4	[3]	I; PU	I/O	**P1[19] —** General purpose digital input/output pin.
										O	**USB_TX_E1 —** Transmit Enable signal for USB port 1 (OTG transceiver).
										O	**USB_PPWR1 —** Port Power enable signal for USB port 1.
										I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
										O	**MC_0A —** Motor control PWM channel 0, output A.
										I/O	**SSP1_SCK —** Serial clock for SSP1.
										O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[24]	78	T9	P7	54	38	30	J6	[3]	I; PU	I/O	**P1[24] —** General purpose digital input/output pin.
										I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
										O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
										I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
										I	**MC_FB2 —** Motor control PWM channel 2 feedback input.
										I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
										O	**LCD_VD[10] —** LCD data.
										O	**LCD_VD[14] —** LCD data.
P1[25]	80	T10	L7	56	39	31	K6	[3]	I; PU	I/O	**P1[25] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_LS1}}$ —** Low Speed status for USB port 1 (OTG transceiver).
										O	**$\overline{\text{USB\_HSTEN1}}$ —** Host Enabled status for USB port 1.
										O	**T1_MAT1 —** Match output for Timer 1, channel 1.
										O	**MC_1A —** Motor control PWM channel 1, output A.
										O	**CLKOUT —** Selectable clock output.
										O	**LCD_VD[11] —** LCD data.
										O	**LCD_VD[15] —** LCD data.
P1[26]	82	R10	P8	57	40	32	H6	[3]	I; PU	I/O	**P1[26] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_SSPND1}}$ —** USB port 1 Bus Suspend status (OTG transceiver).
										O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
										I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
										O	**MC_1B —** Motor control PWM channel 1, output B.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**LCD_VD[12] —** LCD data.
										O	**LCD_VD[20] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P3[19]	161	B14	-	-	-	-	-	[3]	I; PU	I/O	**P3[19] —** General purpose digital input/output pin.
										I/O	**EMC_D[19] —** External memory data line 19.
										O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
P3[20]	167	A13	-	-	-	-	-	[3]	I; PU	I/O	**P3[20] —** General purpose digital input/output pin.
										I/O	**EMC_D[20] —** External memory data line 20.
										O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
										I	**U1_DSR —** Data Set Ready input for UART1.
P3[21]	175	C10	-	-	-	-	-	[3]	I; PU	I/O	**P3[21] —** General purpose digital input/output pin.
										I/O	**EMC_D[21] —** External memory data line 21.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
P3[22]	195	C6	-	-	-	-	-	[3]	I; PU	I/O	**P3[22] —** General purpose digital input/output pin.
										I/O	**EMC_D[22] —** External memory data line 22.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										I	**U1_RI —** Ring Indicator input for UART1.
P3[23]	65	T6	M4	45	-	-	-	[3]	I; PU	I/O	**P3[23] —** General purpose digital input/output pin.
										I/O	**EMC_D[23] —** External memory data line 23.
										I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
										I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
P3[24]	58	R5	N3	40	-	-	-	[3]	I; PU	I/O	**P3[24] —** General purpose digital input/output pin.
										I/O	**EMC_D[24] —** External memory data line 24.
										O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
										I	**T0_CAP1 —** Capture input for Timer 0, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P4[7]	121	L16	K12	84	-	-	-	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
										I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	-	-	-	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
										I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	-	-	-	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
										I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	-	-	-	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
										I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	-	-	-	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
										I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	-	-	-	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
										I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	-	-	-	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
										I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	-	-	-	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
										I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	-	-	-	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
										I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	-	-	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
										I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	-	-	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
										I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	-	-	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
										I/O	**EMC_A[18] —** External memory address line 18.
P4[19]	111	P16	M14	-	-	-	-	[3]	I; PU	I/O	**P4[19] —** General purpose digital input/output pin.
										I/O	**EMC_A[19] —** External memory address line 19.

operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the ARM Cortex-M4 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.15.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.
- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.33.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source is a dedicated watchdog oscillator, which is always running if the watchdog timer is enabled.

7.34 RTC and backup registers

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC on the LPC408x/7x is designed to have extremely low power consumption, i.e. less than 1 μA. The RTC will typically run from the main chip power supply conserving battery power while the rest of the device is powered up. When operating from a battery, the RTC will continue working down to 2.1 V. Battery power can be provided from a standard 3 V lithium button cell.

An ultra-low power 32 kHz oscillator will provide a 1 Hz clock to the time counting portion of the RTC, moving most of the power consumption out of the time counting function.

The RTC includes a calibration mechanism to allow fine-tuning the count rate in a way that will provide less than 1 second per day error when operated at a constant voltage and temperature.

The RTC contains a small set of backup registers (20 bytes) for holding data while the main part of the LPC408x/7x is powered off.

The RTC includes an alarm function that can wake up the LPC408x/7x from all reduced power modes with a time resolution of 1 s.

7.34.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.

7.36.3 Wake-up timer

The LPC408x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.36.4 Power control

The LPC408x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC408x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

7.36.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly” while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. There is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available and $V_{DD(REG)(3V3)} > V_{BAT}$.

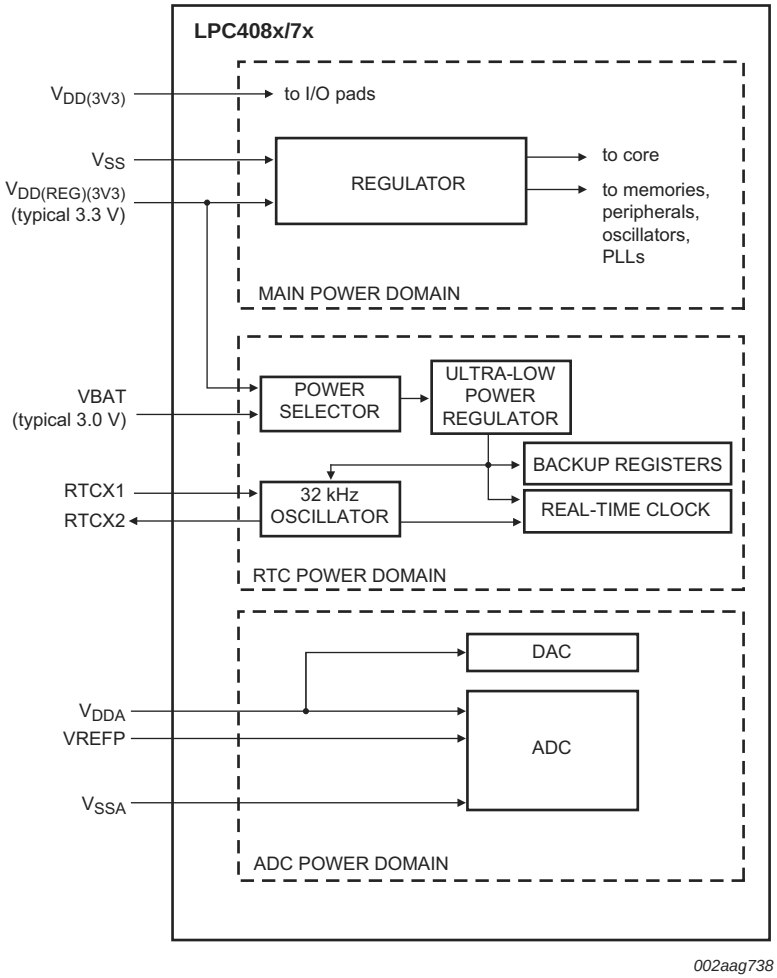
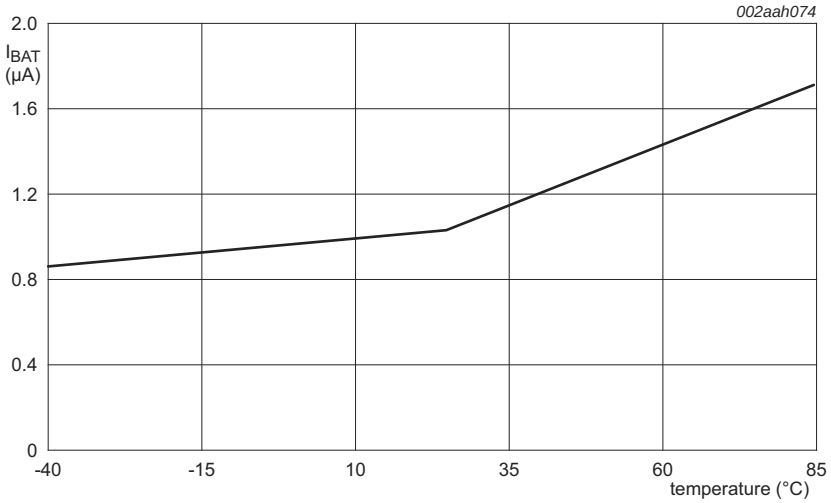


Fig 11. Power distribution



Conditions: $V_{DD(REG)(3V3)} = V_{DDA} = V_{DD(3V3)} = 0$; $V_{BAT} = 3.0$ V.

Fig 14. Part powered off: Typical battery supply current (I_{BAT}) versus temperature

10.2 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the PCONP register. All other blocks are disabled and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. The peripheral clock was set to PCLK = CCLK/4 with CCLK = 12 MHz, 48 MHz, and 120 MHz.

The combined current of several peripherals running at the same time can be less than the sum of each individual peripheral current measured separately.

Table 12. Power consumption for individual analog and digital blocks
T_{amb} = 25 °C; $V_{DD(REG)(3V3)} = V_{DD(3V3)} = V_{DDA}$ = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
Timer0		0.01	0.06	0.15
Timer1		0.02	0.07	0.16
Timer2		0.02	0.07	0.17
Timer3		0.01	0.07	0.16
Timer0 + Timer1 + Timer2 + Timer3		0.07	0.28	0.67
UART0		0.05	0.19	0.45
UART1		0.06	0.24	0.56
UART2		0.05	0.2	0.47
UART3		0.06	0.23	0.56
USART4		0.07	0.27	0.66
UART0 + UART1 + UART2 + UART3 + USART4		0.29	1.13	2.74
PWM0 + PWM1		0.08	0.31	0.75

11. Dynamic characteristics

11.1 Flash memory

Table 13. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 14. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			200	375	400	kHz
N_{endu}	endurance			100000	500000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	64 bytes	[1]	-	1.8	-	ms
t_{prog}	programming time	64 bytes	[1]	-	1.1	-	ms

[1] EEPROM clock frequency = 375 kHz. Programming/erase times increase with decreasing EEPROM clock frequency.

11.2 External memory interface

Table 15. Dynamic characteristics: Static external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		3.3	4.3	6.1	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[3]	2.4 + $T_{cy(clk)}$ × WAITOEN	3.1 + $T_{cy(clk)}$ × WAITOEN	4.2 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[3]	2.7	3.5	4.9	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.2	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 3.8	ns

[2] Parameters specified for 40 % of $V_{DD(3V3)}$ for rising edges and 60 % of $V_{DD(3V3)}$ for falling edges.

[3] $T_{cy(clk)}$ = 1/EMC_CLK (see *LPC408x/7x User manual*).

[4] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[5] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[6] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

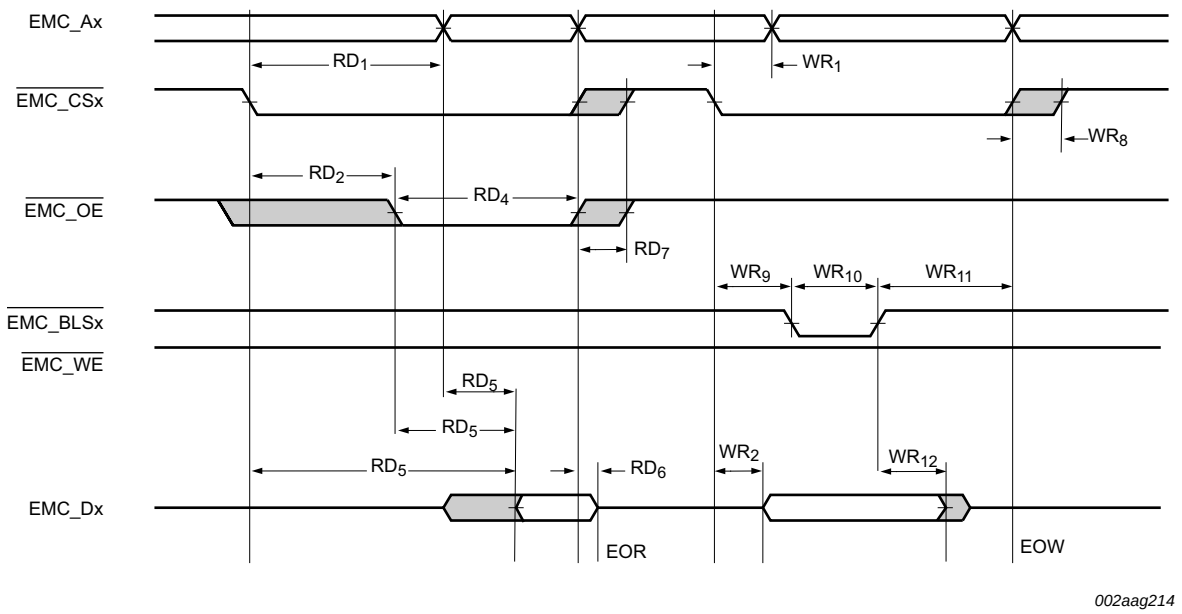


Fig 19. External static memory read/write access (PB = 0)

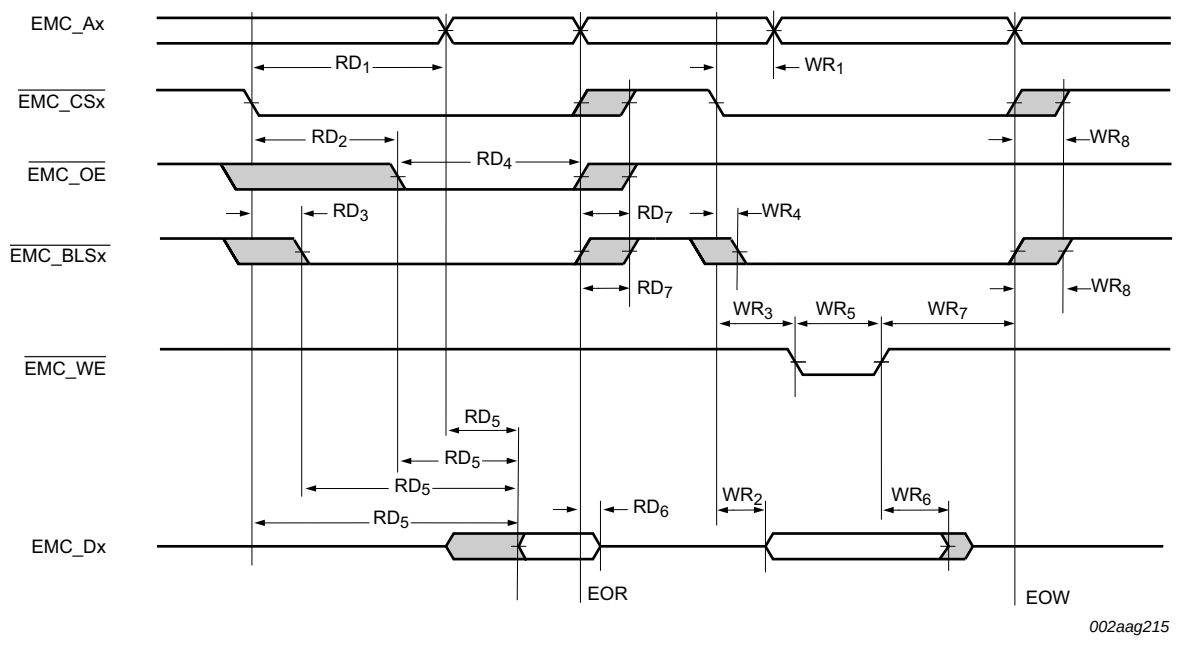


Fig 20. External static memory read/write access (PB =1)

Table 17. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 *…continued*
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
$t_{d(RASV)}$	row address strobe valid delay time		-	t_{cmddly} + 6.8	t_{cmddly} + 10.4	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 2.3	t_{cmddly} + 4.3	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	t_{cmddly} + 6.7	t_{cmddly} + 10.2	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 2.2	t_{cmddly} + 4.1	-	ns
$t_{d(WV)}$	write valid delay time		-	t_{cmddly} + 7.1	t_{cmddly} + 10.9	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 1.5	t_{cmddly} + 2.7	-	ns
$t_{d(AV)}$	address valid delay time		-	t_{cmddly} + 7.7	t_{cmddly} + 11.9	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.0	t_{cmddly} + 1.8	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly}	4.5 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly}	-2.9 + t_{fbdly}	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	t_{cmddly} + 8.7	t_{cmddly} + 13.1	ns
$t_{h(Q)}$	data output hold time		t_{cmddly} + 1.0	t_{cmddly} + 2.0	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

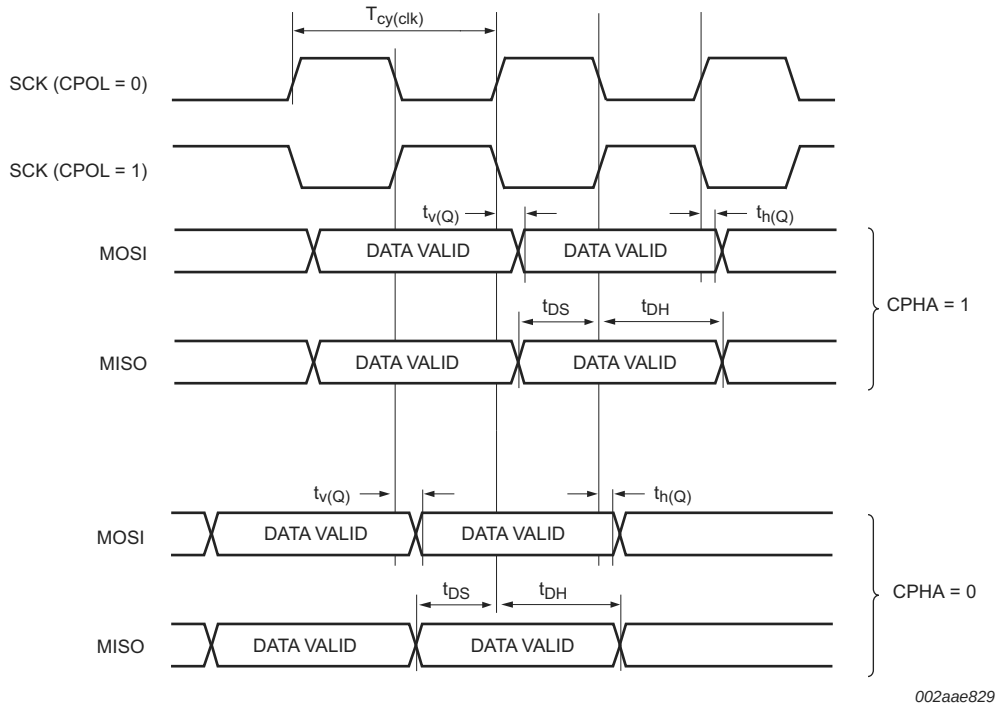


Fig 24. SSP master timing in SPI mode

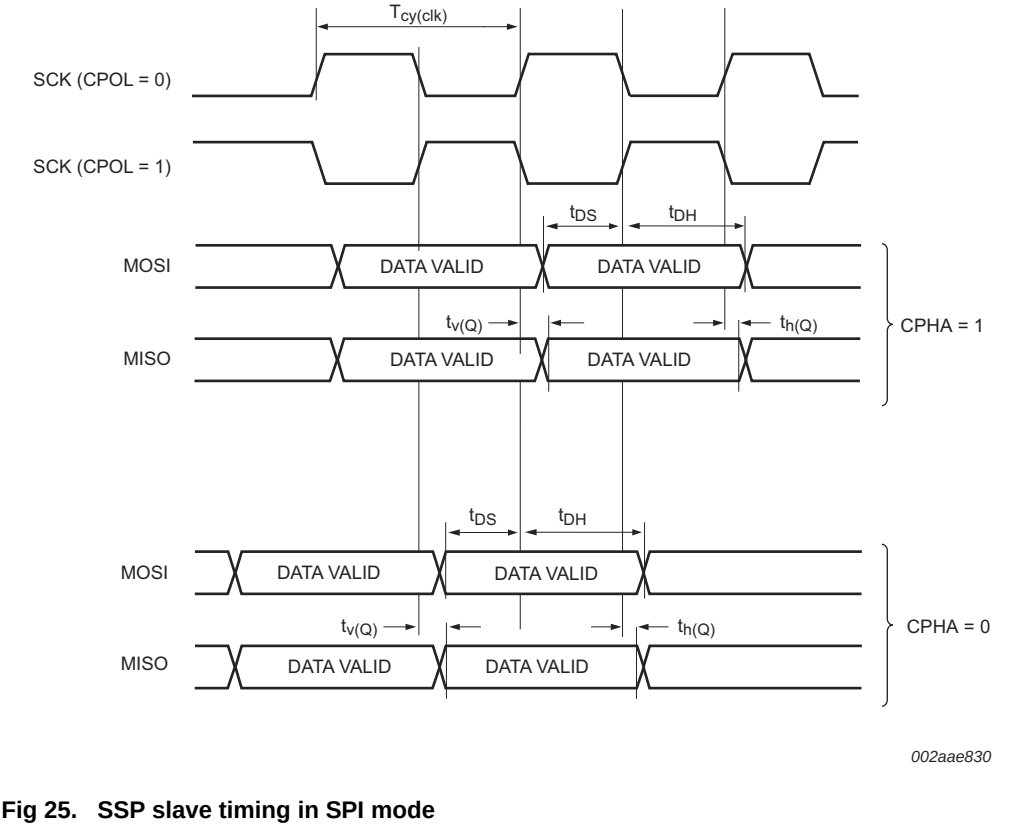


Fig 25. SSP slave timing in SPI mode

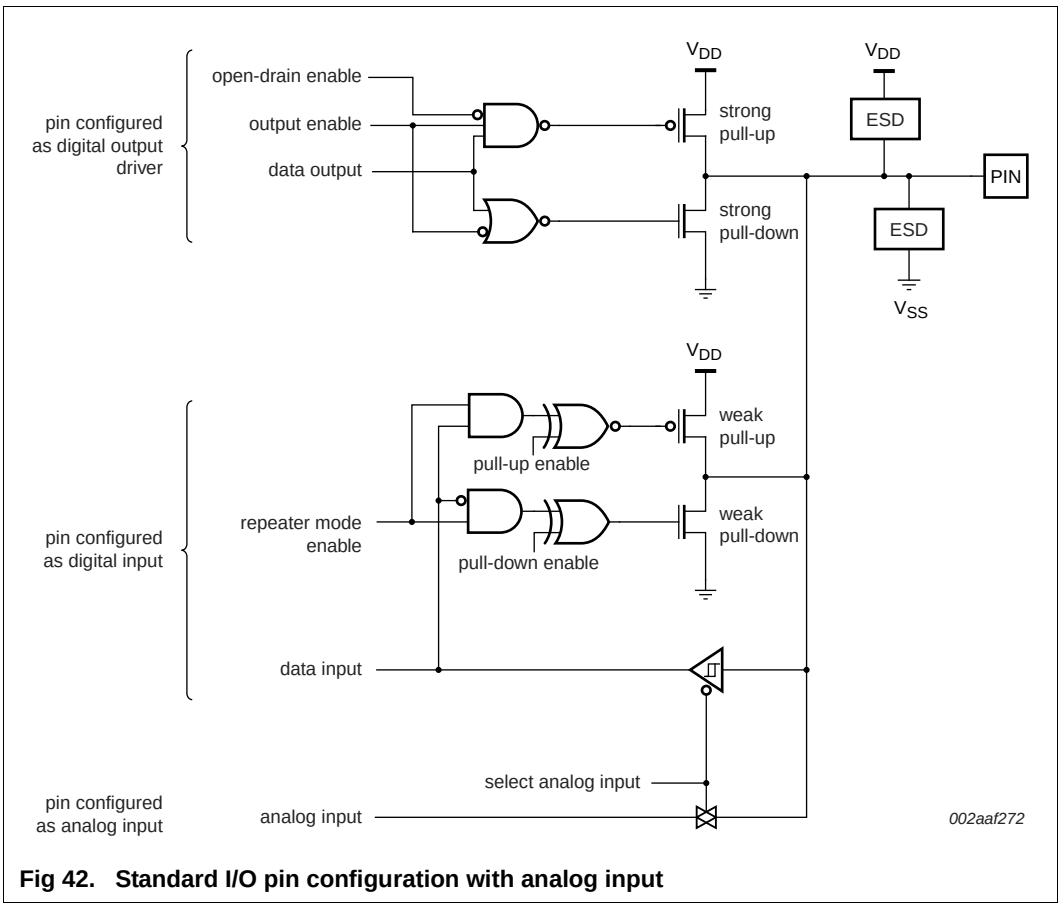


Fig 42. Standard I/O pin configuration with analog input

13.5 Reset pin configuration

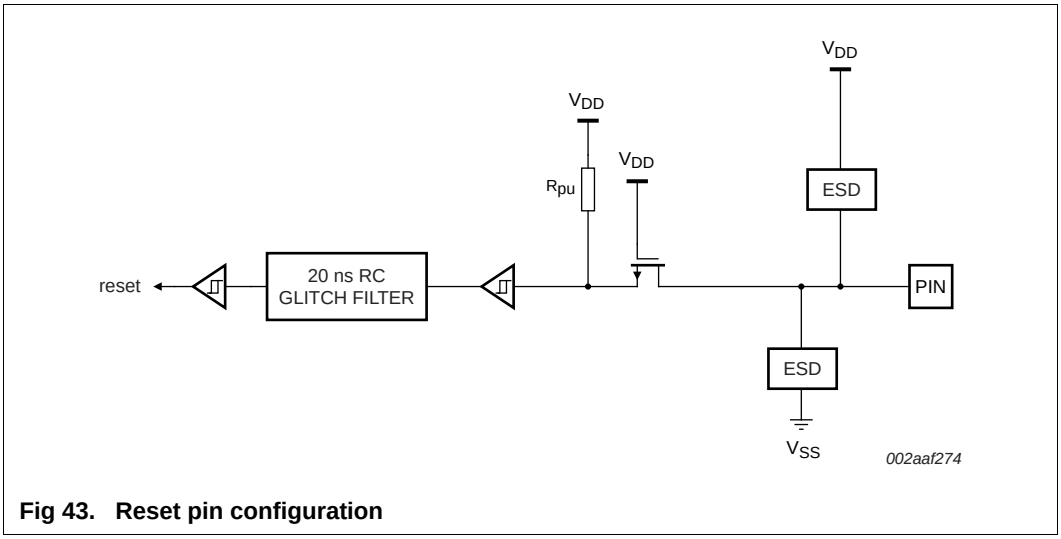


Fig 43. Reset pin configuration

13.6 Reset pin configuration for RTC operation

Under certain circumstances, the RTC may temporarily pause and lose fractions of a second during the rising and falling edges of the $\overline{\text{RESET}}$ signal.

To eliminate the loss of time counts in the RTC due to voltage swing or ramp rate of the $\overline{\text{RESET}}$ signal, connect an RC filter between the $\overline{\text{RESET}}$ pin and the external reset input.

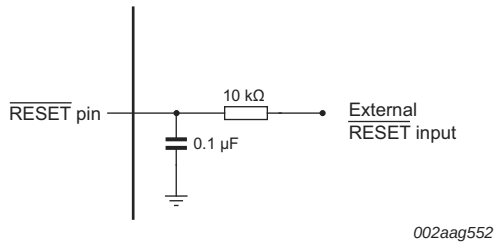
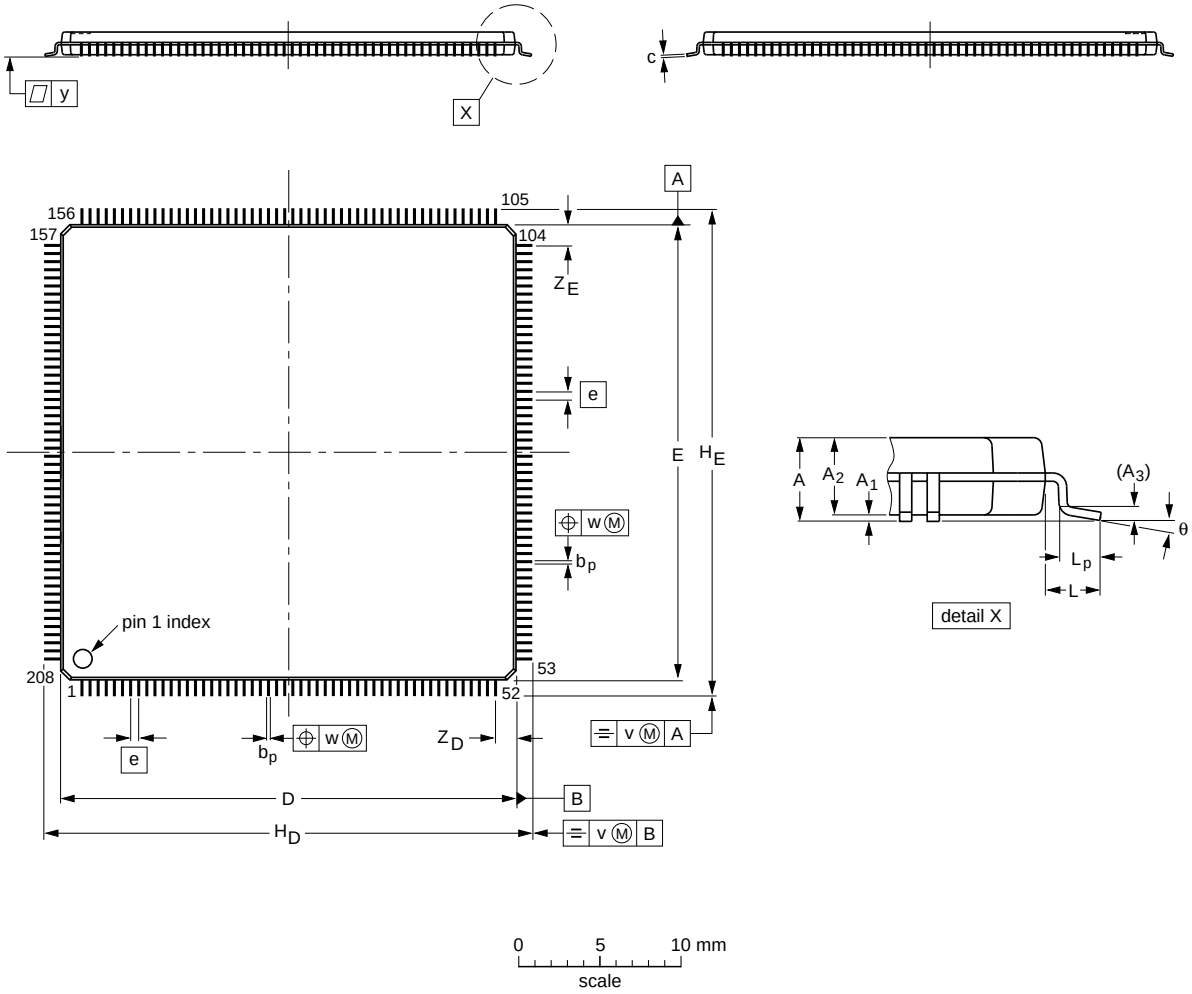


Fig 44. Reset input with RC filter

14. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

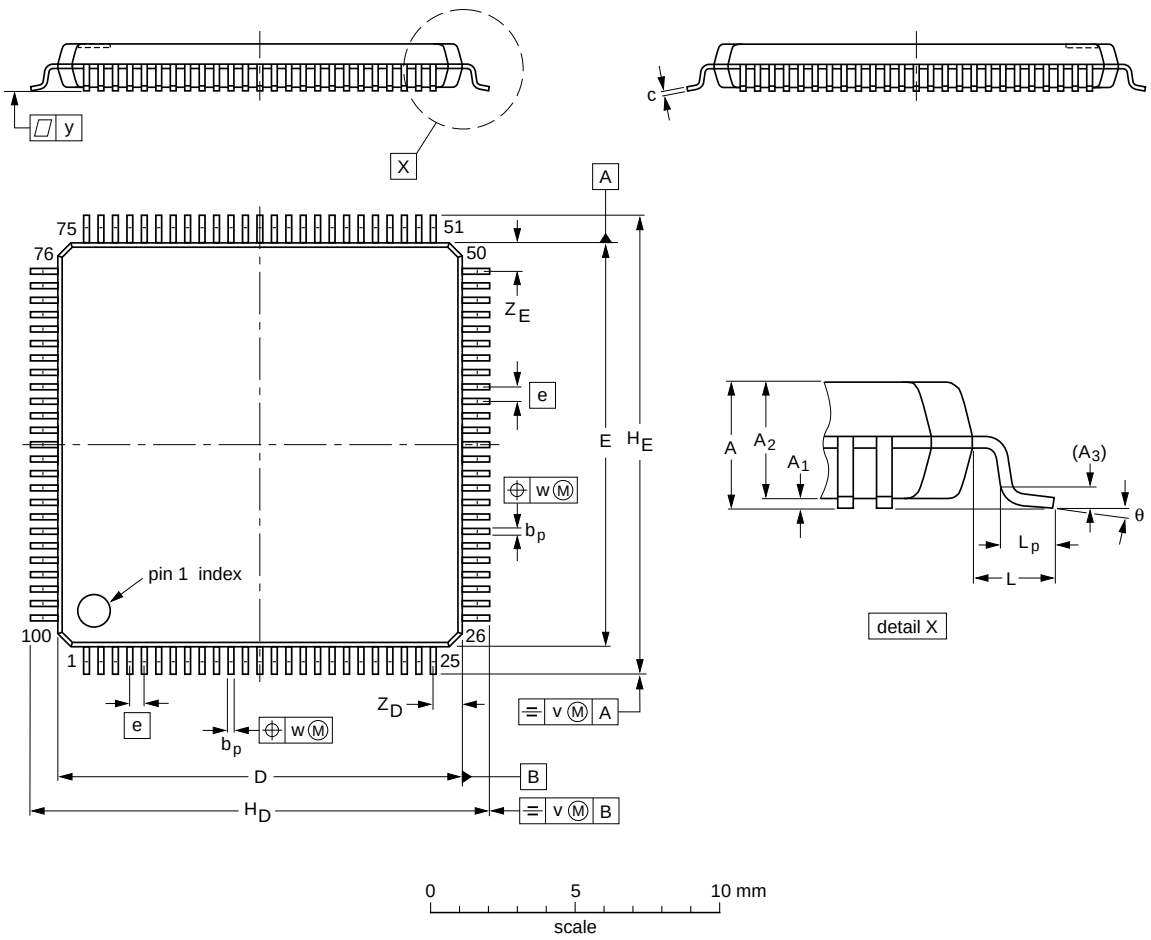
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 45. Package outline SOT459-1 (LQFP208)

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

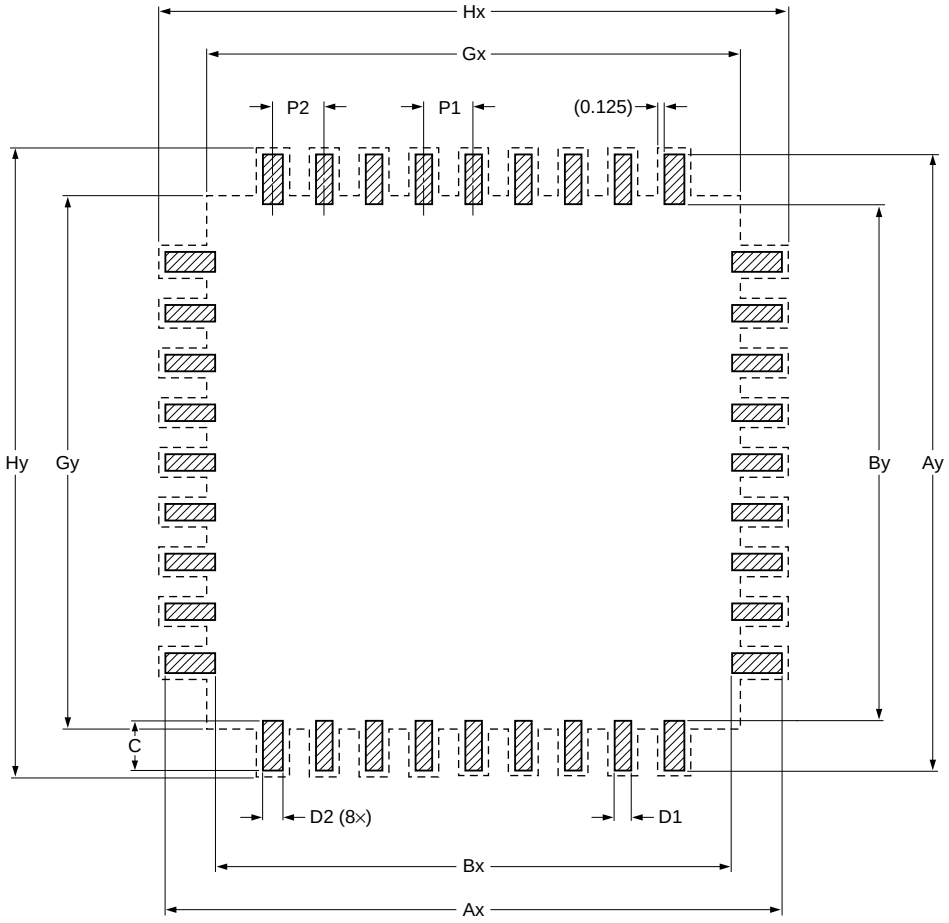
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 49. Package outline SOT407-1 (LQFP100)

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 54. Reflow soldering of the LQFP144 package