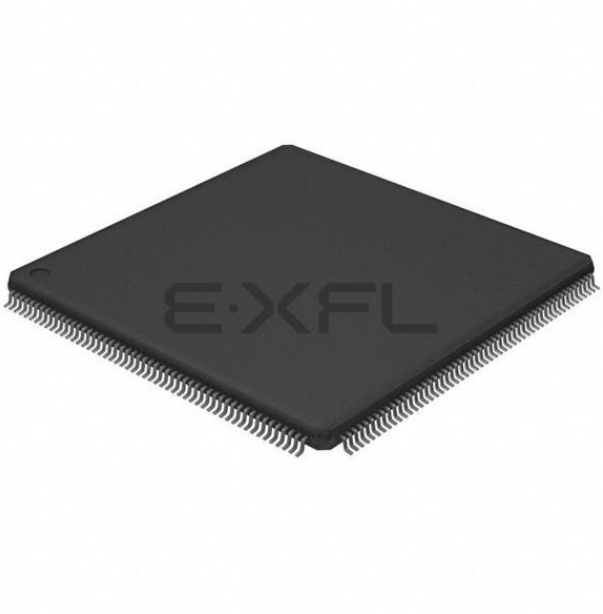

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4078fbd208-551

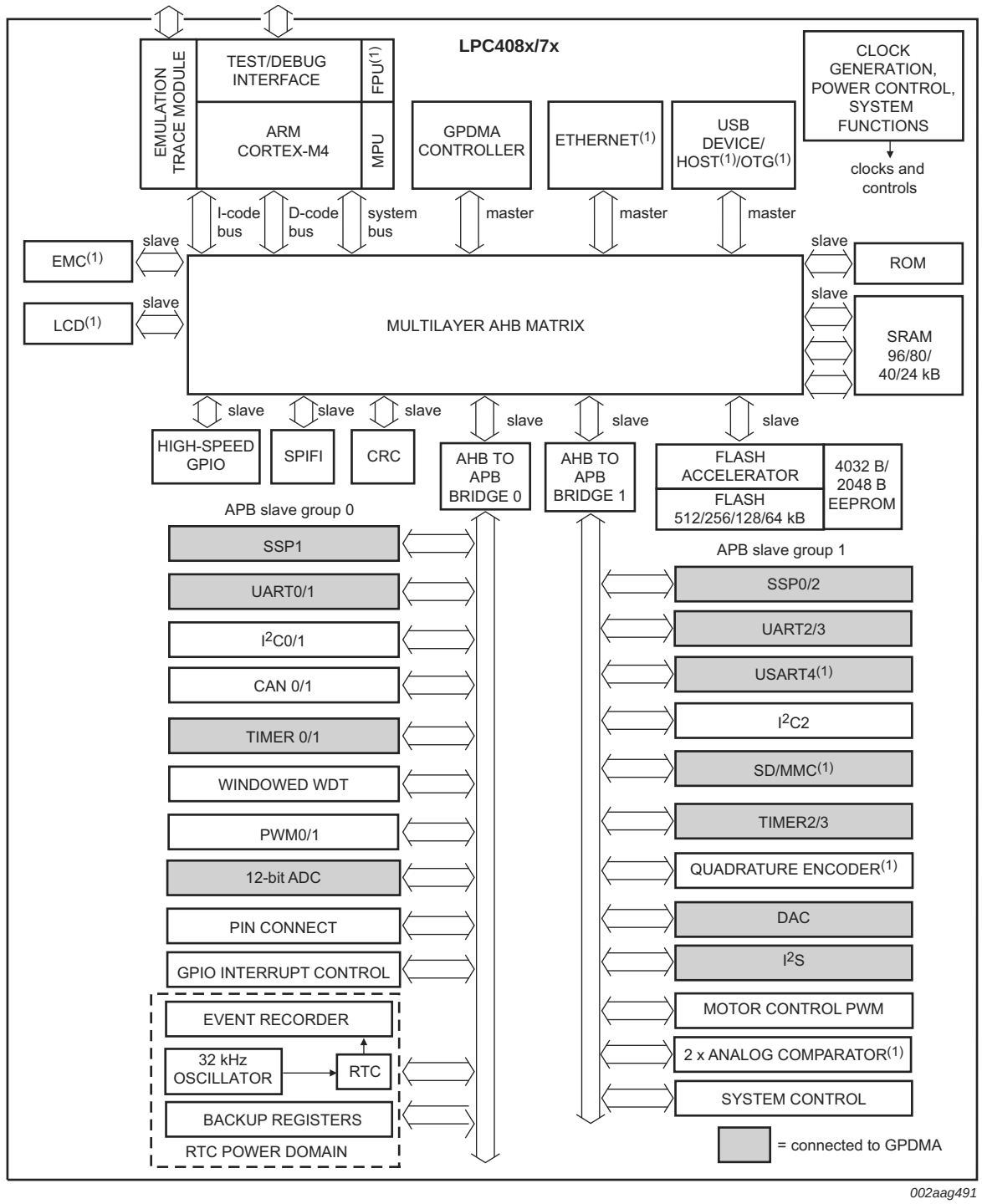
- 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support.
- Two analog comparators.

- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
  - Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
  - Brownout detect with separate threshold for interrupt and forced reset.
  - On-chip Power-On Reset (POR).
- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1 % accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, LQFP144, TFBGA80, and LQFP80 package.

3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

5. Block diagram



(1) Not available on all parts.

Fig 1. Block diagram

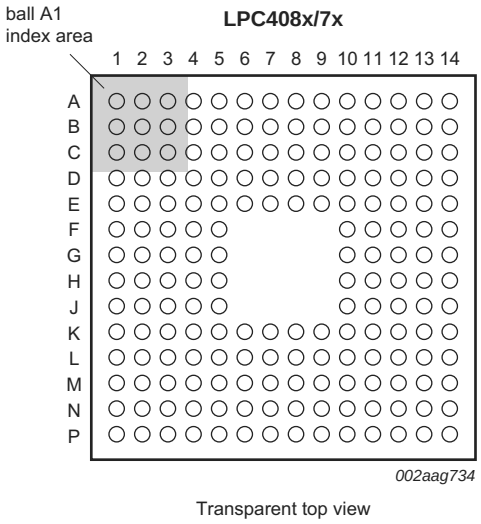


Fig 7. Pin configuration (TFBGA180)

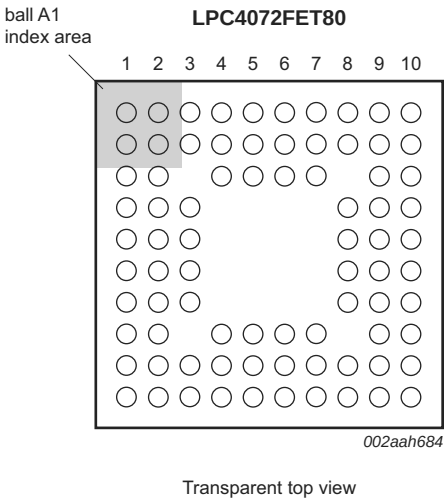


Fig 8. Pin configuration (TFBGA80)

6.2 Pin description

I/O pins on the LPC408x/7x are 5 V tolerant and have input hysteresis unless otherwise indicated in the table below. Crystal pins, power pins, and reference voltage pins are not 5 V tolerant. In addition, when pins are selected to be ADC inputs, they are no longer 5 V tolerant and the input voltage must be limited to the voltage at the ADC positive reference pin (VREFP).

All port pins Pn[m] are multiplexed, and the multiplexed functions appear in Table 3 in the order defined by the FUNC bits of the corresponding IOCON register up to the highest used function number. Each port pin can support up to eight multiplexed functions. IOCON register FUNC values which are reserved are noted as “R” in the pin configuration table.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[3]	144	E16	E13	100	70	55	C10	[3]	I; PU	I/O	**P2[3] —** General purpose digital input/output pin.
										O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
										O	**T2_MAT2 —** Match output for Timer 2, channel 2.
										-	**R —** Function reserved.
										O	**TRACEDATA[2] —** Trace data, bit 2.
										-	**R —** Function reserved.
										O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
P2[4]	142	D17	E14	99	69	54	C9	[3]	I; PU	I/O	**P2[4] —** General purpose digital input/output pin.
										O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
										I	**U1_DSR —** Data Set Ready input for UART1.
										O	**T2_MAT1 —** Match output for Timer 2, channel 1.
										-	**R —** Function reserved.
										O	**TRACEDATA[1] —** Trace data, bit 1.
										-	**R —** Function reserved.
										O	**LCD_ENAB_M —** STN AC bias drive or TFT data enable output.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[31]	39	N2	-	-	-	-	-	[3]	I; PU	I/O	**P2[31] —** General purpose digital input/output pin.
										O	**EMC_DQM3 —** Data mask 3 used with SDRAM and static devices.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT3 —** Match output for Timer 3, channel 3.
P3[0] to P3[31]										I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block.
P3[0]	197	B4	D6	137	-	-	-	[3]	I; PU	I/O	**P3[0] —** General purpose digital input/output pin.
										I/O	**EMC_D[0] —** External memory data line 0.
P3[1]	201	B3	E6	140	-	-	-	[3]	I; PU	I/O	**P3[1] —** General purpose digital input/output pin.
										I/O	**EMC_D[1] —** External memory data line 1.
P3[2]	207	B1	A2	144	-	-	-	[3]	I; PU	I/O	**P3[2] —** General purpose digital input/output pin.
										I/O	**EMC_D[2] —** External memory data line 2.
P3[3]	3	E4	G5	2	-	-	-	[3]	I; PU	I/O	**P3[3] —** General purpose digital input/output pin.
										I/O	**EMC_D[3] —** External memory data line 3.
P3[4]	13	F2	D3	9	-	-	-	[3]	I; PU	I/O	**P3[4] —** General purpose digital input/output pin.
										I/O	**EMC_D[4] —** External memory data line 4.
P3[5]	17	G1	E3	12	-	-	-	[3]	I; PU	I/O	**P3[5] —** General purpose digital input/output pin.
										I/O	**EMC_D[5] —** External memory data line 5.
P3[6]	23	J1	F4	16	-	-	-	[3]	I; PU	I/O	**P3[6] —** General purpose digital input/output pin.
										I/O	**EMC_D[6] —** External memory data line 6.
P3[7]	27	L1	G3	19	-	-	-	[3]	I; PU	I/O	**P3[7] —** General purpose digital input/output pin.
										I/O	**EMC_D[7] —** External memory data line 7.
P3[8]	191	D8	A6	-	-	-	-	[3]	I; PU	I/O	**P3[8] —** General purpose digital input/output pin.
										I/O	**EMC_D[8] —** External memory data line 8.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P5[0] to P5[4]										I/O	**Port 5:** Port 5 is a 5-bit I/O port with individual direction controls for each bit. The operation of port 5 pins depends upon the pin function selected via the pin connect block.
P5[0]	9	F4	E5	6	-	-	-	[3]	I; PU	I/O	**P5[0] —** General purpose digital input/output pin.
										I/O	**EMC_A[24] —** External memory address line 24.
										I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
										O	**T2_MAT2 —** Match output for Timer 2, channel 2.
P5[1]	30	J4	H1	21	-	-	G1	[3]	I; PU	I/O	**P5[1] —** General purpose digital input/output pin.
										I/O	**EMC_A[25] —** External memory address line 25.
										I/O	**SSP2_MISO —** Master In Slave Out for SSP2.
										O	**T2_MAT3 —** Match output for Timer 2, channel 3.
P5[2]	117	L14	L12	81	-	-	-	[11]	I	I/O	**P5[2] —** General purpose digital input/output pin.
										-	**R —** Function reserved.
										I/O	**SSP2_SCK —** Serial clock for SSP2. When using this pin, the SSP2 bit rate is limited to 1 MHz.
										O	**T3_MAT2 —** Match output for Timer 3, channel 2.
										-	**R —** Function reserved.
										I/O	**I2C0_SDA —** I^2C0 data input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).
P5[3]	141	G14	G10	98	-	-	-	[11]	I	I/O	**P5[3] —** General purpose digital input/output pin.
										-	**R —** Function reserved.
										I/O	**SSP2_SSEL —** Slave select for SSP2. When using this pin, the SSP2 bit rate is limited to 1 MHz.
										-	**R —** Function reserved.
										I	**U4_RXD —** Receiver input for USART4.
										I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus.

Table 4. LPC408x/7x memory usage and details

Address range	General Use	Address range details and description	
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 to 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)
		0x9000 0000 to 0x93FF FFFF	Static memory chip select 1 (up to 64 MB)
		0x9800 0000 to 0x9BFF FFFF	Static memory chip select 2 (up to 64 MB)
		0x9C00 0000 to 0x9FFF FFFF	Static memory chip select 3 (up to 64 MB)
		Four dynamic memory chip selects:	
		0xA000 0000 to 0xAFFF FFFF	Dynamic memory chip select 0 (up to 256 MB)
		0xB000 0000 to 0xBFFF FFFF	Dynamic memory chip select 1 (up to 256 MB)
		0xC000 0000 to 0xCFFF FFFF	Dynamic memory chip select 2 (up to 256 MB)
		0xD000 0000 to 0xDFFF FFFF	Dynamic memory chip select 3 (up to 256 MB)
0xE000 0000 to 0xE00F FFFF	Cortex-M4 Private Peripheral Bus	0xE000 0000 to 0xE00F FFFF	Cortex-M4 related functions, includes the NVIC and System Tick Timer.

The LPC408x/7x incorporate several distinct memory regions, shown in the following figures. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

7.9 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.9.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC408x/7x, the NVIC supports 40 vectored interrupts.
- 32 programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.9.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on port 0 and port 2 regardless of the selected function can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

7.10 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupts being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

7.11 External Memory Controller (EMC)

Remark: The EMC is available for parts LPC4088/78/76. Supported memory size and type and EMC bus width vary for different packages (see Table 2). The EMC pin configuration for each part is shown in Table 5.

Table 5. External memory controller pin configuration

Parts	Data bus pins	Address bus pins	Control pins	
			SRAM	**SDRAM**
LPC4088FBD208 LPC4088FET208 LPC4078FBD208 LPC4078FET208	EMC_D[31:0]	EMC_A[25:0]	$\overline{\text{EMC\_BLS}}$[3:0], $\overline{\text{EMC\_CS}}$[3:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC4088FET180 LPC4078FET180 LPC4076FET180	EMC_D[15:0]	EMC_A[19:0]	$\overline{\text{EMC\_BLS}}$[1:0], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC4088FBD144 LPC4078FBD144 LPC4076FBD144	EMC_D[7:0]	EMC_A[15:0]	$\overline{\text{EMC\_BLS}}$[3:2], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	not available

The LPC408x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

- FullCAN messages can generate interrupts.

7.28 General purpose 32-bit timers/external event counters

The LPC408x/7x include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.28.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.29 Pulse Width Modulator (PWM)

The LPC408x/7x contain two standard PWMs.

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC408x/7x. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge

7.33.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source is a dedicated watchdog oscillator, which is always running if the watchdog timer is enabled.

7.34 RTC and backup registers

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC on the LPC408x/7x is designed to have extremely low power consumption, i.e. less than 1 μA. The RTC will typically run from the main chip power supply conserving battery power while the rest of the device is powered up. When operating from a battery, the RTC will continue working down to 2.1 V. Battery power can be provided from a standard 3 V lithium button cell.

An ultra-low power 32 kHz oscillator will provide a 1 Hz clock to the time counting portion of the RTC, moving most of the power consumption out of the time counting function.

The RTC includes a calibration mechanism to allow fine-tuning the count rate in a way that will provide less than 1 second per day error when operated at a constant voltage and temperature.

The RTC contains a small set of backup registers (20 bytes) for holding data while the main part of the LPC408x/7x is powered off.

The RTC includes an alarm function that can wake up the LPC408x/7x from all reduced power modes with a time resolution of 1 s.

7.34.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.

The DMA controller can continue to work in Sleep mode and has access to the peripheral RAMs and all peripheral registers. The flash memory and the main SRAM are not available in Sleep mode, they are disabled in order to save power.

Wake-up from Sleep mode will occur whenever any enabled interrupt occurs.

7.36.4.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down to allow fast wake-up. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The clock divider registers are automatically reset to zero.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

Wake-up from Deep-sleep mode can initiated by the NMI, External Interrupts $\overline{\text{EINT0}}$ through $\overline{\text{EINT3}}$, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a USB input pin transition (USB activity interrupt), a CAN input pin transition, or a Watchdog Timer time-out, when the related interrupt is enabled. Wake-up will occur whenever any enabled interrupt occurs.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after four cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

7.36.4.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

When the chip enters Power-down mode, the IRC, the main oscillator, and all clocks are stopped. The RTC remains running if it has been enabled and RTC interrupts may be used to wake up the CPU. The flash is forced into Power-down mode. The PLLs are automatically turned off and the clock selection multiplexers are set to use the system clock sysclk (the reset state). The clock divider control registers are automatically reset to zero. If the Watchdog timer is running, it will continue running in Power-down mode.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this four IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 12 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

Table 8. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 9. Thermal resistance (LQFP packages)

T_{amb} = −40 °C to +85 °C unless otherwise specified.

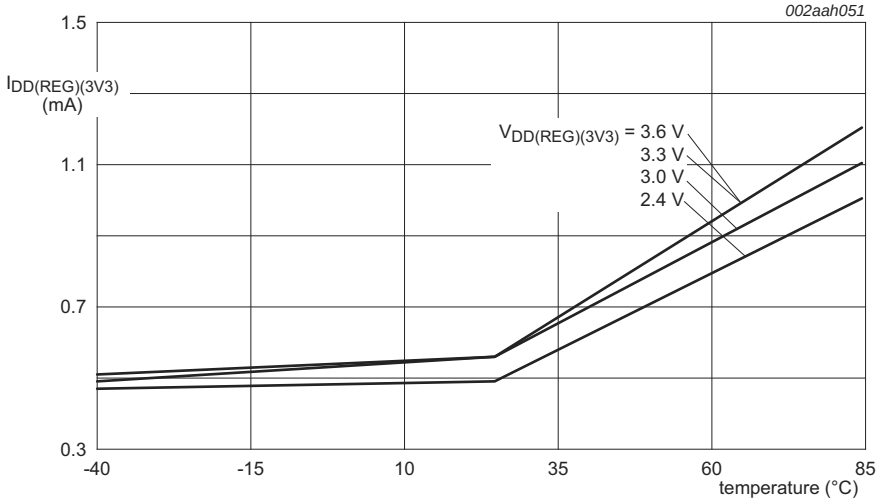
		Thermal resistance value (°C/W): ±15 %		
		LQFP80	**LQFP144**	**LQFP208**
θja				
	JEDEC (4.5 in × 4 in)			
	0 m/s	41	31	27
	1 m/s	35	28	25
	2.5 m/s	32	26	24
	Single-layer (4.5 in × 3 in)			
	0 m/s	61	43	35
	1 m/s	47	35	31
	2.5 m/s	43	33	29
θjc		7.8	9.2	10.5
θjb		11.6	13.5	15.2

Table 10. Thermal resistance value (TFBGA packages)

T_{amb} = −40 °C to +85 °C unless otherwise specified.

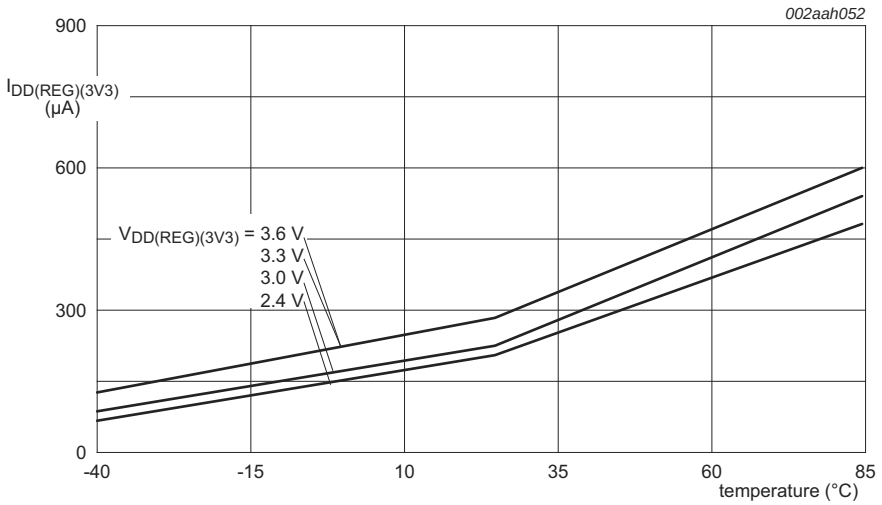
		Thermal resistance value (°C/W): ±15 %	
		TFBGA180	**TFBGA208**
θja			
	JEDEC (4.5 in × 4 in)		
	0 m/s	47	43
	1 m/s	39	37
	2.5 m/s	35	33
	8-layer (4.5 in × 3 in)		
	0 m/s	39	37
	1 m/s	35	33
	2.5 m/s	31	30
θjc		8.5	7.4
θjb		13	16

10.1 Power consumption



Conditions: BOD disabled.

Fig 12. Deep-sleep mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature



Conditions: BOD disabled.

Fig 13. Power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature

11. Dynamic characteristics

11.1 Flash memory

Table 13. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 14. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			200	375	400	kHz
N_{endu}	endurance			100000	500000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	64 bytes	[1]	-	1.8	-	ms
t_{prog}	programming time	64 bytes	[1]	-	1.1	-	ms

[1] EEPROM clock frequency = 375 kHz. Programming/erase times increase with decreasing EEPROM clock frequency.

11.2 External memory interface

Table 15. Dynamic characteristics: Static external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		3.3	4.3	6.1	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[3]	2.4 + $T_{cy(clk)}$ × WAITOEN	3.1 + $T_{cy(clk)}$ × WAITOEN	4.2 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[3]	2.7	3.5	4.9	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.2	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 3.8	ns

[2] Parameters specified for 40 % of $V_{DD(3V3)}$ for rising edges and 60 % of $V_{DD(3V3)}$ for falling edges.

[3] $T_{cy(clk)}$ = 1/EMC_CLK (see *LPC408x/7x User manual*).

[4] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[5] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[6] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

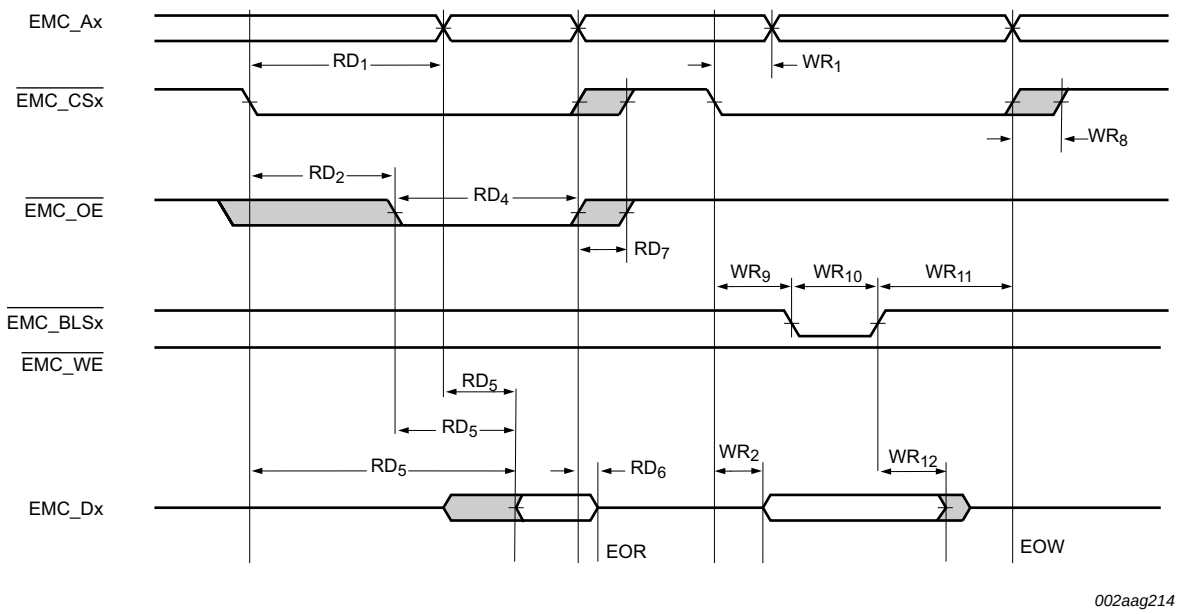


Fig 19. External static memory read/write access (PB = 0)

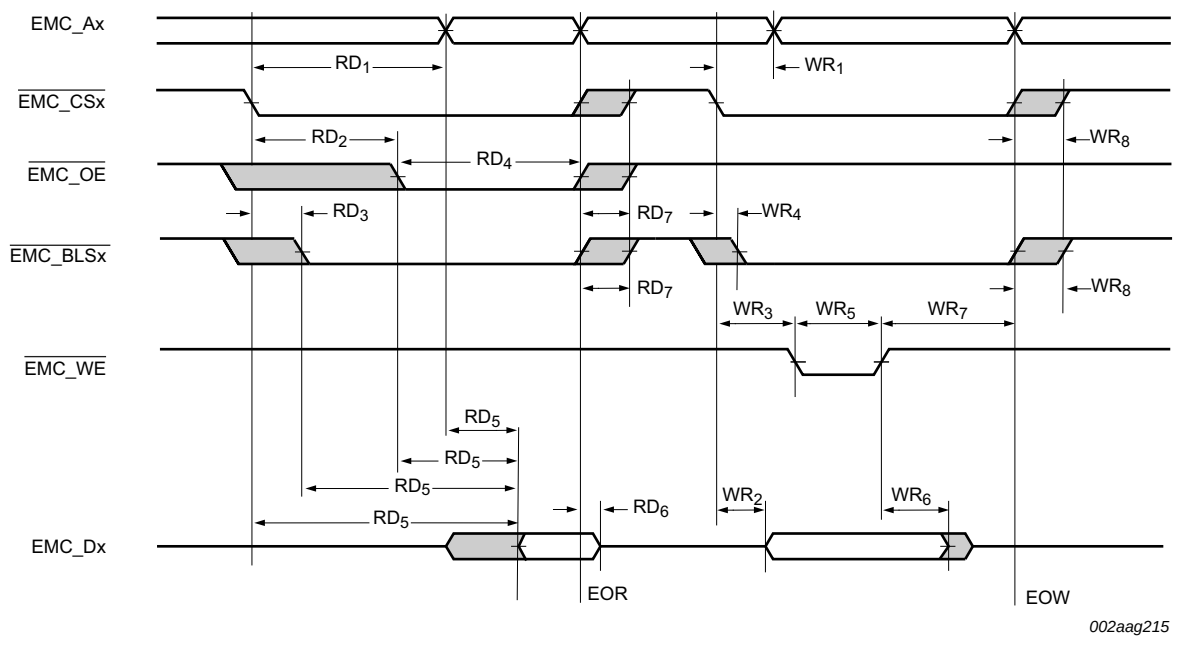


Fig 20. External static memory read/write access (PB =1)

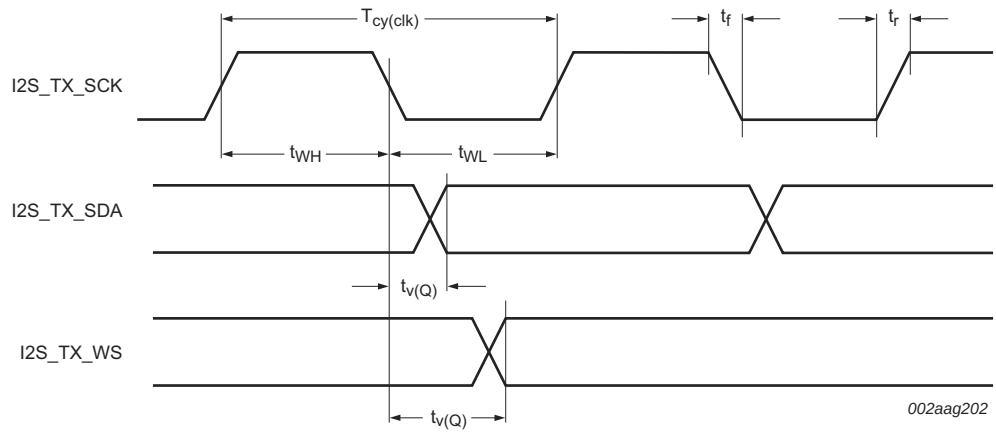


Fig 27. I²S-bus timing (transmit)

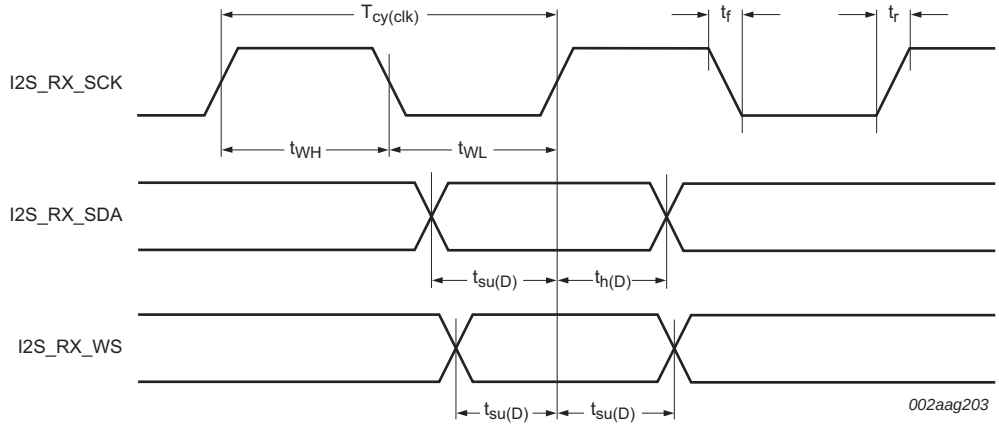


Fig 28. I²S-bus timing (receive)

11.9 LCD

Remark: The LCD controller is available on parts LPC4088.

Table 25. Dynamic characteristics: LCD

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	MHz
$t_{d(QV)}$	data output valid delay time		-	9	ns
$t_{h(Q)}$	data output hold time		−0.5	-	ns

Table 31. Comparator characteristics *…continued*
V_{DDA}= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DV_O	output voltage variation			0	-	V_{DDA}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	–4 to +4.2	-	mV
		V_{IC} = 1.5 V		-	±2	-	mV
		V_{IC} = 2.8 V		-	±2.5		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	µs
t_{PD}	propagation delay	HIGH to LOW; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	122	130	142	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	173	189	233	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	101	108	119	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	114	127	162	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	123	134	143	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	79	91	120	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DDA} = 3.3 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	221	232	254	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	59	63	68	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	183	229	249	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	147	174	213	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	171	192	216	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	235	305	450	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V	[2]	-	5, 10, 20	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +85 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

Table 32. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation (V_{DDA} = 2.6 V; T_{amb} = 85 °C; slow process models).

[2] Settling time applies to switching between comparator and ADC channels.

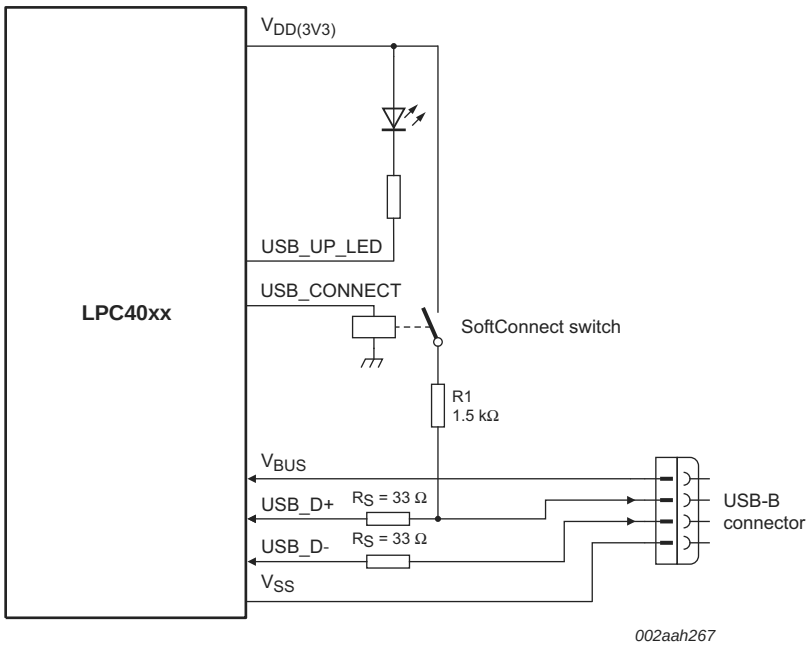


Fig 34. USB interface on a self-powered device

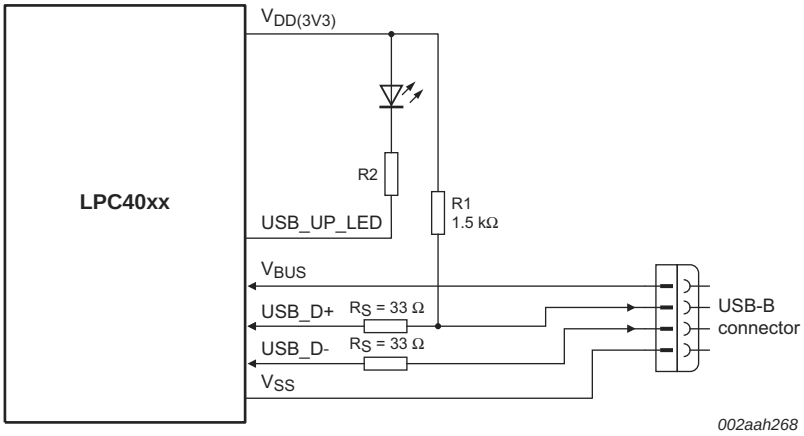
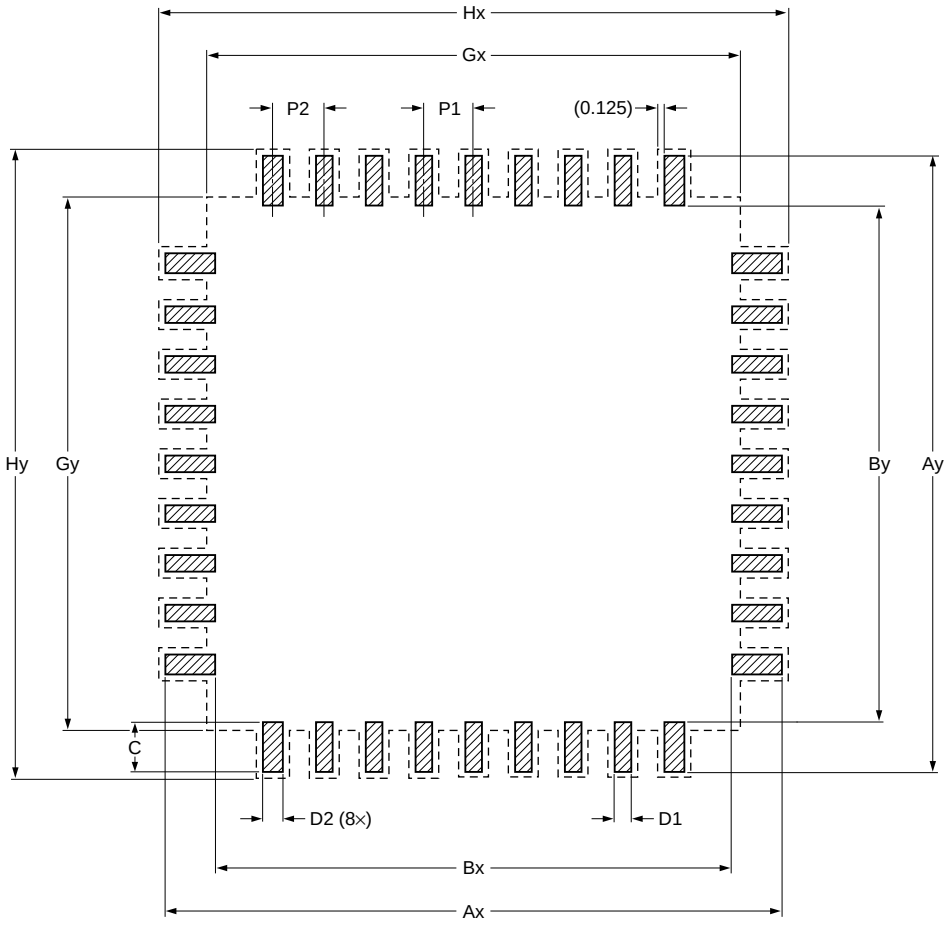


Fig 35. USB interface on a bus-powered device

15. Soldering

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

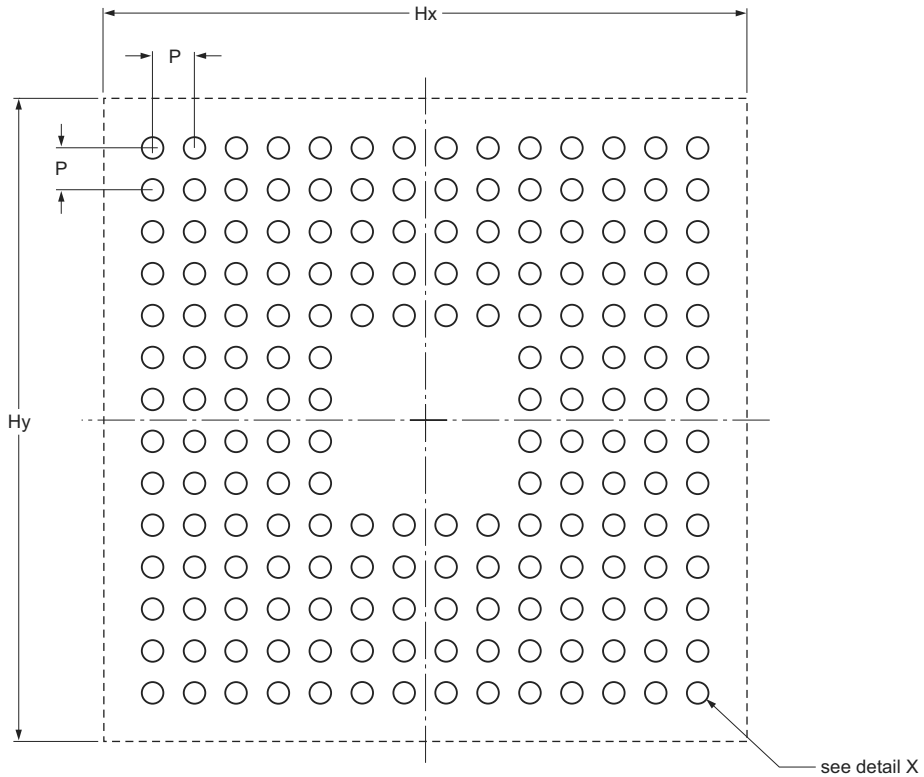
DIMENSIONS in mm

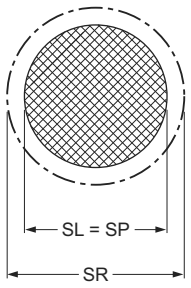
P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 52. Reflow soldering of the LQFP208 package

Footprint information for reflow soldering of TFBGA180 package **SOT570-3**





detail X

solder land (SL)

solder paste deposit (SP)

solder land plus solder paste

solder resist opening (SR)

occupied area

Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.80	0.40	0.40	0.50	12.30	12.30

Issue date ~~14-01-30~~ 15-08-27

Recommend stencil thickness: 0.1 mm

sot570-3_fr

Fig 53. Reflow soldering of the TFBGA180 package