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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4078fbd80-551

6. Pinning information

6.1 Pinning

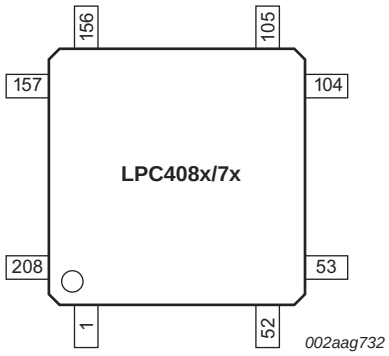


Fig 2. Pin configuration (LQFP208)

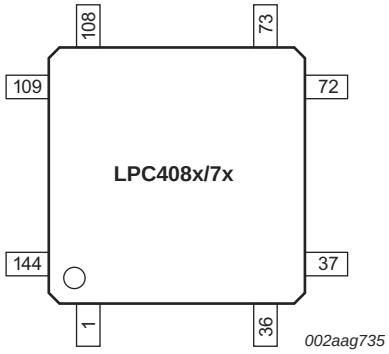


Fig 3. Pin configuration (LQFP144)

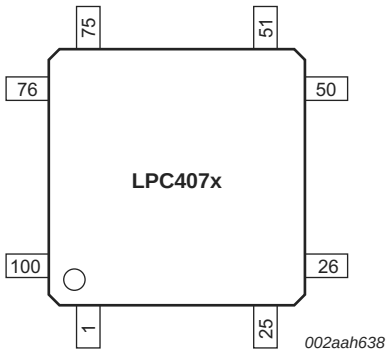


Fig 4. Pin configuration (LQFP100)

Table 3. Pin description

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[0] to P0[31]										I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]	94	U15	M10	66	46	37	J9	[3]	I; PU	I/O	**P0[0] —** General purpose digital input/output pin.
										I	**CAN_RD1 —** CAN1 receiver input.
										O	**U3_TXD —** Transmitter output for UART3.
										I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
										O	**U0_TXD —** Transmitter output for UART0.
P0[1]	96	T14	N11	67	47	38	J10	[3]	I; PU	I/O	**P0[1] —** General purpose digital input/output pin.
										O	**CAN_TD1 —** CAN1 transmitter output.
										I	**U3_RXD —** Receiver input for UART3.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										I	**U0_RXD —** Receiver input for UART0.
P0[2]	202	C4	D5	141	98	79	A2	[3]	I; PU	I/O	**P0[2] —** General purpose digital input/output pin.
										O	**U0_TXD —** Transmitter output for UART0.
										O	**U3_TXD —** Transmitter output for UART3.
P0[3]	204	D6	A3	142	99	80	A1	[3]	I; PU	I/O	**P0[3] —** General purpose digital input/output pin.
										I	**U0_RXD —** Receiver input for UART0.
										I	**U3_RXD —** Receiver input for UART3.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[9]	188	A6	D7	131	91	72	A4	[3]	I; PU	I/O	**P1[9] —** General purpose digital input/output pin.
										I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P1[10]	186	C8	A7	129	90	71	A5	[3]	I; PU	I/O	**P1[10] —** General purpose digital input/output pin.
										I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P1[11]	163	A14	A12	-	-	-	-	[3]	I; PU	I/O	**P1[11] —** General purpose digital input/output pin.
										I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
										I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]	157	A16	A14	-	-	-	-	[3]	I; PU	I/O	**P1[12] —** General purpose digital input/output pin.
										I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
										I/O	**SD_DAT[3] —** Data line 3 for SD card interface.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										-	**R —** Function reserved.
										O	**CMP1_OUT —** Comparator 1, output.
P1[13]	147	D16	D14	-	-	-	-	[3]	I; PU	I/O	**P1[13] —** General purpose digital input/output pin.
										I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[0] to P2[31]										I/O	**Port 2:** Port 2 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block.
P2[0]	154	B17	D12	107	75	60	B10	[3]	I; PU	I/O	**P2[0] —** General purpose digital input/output pin.
										O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
										O	**U1_TXD —** Transmitter output for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_PWR —** LCD panel power enable.
P2[1]	152	E14	C14	106	74	59	B8	[3]	I; PU	I/O	**P2[1] —** General purpose digital input/output pin.
										O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
										I	**U1_RXD —** Receiver input for UART1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_LE —** Line end signal.
P2[2]	150	D15	E11	105	73	58	B9	[3]	I; PU	I/O	**P2[2] —** General purpose digital input/output pin.
										O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
										I	**U1_CTS —** Clear to Send input for UART1.
										O	**T2_MAT3 —** Match output for Timer 2, channel 3.
										-	**R —** Function reserved.
										O	**TRACEDATA[3] —** Trace data, bit 3.
										-	**R —** Function reserved.
										O	**LCD_DCLK —** LCD panel clock.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P3[19]	161	B14	-	-	-	-	-	[3]	I; PU	I/O	**P3[19] —** General purpose digital input/output pin.
										I/O	**EMC_D[19] —** External memory data line 19.
										O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
P3[20]	167	A13	-	-	-	-	-	[3]	I; PU	I/O	**P3[20] —** General purpose digital input/output pin.
										I/O	**EMC_D[20] —** External memory data line 20.
										O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
										I	**U1_DSR —** Data Set Ready input for UART1.
P3[21]	175	C10	-	-	-	-	-	[3]	I; PU	I/O	**P3[21] —** General purpose digital input/output pin.
										I/O	**EMC_D[21] —** External memory data line 21.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
P3[22]	195	C6	-	-	-	-	-	[3]	I; PU	I/O	**P3[22] —** General purpose digital input/output pin.
										I/O	**EMC_D[22] —** External memory data line 22.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										I	**U1_RI —** Ring Indicator input for UART1.
P3[23]	65	T6	M4	45	-	-	-	[3]	I; PU	I/O	**P3[23] —** General purpose digital input/output pin.
										I/O	**EMC_D[23] —** External memory data line 23.
										I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
										I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
P3[24]	58	R5	N3	40	-	-	-	[3]	I; PU	I/O	**P3[24] —** General purpose digital input/output pin.
										I/O	**EMC_D[24] —** External memory data line 24.
										O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
										I	**T0_CAP1 —** Capture input for Timer 0, channel 1.

operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the ARM Cortex-M4 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.15.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.
- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

The I^2S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I^2S connection has one master, which is always the master, and one slave. The I^2S interface on the LPC408x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.26.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I^2S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S input and I^2S output.

7.27 CAN controller and acceptance filters

The LPC408x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.27.1 Features

- Dual-channel CAN controller and bus.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.

- FullCAN messages can generate interrupts.

7.28 General purpose 32-bit timers/external event counters

The LPC408x/7x include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.28.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.29 Pulse Width Modulator (PWM)

The LPC408x/7x contain two standard PWMs.

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC408x/7x. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge

7.36.4.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins and/or the I/O power via the $V_{DD(3V3)}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC408x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.36.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC. This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.36.5 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.36.6 Power domains

The LPC408x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC408x/7x, I/O pads are powered by $V_{DD(3V3)}$, while $V_{DD(REG)(3V3)}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC408x/7x application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly” while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. There is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available and $V_{DD(REG)(3V3)} > V_{BAT}$.

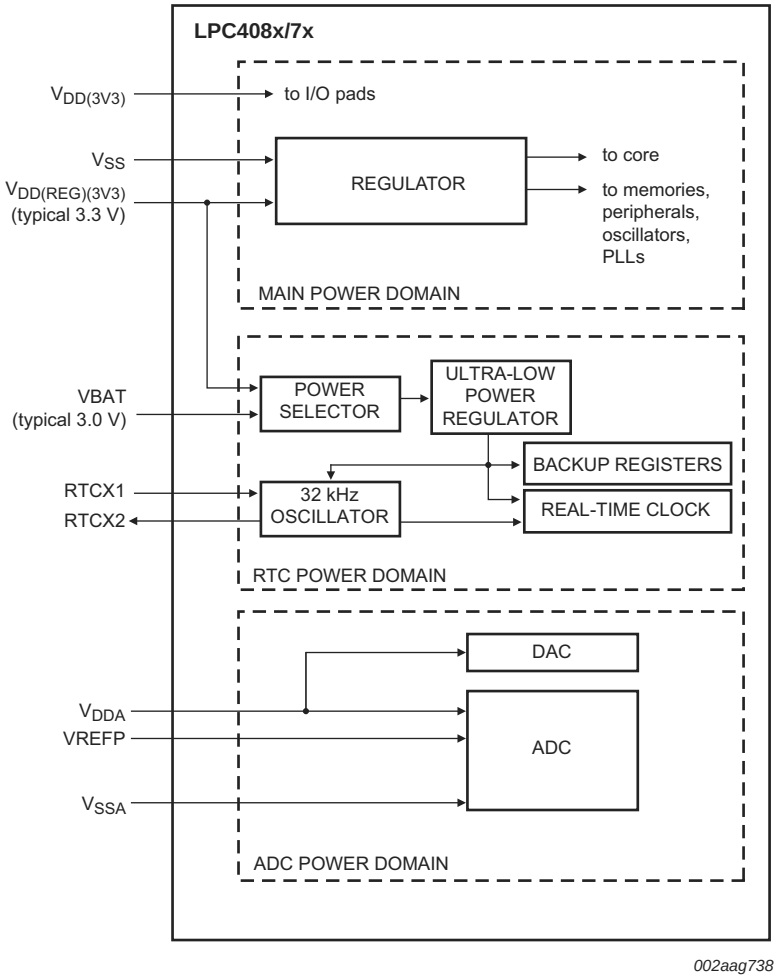


Fig 11. Power distribution

7.37 System control

7.37.1 Reset

Reset has four sources on the LPC408x/7x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, starts the Wake-up timer (see description in Section 7.36.3), causing reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.37.2 Brownout detection

The LPC408x/7x include 2-stage monitoring of the voltage on the $V_{DD(REG)(3V3)}$ pins. If this voltage falls below 2.2 V (typical), the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register.

The second stage of low-voltage detection asserts reset to inactivate the LPC408x/7x when the voltage on the $V_{DD(REG)(3V3)}$ pins falls below 1.85 V (typical). This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the power-on reset circuitry maintains the overall reset.

Both the 2.2 V and 1.85 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.2 V detection to reliably interrupt, or a regularly executed event loop to sense the condition.

7.37.3 Code security (Code Read Protection - CRP)

This feature of the LPC408x/7x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P2[10] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.37.4 APB interface

The APB peripherals are split into two separate APB buses in order to distribute the bus bandwidth and thereby reducing stalls caused by contention between the CPU and the GPDMA controller.

7.37.5 AHB multilayer matrix

The LPC408x/7x use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M4 to the flash memory, the main (32 kB) static RAM, and the Boot ROM. The GPDMA can also access all of these memories. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

7.37.6 External interrupt inputs

The LPC408x/7x include up to 30 edge sensitive interrupt inputs combined with one level sensitive external interrupt input as selectable pin function. The external interrupt input can optionally be used to wake up the processor from Power-down mode.

7.37.7 Memory mapping control

The Cortex-M4 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M4 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC408x/7x is configured for 128 total interrupts.

7.38 Debug control

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail		–0.5	+4.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			–0.5	+4.6	V
V_{DDA}	analog 3.3 V pad supply voltage			–0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		–0.5	+4.6	V

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{CM}	differential common mode voltage range	includes V_{DI} range	[20]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[20]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	[20]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	[20]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[20]	-	-	20	pF
Oscillator pins (see Section 13.2)							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	-	3.6	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD((3V3)}$ ≤ 3.6 V. Guaranteed by design.

[3] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[5] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[6] Boost control bits in the PBOOST register set to 0x0 (see *LPC408x/7x User manual*).

[7] Boost control bits in the PBOOST register set to 0x3 (see *LPC408x/7x User manual*).

[8] IRC running at 12 MHz; main oscillator and PLL disabled; PCLK = CCLK/4.

[9] BOD disabled.

[10] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 0; T_{amb} = 25 °C.

[11] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[12] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[13] V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[14] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[15] Including voltage on outputs in 3-state mode.

[16] $V_{DD(3V3)}$ supply voltages must be present.

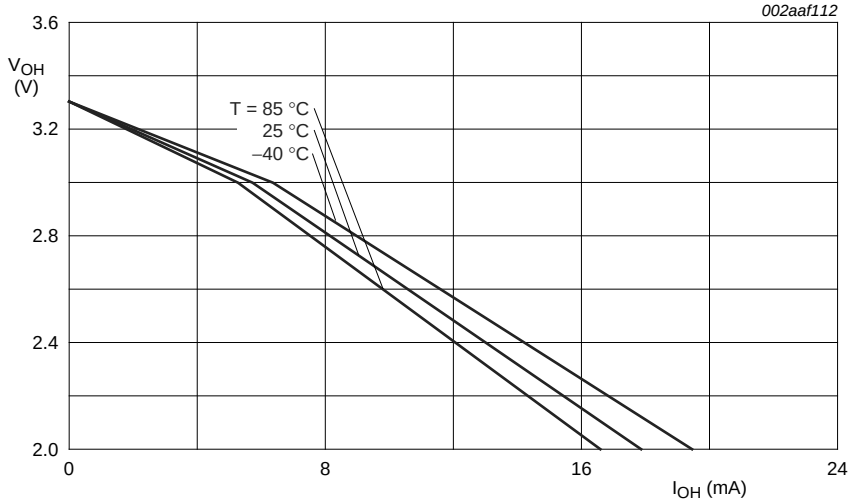
[17] 3-state outputs go into 3-state mode in Deep power-down mode.

[18] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[19] To V_{SS}.

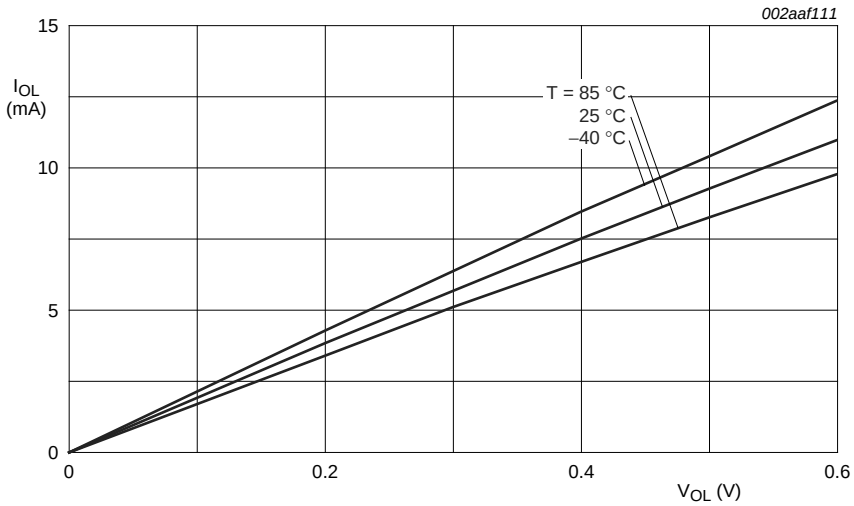
[20] 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

10.3 Electrical pin characteristics



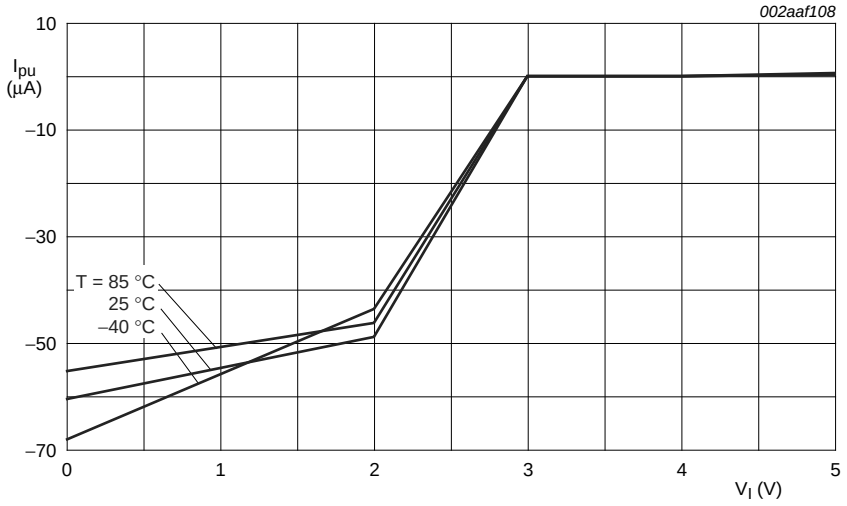
Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 15. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



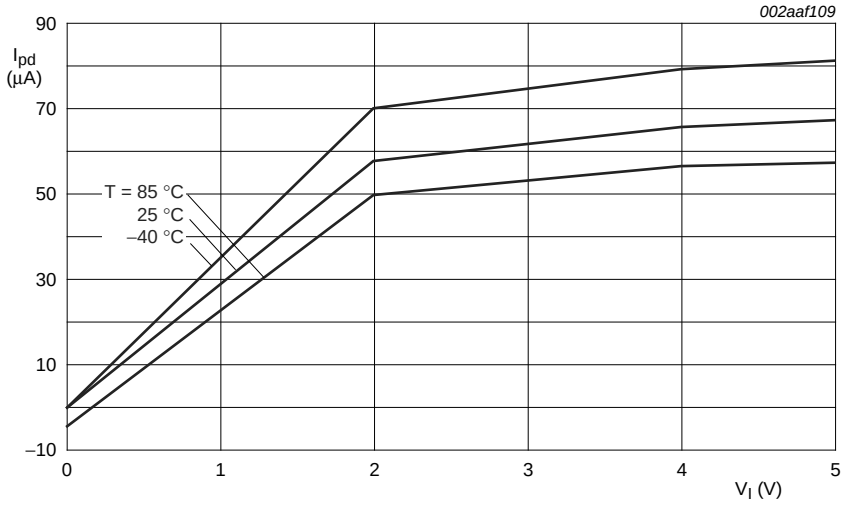
Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 16. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 17. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 18. Typical pull-down current I_{pd} versus input voltage V_I

Table 16. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

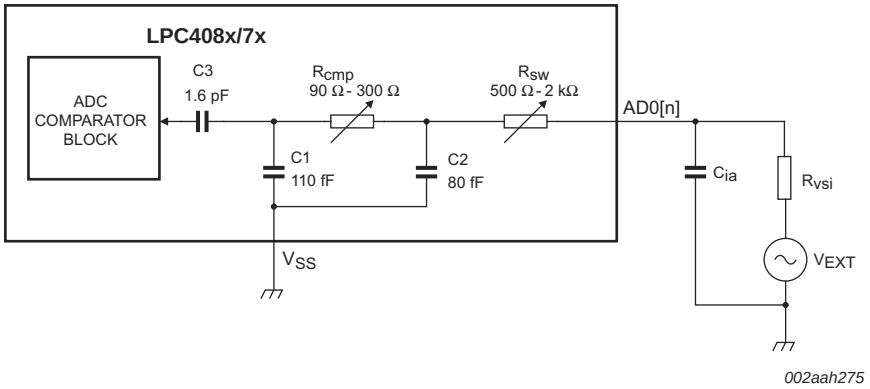
Symbol	Parameter		Min	Typ	Max	Unit
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time	[2]	-	$t_{clkndly}$ + 3.5	$t_{clk0dly}$ + 5.0	ns
$t_{h(S)}$	chip select hold time	[2]	$t_{clkndly}$ - 1.0	$t_{clkndly}$ - 1.2	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.6	$t_{clkndly}$ + 5.0	ns
$t_{h(RAS)}$	row address strobe hold time	[2]	$t_{clkndly}$ - 0.8	$t_{clkndly}$ - 0.9	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.4	$t_{clkndly}$ + 4.9	ns
$t_{h(CAS)}$	column address strobe hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 1.0	-	ns
$t_{d(WV)}$	write valid delay time	[2]	-	$t_{clkndly}$ + 4.1	$t_{clkndly}$ + 6.0	ns
$t_{h(W)}$	write hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 0.7		ns
$t_{d(AV)}$	address valid delay time	[2]	-	$t_{clkndly}$ + 4.6	$t_{clkndly}$ + 6.8	ns
$t_{h(A)}$	address hold time	[2]	$t_{clkndly}$ - 1.1	$t_{clkndly}$ - 1.2	-	ns
Read cycle parameters when EMC_CLKOUT0 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly}	4.5 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly}	-2.9 + t_{fbdly}	-	ns
Read cycle parameters when EMC_CLKOUT1 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	4.5 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-2.9 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time	[2]	-	$t_{clkndly}$+ 5.4	$t_{clkndly}$+ 7.8	ns
$t_{h(Q)}$	data output hold time	[2]	$t_{clkndly}$ − 0.4	$t_{clkndly}$	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] $t_{clkndly}$ represents $t_{clk0dly}$ when EMC_CLKOUT0 clocks SDRAM. $t_{clkndly}$represents $t_{clk1dly}$ when EMC_CLKOUT1 clocks SDRAM.

Table 17. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1 $t_{clk0dly}$ = 0 and $t_{clk1dly}$ = 0						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	t_{cmddly} + 6.8	t_{cmddly} + 10.4	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.2	t_{cmddly} + 2.1	-	ns



The values of resistor components R_{cmp} and R_{sw} vary with temperature and input voltage and are process-dependent.

Fig 33. ADC interface to pins ADC0_IN[n]

Table 29. ADC interface components

Component	Range	Description
R_{cmp}	90 Ω to 300 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
R_{sw}	500 Ω to 2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
C1	110 fF	Parasitic capacitance from the ADC block level.
C2	80 fF	Parasitic capacitance from the ADC block level.
C3	1.6 pF	Sampling capacitor.

12.2 DAC electrical characteristics

Table 30. 10-bit DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
E_D	differential linearity error	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity	-	±1.5	-	LSB
E_O	offset error	-	0.6	-	%
E_G	gain error	-	0.6	-	%
C_L	load capacitance	-	-	200	pF
R_L	load resistance	1	-	-	kΩ

12.3 Comparator electrical characteristics

Table 31. Comparator characteristics

V_{DDA}= 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{DD}	supply current			-	55	-	μA
V_{IC}	common-mode input voltage			0	-	V_{DDA}	V

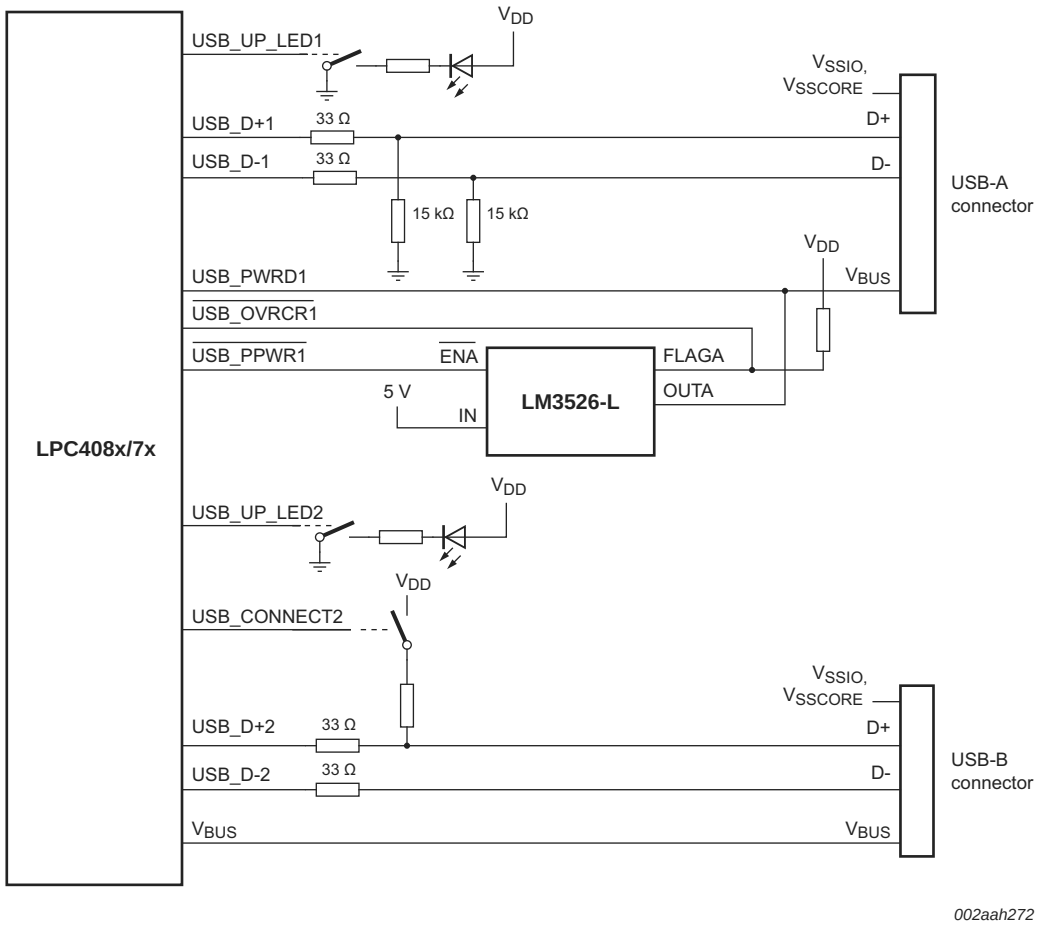


Fig 39. USB device port configuration: port 1 host and port 2 device

13.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

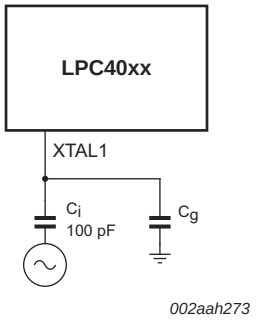


Fig 40. Slave mode operation of the on-chip oscillator

17. References

[1] LPC408x/7x User manual UM10562:
http://www.nxp.com/documents/user_manual/UM10562.pdf

[2] LPC407x/8x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC407X_8X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC408X_7X v.3	20140501	Product data sheet	CIN 201404014I	LPC408X_7X v.2
Modifications:	• Added TFBGA80 to features list. • Added Section 11.11 “SPIFI”. • Table 3: – Added function SSP2_SCK to pin P5[2]. – Added function SSP2_SSEL to pin P5[3]. – Updated pin description of STCLK. – 5 ns glitch filter changed to 10 ns for EINTx pins. – LQFP80 pin 12 changed from P2[30] to DNC. • Table 11: Added Table note 3 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”. • Table 28: Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”. • Section 7.37.2 “Brownout detection”: Updated BOD interrupt and reset values. • Table 15: Added typical specs. • Table 16: – Added typical specs – Removed “All programmable delays EMCDLYCTL are bypassed” from table title. • Table 17: – Added typical specs – Removed “All programmable delays EMCDLYCTL are bypassed” from table title. • Table note 9 added in Table 28 “12-bit ADC characteristics”.			