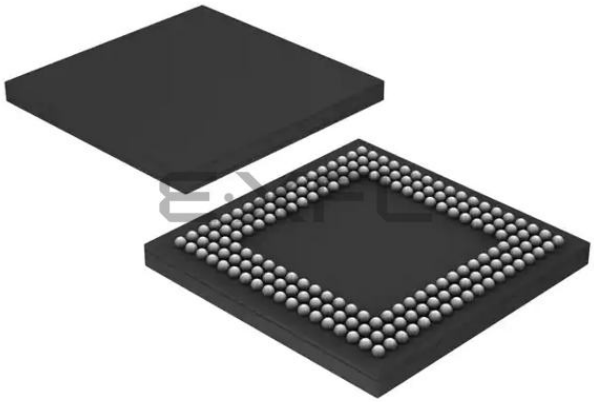

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4078fet180-551

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[13]	45	R2	J5	32	-	-	-	[5]	I; PU	I/O	**P0[13] —** General purpose digital input/output pin.
										O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
										I	**ADC0_IN[7] —** A/D converter 0, input 7. When configured as an ADC input, the digital function of the pin must be disabled.
P0[14]	69	T7	M5	48	-	-	-	[3]	I; PU	I/O	**P0[14] —** General purpose digital input/output pin.
										O	**USB_HSTEN2 —** Host Enabled status for USB port 2.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
P0[15]	128	J16	H13	89	62	47	F9	[3]	I; PU	I/O	**P0[15] —** General purpose digital input/output pin.
										O	**U1_TXD —** Transmitter output for UART1.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[2] —** Data bit 0 for SPIFI.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[20]	120	M17	K14	83	58	-	-	[3]	I; PU	I/O	**P0[20] —** General purpose digital input/output pin.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_CMD —** Command line for SD card interface.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[14] —** LCD data.
P0[21]	118	M16	K11	82	57	-	-	[3]	I; PU	I/O	**P0[21] —** General purpose digital input/output pin.
										I	**U1_RI —** Ring Indicator input for UART1.
										O	**SD_PWR —** Power Supply Enable for external SD card power supply.
										O	**U4_OE —** RS-485/EIA-485 output enable signal for UART4.
										I	**CAN_RD1 —** CAN1 receiver input.
										I/O	**U4_SCLK —** USART 4 clock input or output in synchronous mode.
P0[22]	116	N17	L14	80	56	44	H10	[6]	I; PU	I/O	**P0[22] —** General purpose digital input/output pin.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
										O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
										O	**CAN_TD1 —** CAN1 transmitter output.
										O	**SPIFI_CLK —** Clock output for SPIFI.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[24]	78	T9	P7	54	38	30	J6	[3]	I; PU	I/O	**P1[24] —** General purpose digital input/output pin.
										I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
										O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
										I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
										I	**MC_FB2 —** Motor control PWM channel 2 feedback input.
										I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
										O	**LCD_VD[10] —** LCD data.
										O	**LCD_VD[14] —** LCD data.
P1[25]	80	T10	L7	56	39	31	K6	[3]	I; PU	I/O	**P1[25] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_LS1}}$ —** Low Speed status for USB port 1 (OTG transceiver).
										O	**$\overline{\text{USB\_HSTEN1}}$ —** Host Enabled status for USB port 1.
										O	**T1_MAT1 —** Match output for Timer 1, channel 1.
										O	**MC_1A —** Motor control PWM channel 1, output A.
										O	**CLKOUT —** Selectable clock output.
										O	**LCD_VD[11] —** LCD data.
										O	**LCD_VD[15] —** LCD data.
P1[26]	82	R10	P8	57	40	32	H6	[3]	I; PU	I/O	**P1[26] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_SSPND1}}$ —** USB port 1 Bus Suspend status (OTG transceiver).
										O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
										I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
										O	**MC_1B —** Motor control PWM channel 1, output B.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**LCD_VD[12] —** LCD data.
										O	**LCD_VD[20] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P4[7]	121	L16	K12	84	-	-	-	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
										I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	-	-	-	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
										I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	-	-	-	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
										I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	-	-	-	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
										I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	-	-	-	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
										I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	-	-	-	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
										I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	-	-	-	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
										I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	-	-	-	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
										I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	-	-	-	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
										I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	-	-	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
										I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	-	-	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
										I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	-	-	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
										I/O	**EMC_A[18] —** External memory address line 18.
P4[19]	111	P16	M14	-	-	-	-	[3]	I; PU	I/O	**P4[19] —** General purpose digital input/output pin.
										I/O	**EMC_A[19] —** External memory address line 19.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P5[0] to P5[4]										I/O	**Port 5:** Port 5 is a 5-bit I/O port with individual direction controls for each bit. The operation of port 5 pins depends upon the pin function selected via the pin connect block.
P5[0]	9	F4	E5	6	-	-	-	[3]	I; PU	I/O	**P5[0] —** General purpose digital input/output pin.
										I/O	**EMC_A[24] —** External memory address line 24.
										I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
										O	**T2_MAT2 —** Match output for Timer 2, channel 2.
P5[1]	30	J4	H1	21	-	-	G1	[3]	I; PU	I/O	**P5[1] —** General purpose digital input/output pin.
										I/O	**EMC_A[25] —** External memory address line 25.
										I/O	**SSP2_MISO —** Master In Slave Out for SSP2.
										O	**T2_MAT3 —** Match output for Timer 2, channel 3.
P5[2]	117	L14	L12	81	-	-	-	[11]	I	I/O	**P5[2] —** General purpose digital input/output pin.
										-	**R —** Function reserved.
										I/O	**SSP2_SCK —** Serial clock for SSP2. When using this pin, the SSP2 bit rate is limited to 1 MHz.
										O	**T3_MAT2 —** Match output for Timer 3, channel 2.
										-	**R —** Function reserved.
										I/O	**I2C0_SDA —** I^2C0 data input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).
P5[3]	141	G14	G10	98	-	-	-	[11]	I	I/O	**P5[3] —** General purpose digital input/output pin.
										-	**R —** Function reserved.
										I/O	**SSP2_SSEL —** Slave select for SSP2. When using this pin, the SSP2 bit rate is limited to 1 MHz.
										-	**R —** Function reserved.
										I	**U4_RXD —** Receiver input for USART4.
										I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus.

7.14 LCD controller

Remark: The LCD controller is available on parts LPC4088.

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.14.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.15 Ethernet

Remark: The Ethernet block is available on parts LPC4088/78/76.

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex

- Buffered output.
- Power-down mode.
- Selectable output drive.
- Dedicated conversion timer.
- DMA support.

7.21 Comparator

Remark: The comparator is available on parts LPC4088/7876.

Two embedded comparators are available to compare the voltage levels on external pins or against internal voltages. Up to four voltages on external pins and several internal reference voltages are selectable on each comparator. Additionally, two of the external inputs can be selected to drive an input common on both comparators.

7.21.1 Features

- Up to five selectable external sources per comparator; fully configurable on either positive or negative comparator input channels.
- 0.9 V internal band gap reference voltage selectable as either positive or negative input on each comparator.
- 32-stage voltage ladder internal reference for selectable voltages on each comparator; configurable on either positive or negative comparator input.
- Voltage ladder source voltage is selectable from an external pin or the 3.3 V analog voltage supply.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Relaxation oscillator circuitry output, for a 555 style timer operation.
- Individual comparator outputs can be connected to I/O pins.
- Separate interrupt for each comparator.
- Edge and level comparator outputs connect to two timers allowing edge counting while a level match has been asserted or measuring the time between two voltage trip points.

7.22 UART0/1/2/3 and USART4

Remark: UART0/1/2/3 are available on all parts. USART4 is available on parts LPC4088/78/76.

The LPC408x/7x contain five UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.22.1 Features

- Maximum UART data bit rate of 7.5 MBit/s.

7.36.1.3 RTC oscillator

The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be output on the CLKOUT pin in order to allow trimming the RTC oscillator without interference from a probe.

7.36.1.4 Watchdog oscillator

The Watchdog Timer has a dedicated oscillator that provides a 500 kHz clock to the Watchdog Timer that is always running if the Watchdog Timer is enabled. The Watchdog oscillator clock can be output on the CLKOUT pin in order to allow observe its frequency.

In order to allow Watchdog Timer operation with minimum power consumption, which can be important in reduced power modes, the Watchdog oscillator frequency is not tightly controlled. The Watchdog oscillator frequency will vary over temperature and power supply within a particular part, and may vary by processing across different parts. This variation should be taken into account when determining Watchdog reload values.

Within a particular part, temperature and power supply variations can produce up to a ±17 % frequency variation. Frequency variation between devices under the same operating conditions can be up to ±30 %.

7.36.2 Main PLL (PLL0) and Alternate PLL (PLL1)

PLL0 (also called the Main PLL) and PLL1 (also called the Alternate PLL) are functionally identical but have somewhat different input possibilities and output connections. These possibilities are shown in Figure 10. The Main PLL can receive its input from either the IRC or the main oscillator and can potentially be used to provide the clocks to nearly everything on the device. The Alternate PLL receives its input only from the main oscillator and is intended to be used as an alternate source of clocking to the USB. The USB has timing needs that may not always be filled by the Main PLL.

Both PLLs are disabled and powered off on reset. If the Alternate PLL is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz to the USB clock through that route. The source for each clock must be selected via the CLKSEL registers and can be further reduced by clock dividers as needed.

PLL0 accepts an input clock frequency from either the IRC or the main oscillator. If only the Main PLL is used, then its output frequency must be an integer multiple of all other clocks needed in the system. PLL1 takes its input only from the main oscillator, requiring an external crystal in the range of 10 to 25 MHz. In each PLL, the Current Controlled Oscillator (CCO) operates in the range of 156 MHz to 320 MHz, so there are additional dividers to bring the output down to the desired frequencies. The minimum output divider value is 2, insuring that the output of the PLLs have a 50 % duty cycle.

If the USB is used, the possibilities for the CPU clock and other clocks will be limited by the requirements that the frequency be precise and very low jitter, and that the PLL0 output must be a multiple of 48 MHz. Even multiples of 48 MHz that are within the operating range of the PLL are 192 MHz and 288 MHz. Also, only the main oscillator in conjunction with the PLL can meet the precision and jitter specifications for USB. It is due to these limitations that the Alternate PLL is provided.

The alternate PLL accepts an input clock frequency from the main oscillator in the range of 10 MHz to 25 MHz only. When used as the USB clock, the input frequency is multiplied up to a multiple of 48 MHz (192 MHz or 288 MHz as described above).

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly” while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. There is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available and $V_{DD(REG)(3V3)} > V_{BAT}$.

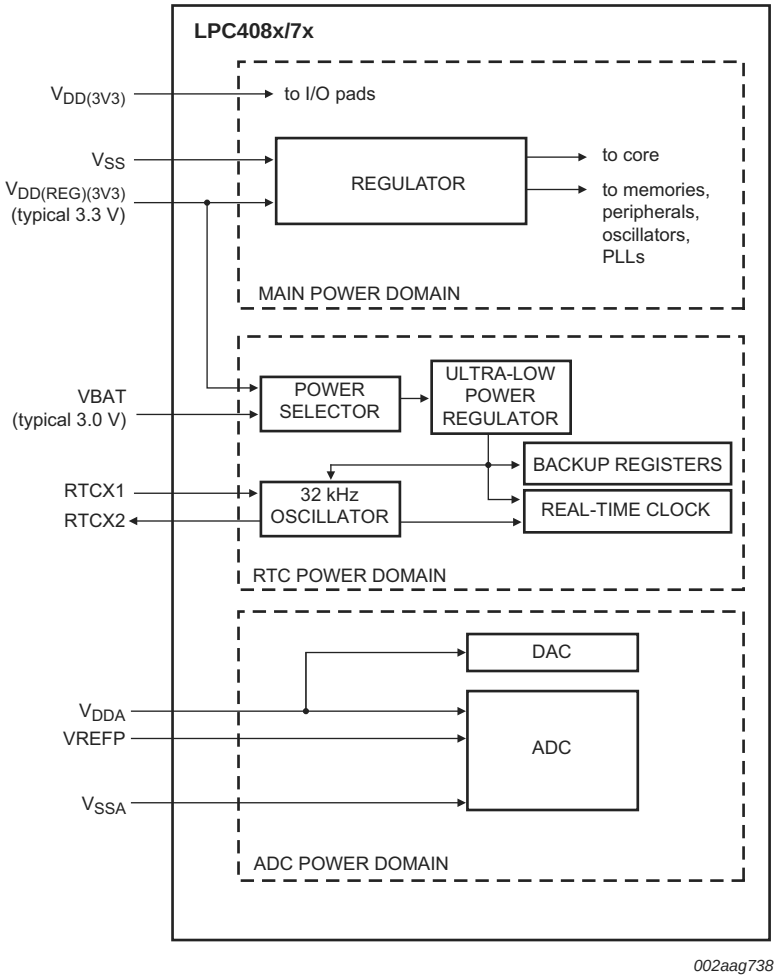


Fig 11. Power distribution

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3]	2.7	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[4]	2.1	3.0	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.7	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]	-	7.5	-	mA
		CCLK = 120 MHz; PLL enabled	[5][7]	-	56	-	mA
		active mode; code `while(1){}` executed from flash; all peripherals enabled; PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]		14	-	-
		CCLK = 120 MHz; PLL enabled	[5][7]		120	-	mA
		Sleep mode	[5][8]	-	5.5	-	mA
		Deep-sleep mode	[5][9]	-	550	1200	µA
		Power-down mode	[5][9]	-	280	600	µA
I_{BAT}	battery supply current	RTC running; part powered down; $V_{DD(REG)(3V3)}$ =0 V; $V_{i(VBAT)}$ = 3.0 V; $V_{DD(3V3)}$ = 0 V.	[10]	-	1	9	µA
		part powered; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.0 V	[11]		<10		nA

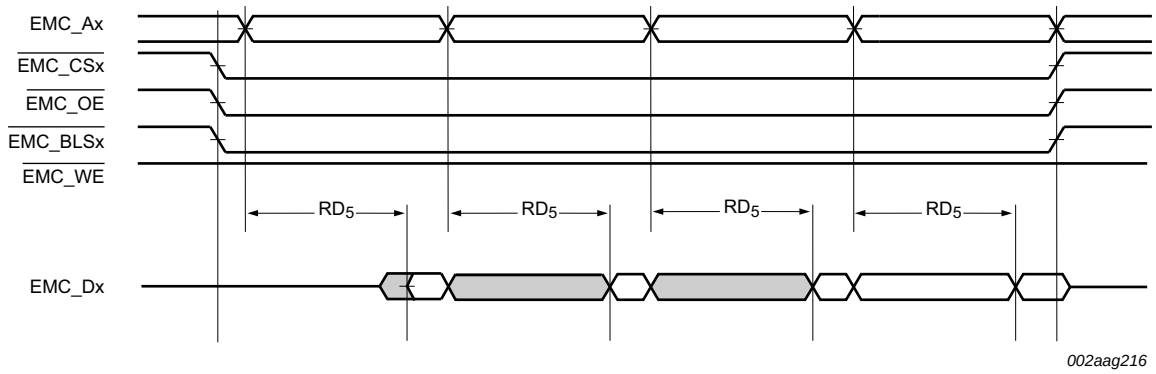


Fig 21. External static memory burst read cycle

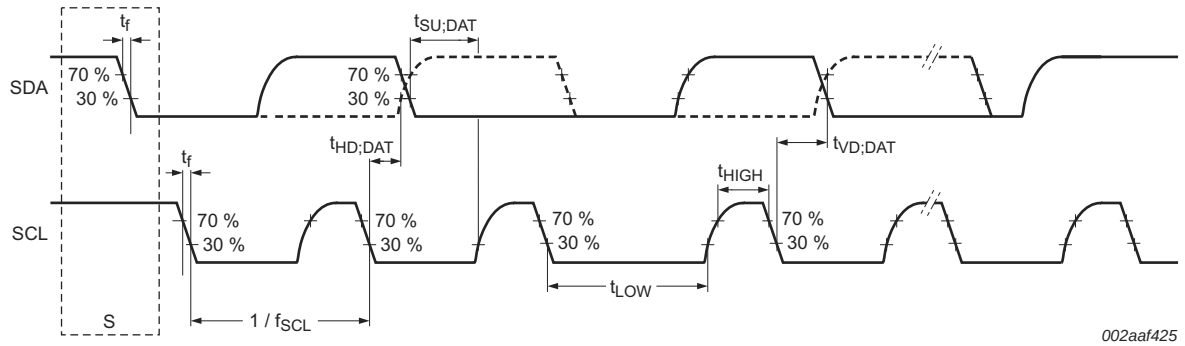


Fig 26. I²C-bus pins clock timing

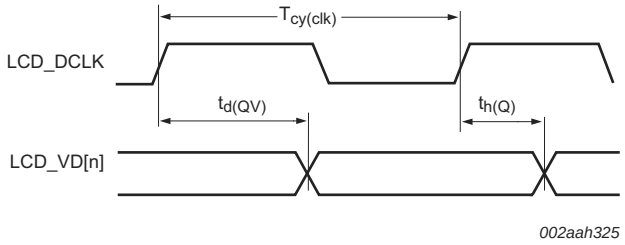
11.8 I²S-bus interface

Table 24. Dynamic characteristics: I²S-bus interface pins

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
common to input and output						
t_r	rise time		[1]	-	6.7	ns
t_f	fall time		[1]	-	8.0	ns
t_{WH}	pulse width HIGH	on pins I2S_TX_SCK and I2S_RX_SCK	[1]	25	-	-
t_{WL}	pulse width LOW	on pins I2S_TX_SCK and I2S_RX_SCK	[1]	-	25	ns
output						
$t_{v(Q)}$	data output valid time	on pin I2S_TX_SDA;	[1]	-	6	ns
input						
$t_{su(D)}$	data input set-up time	on pin I2S_RX_SDA	[1]	5	-	ns
$t_{h(D)}$	data input hold time	on pin I2S_RX_SDA	[1]	2	-	ns

[1] CCLK = 100 MHz; peripheral clock to the I²S-bus interface PCLK = CCLK / 4. I²S clock cycle time $T_{cy(clk)}$ = 1600 ns, corresponds to the SCK signal in the *I²S-bus specification*.



The LCD panel clock is shown with the default polarity. The clock can be inverted via the IPC bit in the LCD_POL register. Typically, the LCD panel uses the falling edge of the LCD_DCLK to sample the data.

Fig 29. LCD timing

11.10 SD/MMC

Remark: The SD/MMC card interface is available on parts LPC4088/78/76.

Table 26. Dynamic characteristics: SD/MMC

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	25	MHz
		on pin SD_CLK; identification mode		25	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DAT[3:0] as outputs	-	23	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DAT[3:0] as outputs	3.5	-	ns

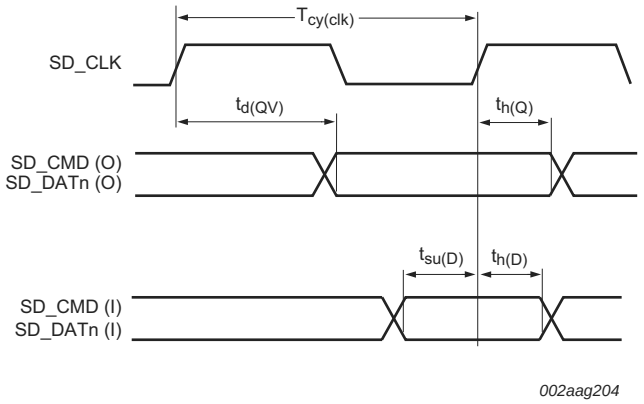


Fig 30. SD/MMC timing

Table 33. Comparator voltage ladder reference static characteristics
V_{DDA} = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal V_{DDA} supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		–0.45	–0.5	–0.55	%
		decimal code = 16		–0.99	–1.1	–1.21	%
		decimal code = 24		–1.26	–1.4	–1.54	%
		decimal code = 30		–1.35	–1.5	–1.65	%
		decimal code = 31		–1.35	–1.5	–1.65	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		0.44	0.4	0.36	%
		decimal code = 16		–0.18	–0.2	–0.22	%
		decimal code = 24		–0.45	–0.5	–0.55	%
		decimal code = 30		–0.54	–0.6	–0.66	%
		decimal code = 31		–0.45	–0.5	–0.55	%

[1] Measured on typical silicon samples with a 2 kHz input signal and overdrive < 100 μV. Power switched off to all analog peripherals except the comparator.

13. Application information

13.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC4088 and LPC4078/76 and as device-only controller on parts LPC4074/72.

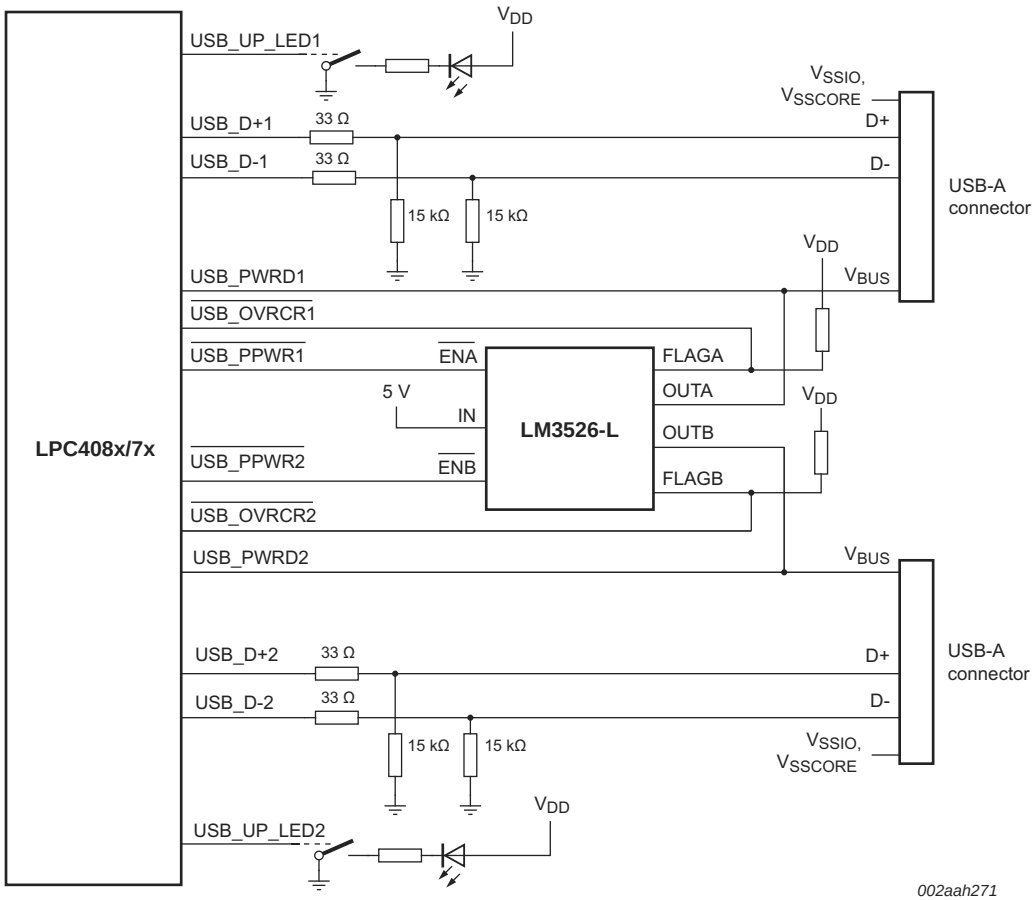
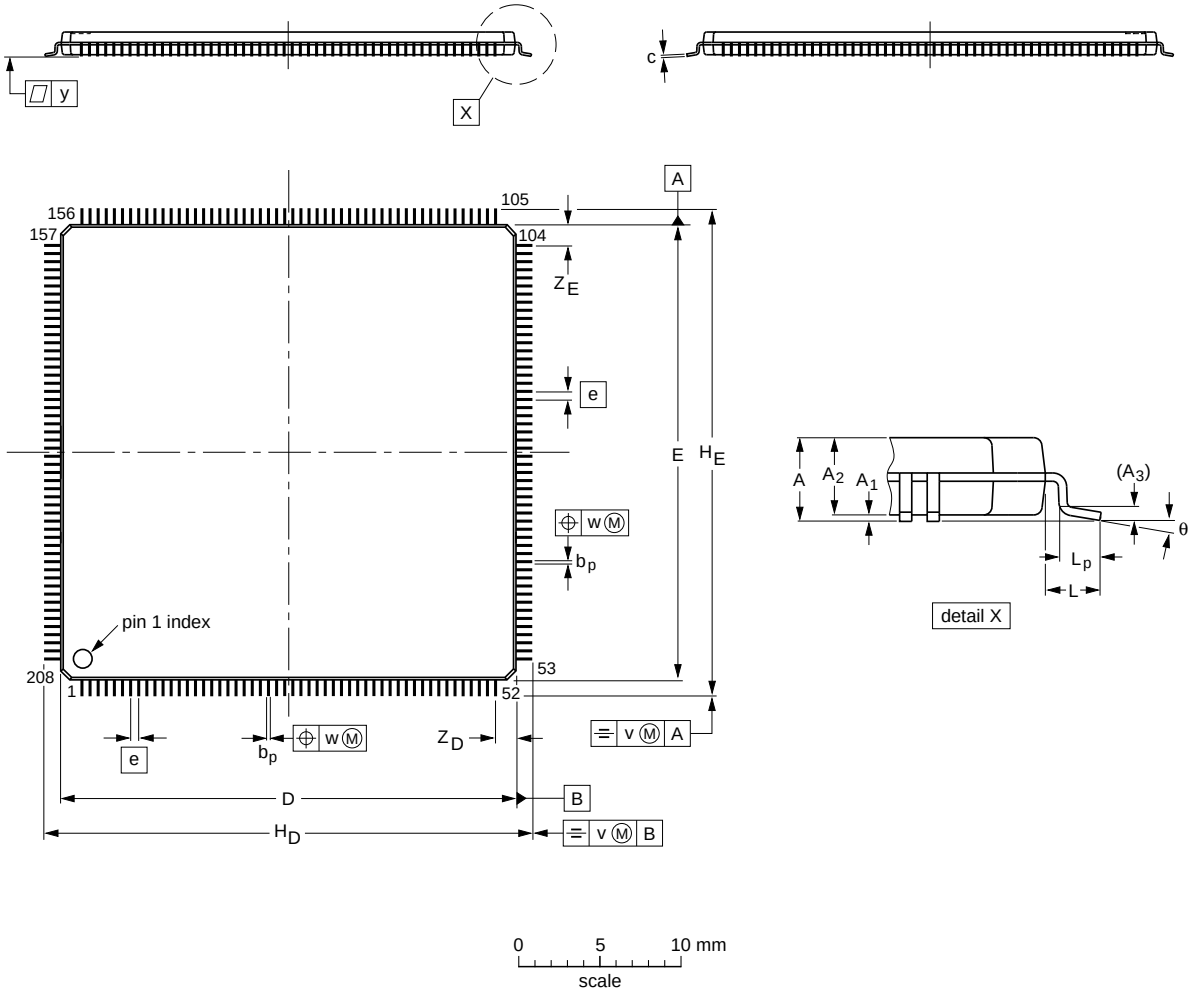


Fig 38. USB host port configuration: port 1 and port 2 as hosts

14. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

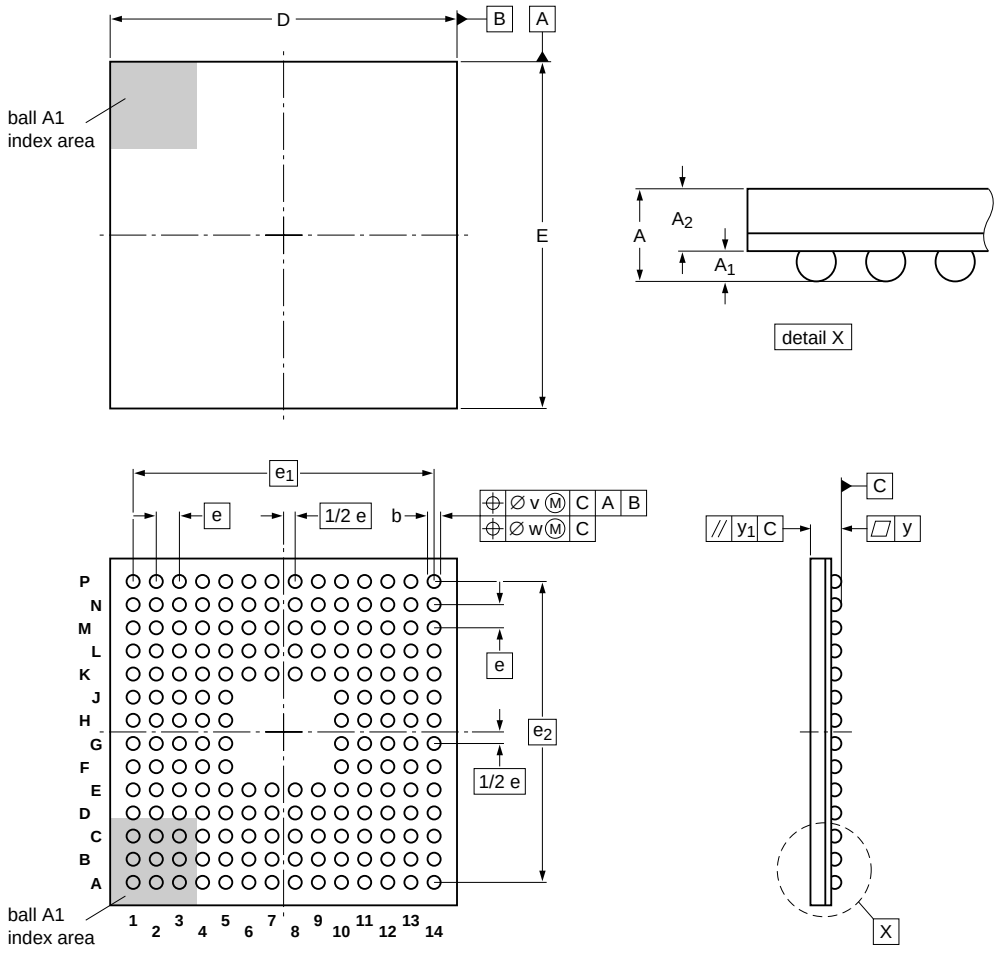
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 45. Package outline SOT459-1 (LQFP208)

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

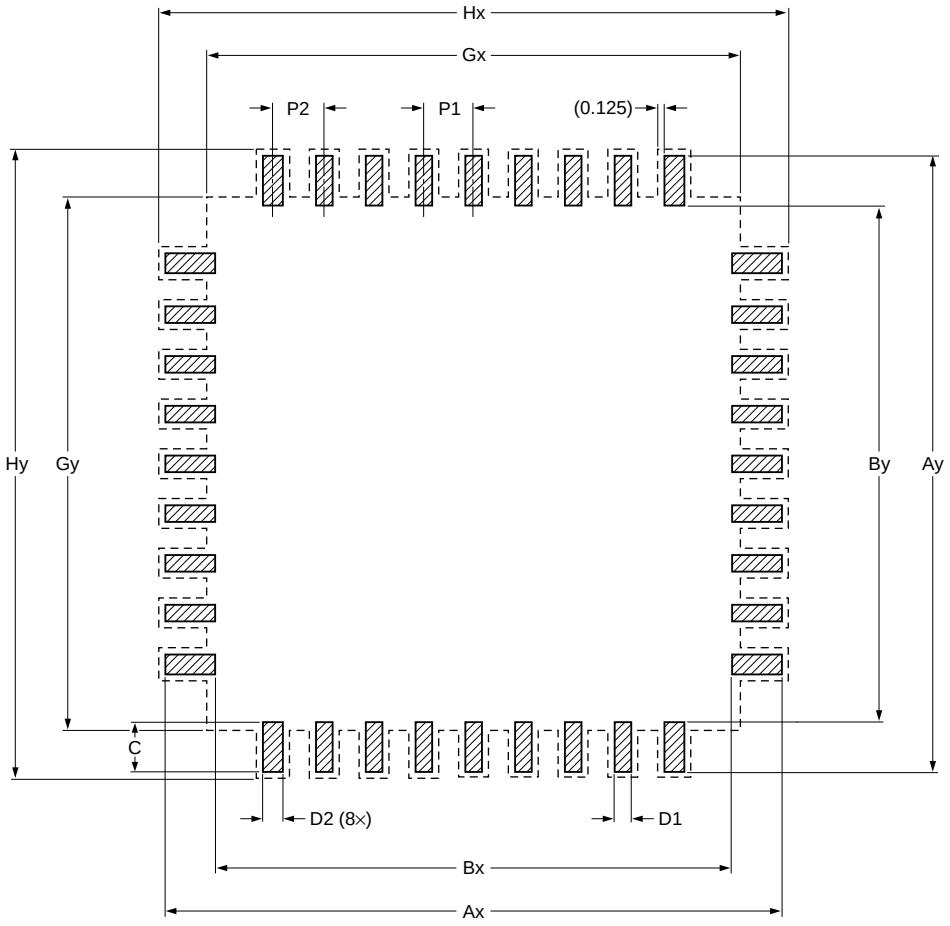
UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 47. Package outline SOT570-3 (TFBGA180)

15. Soldering

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 52. Reflow soldering of the LQFP208 package

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC408X_7X v.3	20140501	Product data sheet	CIN 201404014I	LPC408X_7X v.2
Modifications:	• Added TFBGA80 to features list. • Added Section 11.11 “SPIFI”. • Table 3: – Added function SSP2_SCK to pin P5[2]. – Added function SSP2_SSEL to pin P5[3]. – Updated pin description of STCLK. – 5 ns glitch filter changed to 10 ns for EINTx pins. – LQFP80 pin 12 changed from P2[30] to DNC. • Table 11: Added Table note 3 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”. • Table 28: Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”. • Section 7.37.2 “Brownout detection”: Updated BOD interrupt and reset values. • Table 15: Added typical specs. • Table 16: – Added typical specs – Removed “All programmable delays EMCDLYCTL are bypassed” from table title. • Table 17: – Added typical specs – Removed “All programmable delays EMCDLYCTL are bypassed” from table title. • Table note 9 added in Table 28 “12-bit ADC characteristics”.			

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC408X_7X v.2	20130703	Product data sheet	-	LPC408X_7X v.1.1
	• Added LQFP100 and TFBGA80. • Table 3: – Removed overbar from NMI. – Added minimum reset pulse width of 50 ns to $\overline{\text{RESET}}$ pin. – Updated Table note 14 for RTCX pins (32 kHz crystal must be used to operate RTC). – Added boundary scan information to description for $\overline{\text{RESET}}$ pin. • Table 11: – Updated typ numbers for $I_{DD(REG)(3V3)}$ and I_{BAT}. – Added max values for deep sleep, power down, and deep PD for I_{BAT}. • Table 15, Table note 3: Changed $T_{cy(clk)}$ = 1/CCLK to $T_{cy(clk)}$ = 1/EMC_CLK. • Table 21: Removed reference to $\overline{\text{RESET}}$ pin from Table note 1. • Table 22: – Removed $T_{cy(PCLK)}$ spec; already given by the maximum chip frequency. – Changed min clock cycle time for SSP slave from 120 to 100. – Updated Table note 1 and Table note 3. • Section 7.24.1 “Features”: Changed max speed for SSP master from 60 to 33. • Updated EMC timing specs to C_L = 30 pF in Table 15, Table 16, Table 17, and Table 18. • SOT570-2 obsolete; replaced with SOT570-3.			
LPC408X_7X v.1.1	20121114	Product data sheet	-	LPC408X_7X v.1
Modifications:	• Changed data sheet status to Product.			
LPC408X_7X v.1	20120917	Objective data sheet	-	-