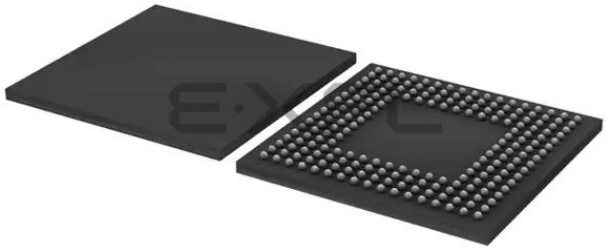

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4078fet208-551

- 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support.
- Two analog comparators.

- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
  - Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
  - Brownout detect with separate threshold for interrupt and forced reset.
  - On-chip Power-On Reset (POR).
- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1 % accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, LQFP144, TFBGA80, and LQFP80 package.

3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

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4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC4088			
LPC4088FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4088FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1
LPC4088FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4088FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4078			
LPC4078FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4078FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1
LPC4078FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4078FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4078FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC4078FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC4076			
LPC4076FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4076FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4074			
LPC4074FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4074FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC4072			
LPC4072FET80	TFBGA80	plastic thin fine-pitch ball grid array package; 80 balls	SOT1328-1
LPC4072FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)	EEPROM (B)	EMC bus width (bit)	LCD	Ethernet	USB	CAN	UART	QEI	SD/MMC	Comparator	FPU	Package
LPC4088														
LPC4088FBD208	512	96	4032	32	yes	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP208
LPC4088FET208	512	96	4032	32	yes	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA208
LPC4088FET180	512	96	4032	16	yes	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180
LPC4088FBD144	512	96	4032	8	yes	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4078														
LPC4078FBD208	512	96	4032	32	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP208
LPC4078FET208	512	96	4032	32	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA208
LPC4078FET180	512	96	4032	16	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	77	62	A10	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
										I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
										O	**T2_MAT2 —** Match output for Timer 2, channel 2.
										I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
										I	**CMP1_IN[3] —** Comparator 1, input 3.
										-	**R —** Function reserved.
										O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	76	61	A9	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
										I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
										O	**T2_MAT3 —** Match output for Timer 2, channel 3.
										I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
										I	**CMP1_IN[2] —** Comparator 1, input 2.
										-	**R —** Function reserved.
										O	**LCD_VD[17] —** LCD data.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[16]	130	J14	H14	90	63	48	F8	[3]	I; PU	I/O	**P0[16] —** General purpose digital input/output pin.
										I	**U1_RXD —** Receiver input for UART1.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[3] —** Data bit 0 for SPIFI.
P0[17]	126	K17	J12	87	61	46	F10	[3]	I; PU	I/O	**P0[17] —** General purpose digital input/output pin.
										I	**U1_CTS —** Clear to Send input for UART1.
										I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[1] —** Data bit 0 for SPIFI.
P0[18]	124	K15	J13	86	60	45	G10	[3]	I; PU	I/O	**P0[18] —** General purpose digital input/output pin.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
										I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[0] —** Data bit 0 for SPIFI.
P0[19]	122	L17	J10	85	59	-	-	[3]	I; PU	I/O	**P0[19] —** General purpose digital input/output pin.
										I	**U1_DSR —** Data Set Ready input for UART1.
										O	**SD_CLK —** Clock output line for SD card interface.
										I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[13] —** LCD data.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[27]	88	T12	M9	61	43	-	-	[3]	I; PU	I/O	**P1[27] —** General purpose digital input/output pin.
										I	**$\overline{\text{USB\_INT1}}$ —** USB port 1 OTG transceiver interrupt (OTG transceiver).
										I	**$\overline{\text{USB\_OVRCR1}}$ —** USB port 1 Over-Current status.
										I	**T0_CAP1 —** Capture input for Timer 0, channel 1.
										O	**CLKOUT —** Selectable clock output.
										-	**R —** Function reserved.
										O	**LCD_VD[13] —** LCD data.
										O	**LCD_VD[21] —** LCD data.
P1[28]	90	T13	P10	63	44	35	J8	[3]	I; PU	I/O	**P1[28] —** General purpose digital input/output pin.
										I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).
										I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
										O	**T0_MAT0 —** Match output for Timer 0, channel 0.
										O	**MC_2A —** Motor control PWM channel 2, output A.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										O	**LCD_VD[14] —** LCD data.
										O	**LCD_VD[22] —** LCD data.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[24]	53	P5	P1	-	-	-	-	[3]	I; PU	I/O	**P2[24] —** General purpose digital input/output pin.
										O	**EMC_CKE0 —** SDRAM clock enable 0.
P2[25]	54	R4	P2	-	-	-	-	[3]	I; PU	I/O	**P2[25] —** General purpose digital input/output pin.
										O	**EMC_CKE1 —** SDRAM clock enable 1.
P2[26]	57	T4	-	-	-	-	-	[3]	I; PU	I/O	**P2[26] —** General purpose digital input/output pin.
										O	**EMC_CKE2 —** SDRAM clock enable 2.
										I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P2[27]	47	P3	-	-	-	-	-	[3]	I; PU	I/O	**P2[27] —** General purpose digital input/output pin.
										O	**EMC_CKE3 —** SDRAM clock enable 3.
										I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
										O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P2[28]	49	P4	M2	-	-	-	-	[3]	I; PU	I/O	**P2[28] —** General purpose digital input/output pin.
										O	**EMC_DQM0 —** Data mask 0 used with SDRAM and static devices.
P2[29]	43	N3	L1	-	-	-	-	[3]	I; PU	I/O	**P2[29] —** General purpose digital input/output pin.
										O	**EMC_DQM1 —** Data mask 1 used with SDRAM and static devices.
P2[30]	31	L4	-	-	-	-	-	[3]	I; PU	I/O	**P2[30] —** General purpose digital input/output pin.
										O	**EMC_DQM2 —** Data mask 2 used with SDRAM and static devices.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT2 —** Match output for Timer 3, channel 2.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
V_{SS}	33, 63, 77, 93, 114, 133, 148, 169, 189, 200	L3, T5, R9, P12, N16, H14, E15, A12, B6, A2	H4, P4, L9, L13, G13, D13, C11, B4	44, 65, 79, 103, 117, 139	31, 55, 72, 97	24, 43, 57, 78	H4, G8, G9, B3			G	Ground: 0 V reference for digital IO pins.
V_{SSREG}	32, 84, 172	D12, K4, P10	H3, L8, A10	22, 59, 119	15, 41, 83	33, 66	J7, F3			G	Ground: 0 V reference for internal logic.
V_{SSA}	22	J2	F3	15	11	9	E2			G	Analog ground: 0 V power supply and reference for the ADC and DAC. This should be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
XTAL1	44	M4	L2	31	22	19	J1	[14] [16]		I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	46	N4	K4	33	23	20	K1	[14] [16]		O	Output from the oscillator amplifier.
DNC	-	-	-	-	-	12	-				Do not connect.

[1] PU = internal pull-up enabled (for $V_{DD(REG)(3V3)}$ = 3.3 V, pulled up to 3.3 V); IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] I = Input; O = Output; G = Ground; S = Supply.

[3] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[4] 5 V tolerant standard pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis. This pad can be powered by VBAT.

[5] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and analog input. When configured as a ADC input, digital section of the pad is disabled.

[6] 5 V tolerant fast pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis.

[7] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[8] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

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Table 4. LPC408x/7x memory usage and details

Address range	General Use	Address range details and description	
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 to 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)
		0x9000 0000 to 0x93FF FFFF	Static memory chip select 1 (up to 64 MB)
		0x9800 0000 to 0x9BFF FFFF	Static memory chip select 2 (up to 64 MB)
		0x9C00 0000 to 0x9FFF FFFF	Static memory chip select 3 (up to 64 MB)
		Four dynamic memory chip selects:	
		0xA000 0000 to 0xAFFF FFFF	Dynamic memory chip select 0 (up to 256 MB)
		0xB000 0000 to 0xBFFF FFFF	Dynamic memory chip select 1 (up to 256 MB)
		0xC000 0000 to 0xCFFF FFFF	Dynamic memory chip select 2 (up to 256 MB)
		0xD000 0000 to 0xDFFF FFFF	Dynamic memory chip select 3 (up to 256 MB)
0xE000 0000 to 0xE00F FFFF	Cortex-M4 Private Peripheral Bus	0xE000 0000 to 0xE00F FFFF	Cortex-M4 related functions, includes the NVIC and System Tick Timer.

The LPC408x/7x incorporate several distinct memory regions, shown in the following figures. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

7.9 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.9.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC408x/7x, the NVIC supports 40 vectored interrupts.
- 32 programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.9.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on port 0 and port 2 regardless of the selected function can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

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7.10 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupts being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

7.11 External Memory Controller (EMC)

Remark: The EMC is available for parts LPC4088/78/76. Supported memory size and type and EMC bus width vary for different packages (see Table 2). The EMC pin configuration for each part is shown in Table 5.

Table 5. External memory controller pin configuration

Parts	Data bus pins	Address bus pins	Control pins	
			SRAM	**SDRAM**
LPC4088FBD208 LPC4088FET208 LPC4078FBD208 LPC4078FET208	EMC_D[31:0]	EMC_A[25:0]	$\overline{\text{EMC\_BLS}}$[3:0], $\overline{\text{EMC\_CS}}$[3:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC4088FET180 LPC4078FET180 LPC4076FET180	EMC_D[15:0]	EMC_A[19:0]	$\overline{\text{EMC\_BLS}}$[1:0], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC4088FBD144 LPC4078FBD144 LPC4076FBD144	EMC_D[7:0]	EMC_A[15:0]	$\overline{\text{EMC\_BLS}}$[3:2], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	not available

The LPC408x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

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7.36.3 Wake-up timer

The LPC408x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.36.4 Power control

The LPC408x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC408x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

7.36.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

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Table 16. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time	[2]	-	$t_{clkndly}$ + 3.5	$t_{clk0dly}$ + 5.0	ns
$t_{h(S)}$	chip select hold time	[2]	$t_{clkndly}$ - 1.0	$t_{clkndly}$ - 1.2	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.6	$t_{clkndly}$ + 5.0	ns
$t_{h(RAS)}$	row address strobe hold time	[2]	$t_{clkndly}$ - 0.8	$t_{clkndly}$ - 0.9	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	[2]	-	$t_{clkndly}$ + 3.4	$t_{clkndly}$ + 4.9	ns
$t_{h(CAS)}$	column address strobe hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 1.0	-	ns
$t_{d(WV)}$	write valid delay time	[2]	-	$t_{clkndly}$ + 4.1	$t_{clkndly}$ + 6.0	ns
$t_{h(W)}$	write hold time	[2]	$t_{clkndly}$ - 0.9	$t_{clkndly}$ - 0.7		ns
$t_{d(AV)}$	address valid delay time	[2]	-	$t_{clkndly}$ + 4.6	$t_{clkndly}$ + 6.8	ns
$t_{h(A)}$	address hold time	[2]	$t_{clkndly}$ - 1.1	$t_{clkndly}$ - 1.2	-	ns
Read cycle parameters when EMC_CLKOUT0 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly}	4.5 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly}	-2.9 + t_{fbdly}	-	ns
Read cycle parameters when EMC_CLKOUT1 used						
$t_{su(D)}$	data input set-up time		5.6 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	4.5 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
$t_{h(D)}$	data input hold time		-2.2 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-2.9 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time	[2]	-	$t_{clkndly}$+ 5.4	$t_{clkndly}$+ 7.8	ns
$t_{h(Q)}$	data output hold time	[2]	$t_{clkndly}$ − 0.4	$t_{clkndly}$	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] $t_{clkndly}$ represents $t_{clk0dly}$ when EMC_CLKOUT0 clocks SDRAM. $t_{clkndly}$represents $t_{clk1dly}$ when EMC_CLKOUT1 clocks SDRAM.

Table 17. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1 $t_{clk0dly}$ = 0 and $t_{clk1dly}$ = 0						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	t_{cmddly} + 6.8	t_{cmddly} + 10.4	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.2	t_{cmddly} + 2.1	-	ns

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11.3 External clock

Table 19. Dynamic characteristic: external clock (see Figure 40)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency	1	-	25	MHz
$T_{cy(clk)}$	clock cycle time	40	-	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

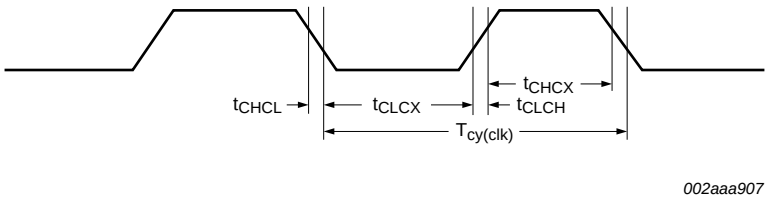

Fig 23. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Internal oscillators

Table 20. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	11.88	12	12.12	MHz
$f_{i(RTC)}$	RTC input frequency	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 I/O pins

Table 21. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pin. For details, see the LPC408x/7x IBIS model available on the NXP website.

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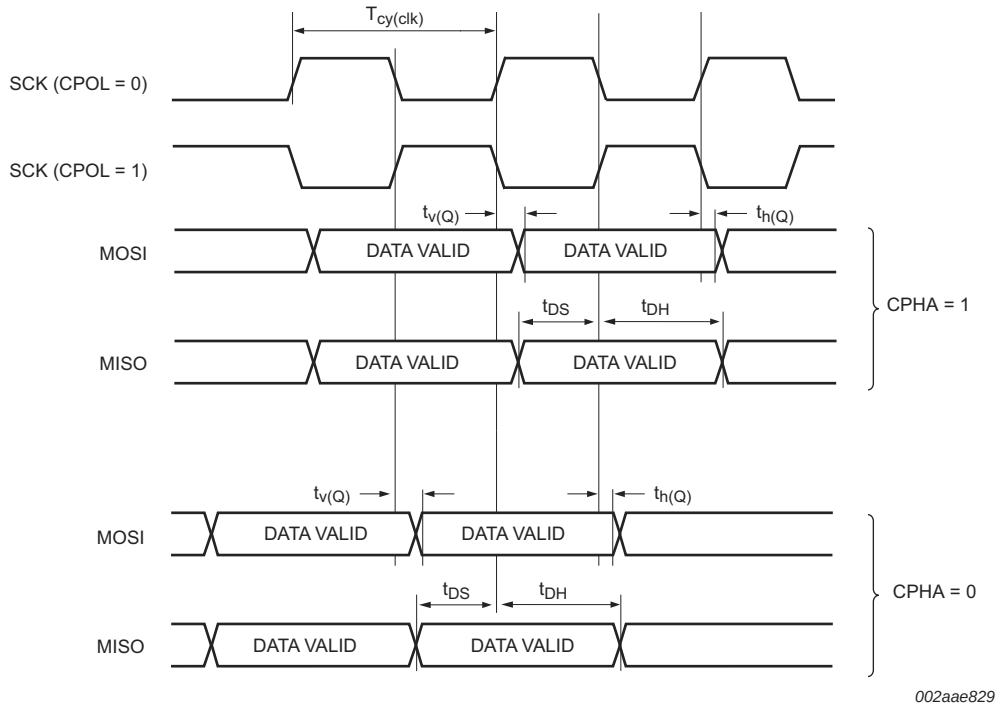

Fig 24. SSP master timing in SPI mode

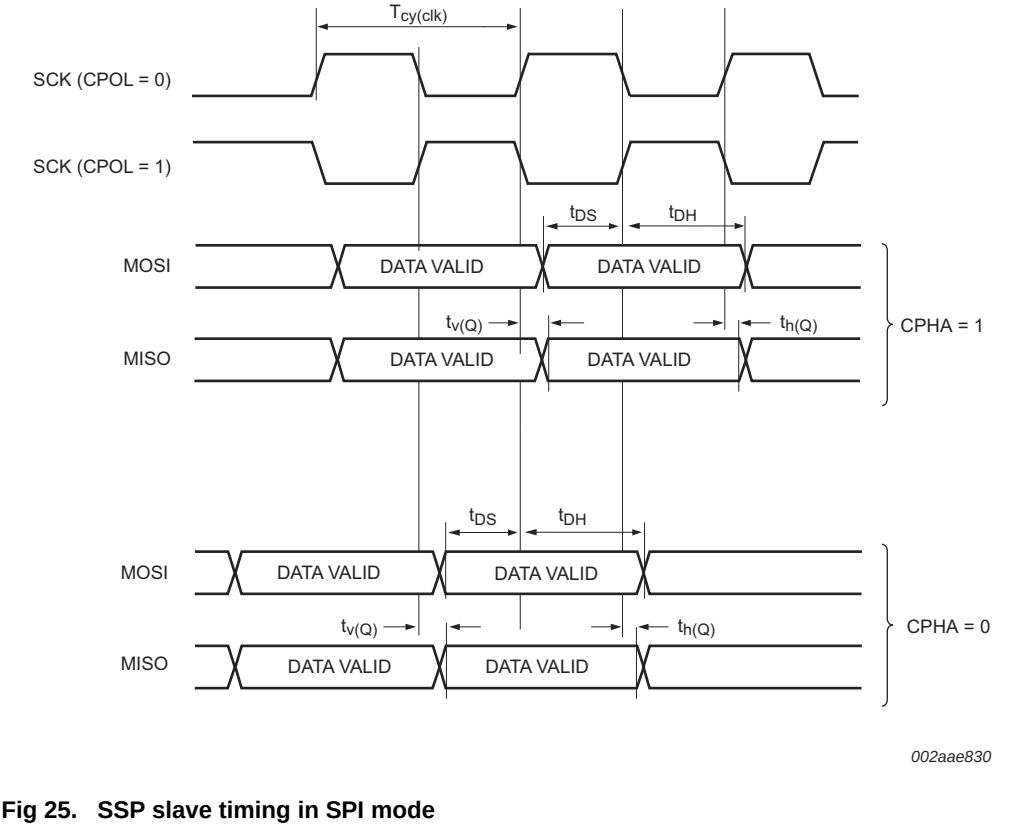

Fig 25. SSP slave timing in SPI mode

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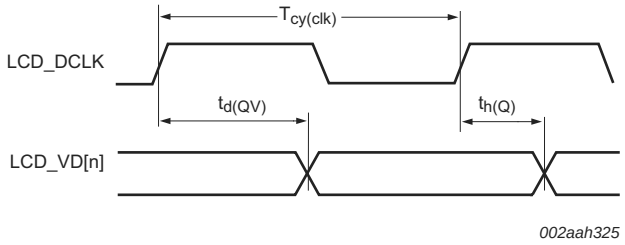

The LCD panel clock is shown with the default polarity. The clock can be inverted via the IPC bit in the LCD_POL register. Typically, the LCD panel uses the falling edge of the LCD_DCLK to sample the data.

Fig 29. LCD timing

11.10 SD/MMC

Remark: The SD/MMC card interface is available on parts LPC4088/78/76.

Table 26. Dynamic characteristics: SD/MMC

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	25	MHz
		on pin SD_CLK; identification mode		25	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DAT[3:0] as outputs	-	23	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DAT[3:0] as outputs	3.5	-	ns

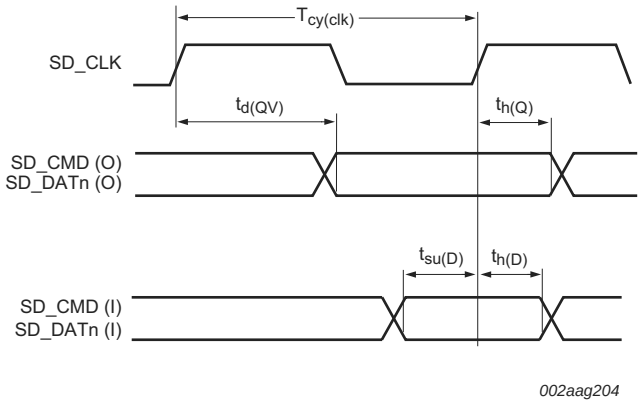

Fig 30. SD/MMC timing

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Table 33. Comparator voltage ladder reference static characteristics
V_{DDA} = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal V_{DDA} supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		–0.45	–0.5	–0.55	%
		decimal code = 16		–0.99	–1.1	–1.21	%
		decimal code = 24		–1.26	–1.4	–1.54	%
		decimal code = 30		–1.35	–1.5	–1.65	%
		decimal code = 31		–1.35	–1.5	–1.65	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		0.44	0.4	0.36	%
		decimal code = 16		–0.18	–0.2	–0.22	%
		decimal code = 24		–0.45	–0.5	–0.55	%
		decimal code = 30		–0.54	–0.6	–0.66	%
		decimal code = 31		–0.45	–0.5	–0.55	%

[1] Measured on typical silicon samples with a 2 kHz input signal and overdrive < 100 μV. Power switched off to all analog peripherals except the comparator.

13. Application information

13.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC4088 and LPC4078/76 and as device-only controller on parts LPC4074/72.

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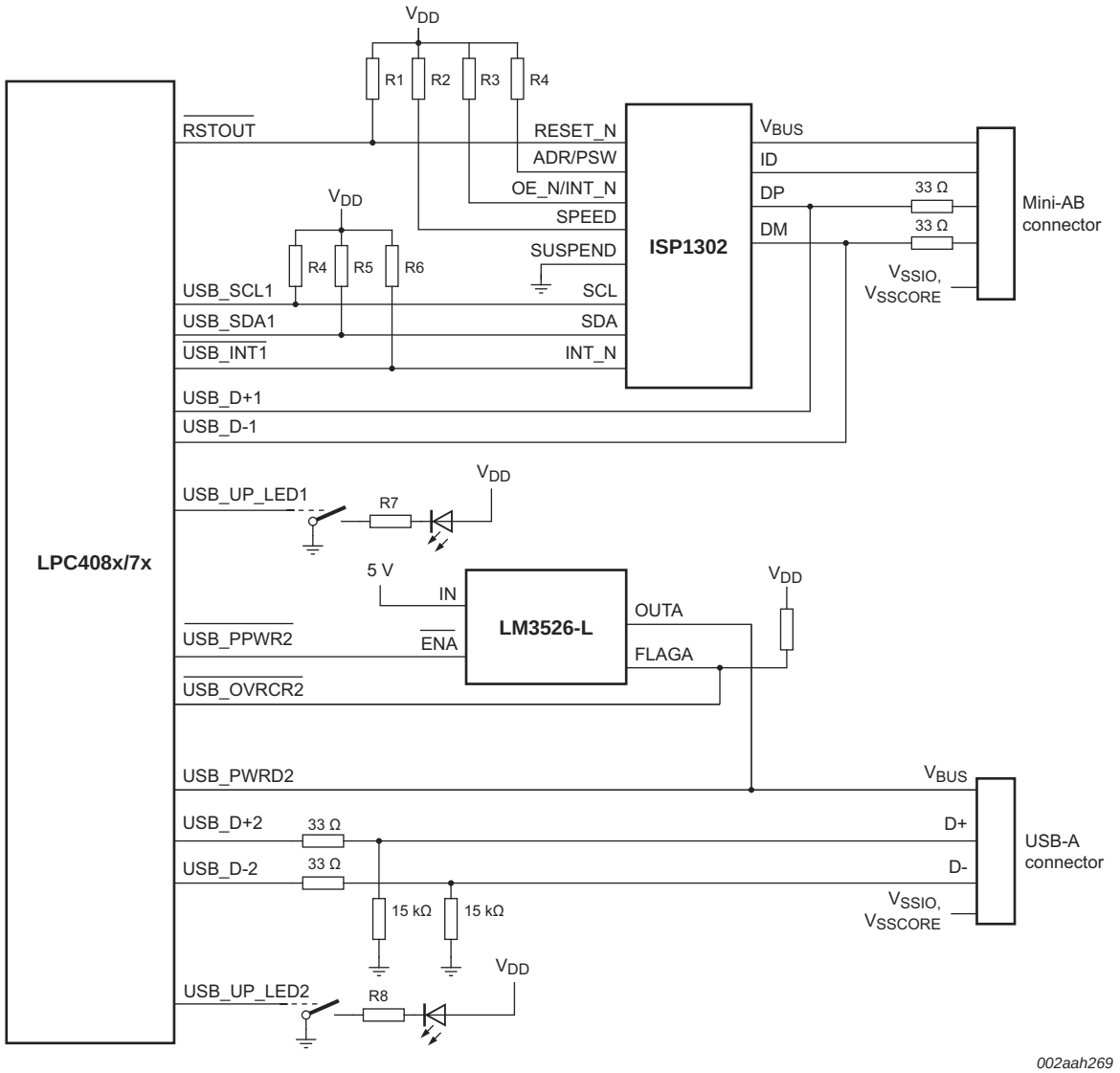

Fig 36. USB OTG port configuration: port 1 OTG dual-role device, port 2 host

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In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 40), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 41 and in Table 34 and Table 35. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 41 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

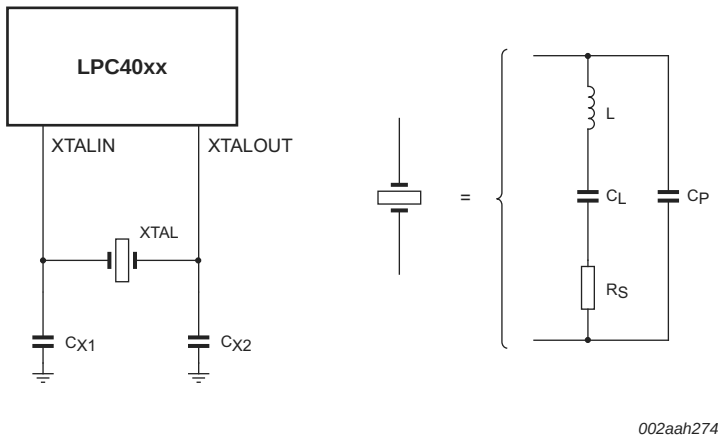

Fig 41. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 34. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

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To eliminate the loss of time counts in the RTC due to voltage swing or ramp rate of the $\overline{\text{RESET}}$ signal, connect an RC filter between the $\overline{\text{RESET}}$ pin and the external reset input.

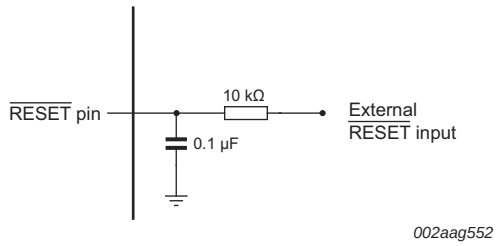

Fig 44. Reset input with RC filter

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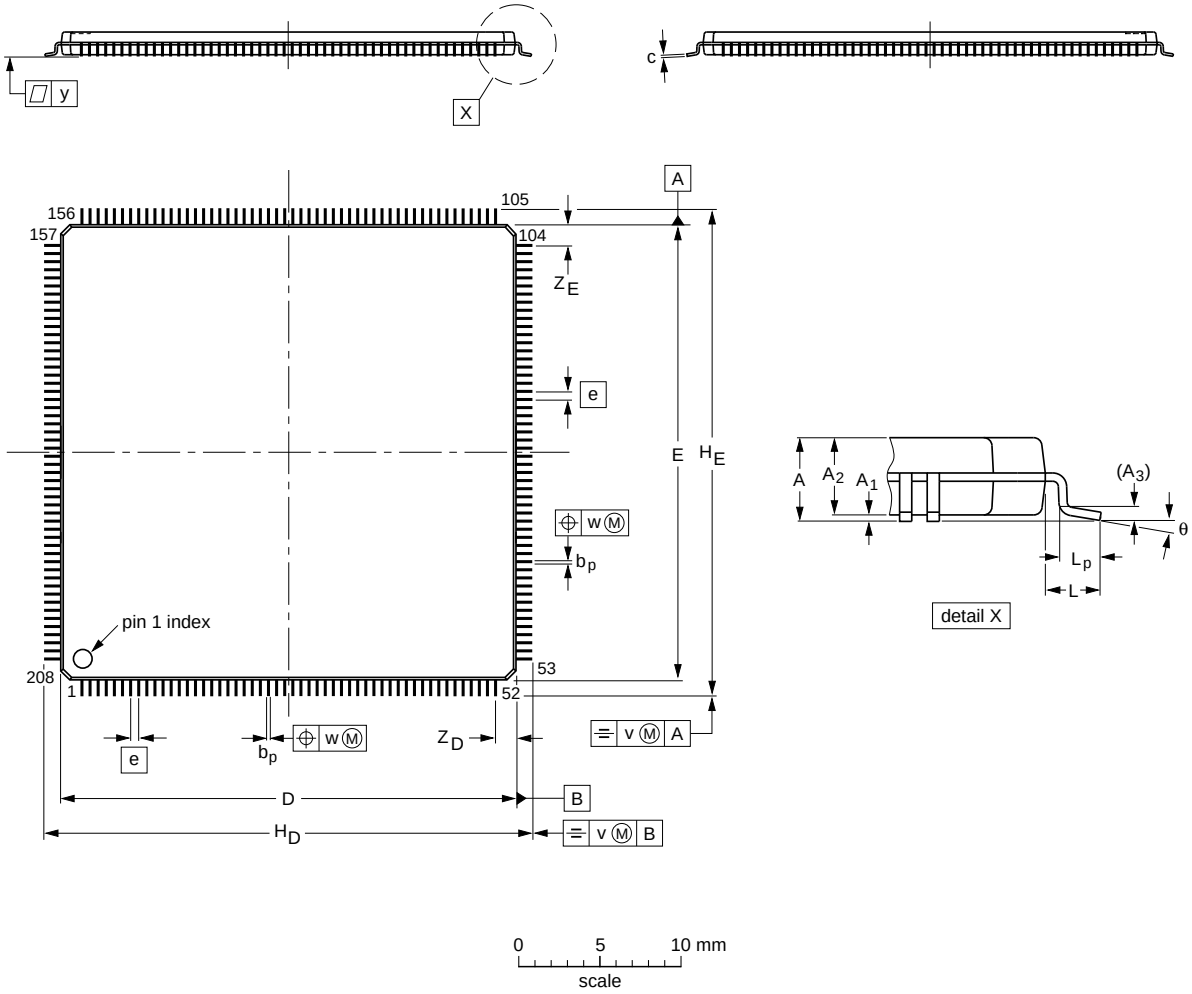
14. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 45. Package outline SOT459-1 (LQFP208)

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21. Contents

continued >>

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