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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4088fbd144-551

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[4]	168	B12	A11	116	81	-	-	[3]	I; PU	I/O	**P0[4] —** General purpose digital input/output pin.
										I/O	**I2S_RX_SCK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
										I	**CAN_RD2 —** CAN2 receiver input.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I/O	**CMP_ROSC —** Comparator relaxation oscillator for 555 timer applications.
										-	**R —** Function reserved.
										O	**LCD_VD[0] —** LCD data.
P0[5]	166	C12	B11	115	80	-	-	[3]	I; PU	I/O	**P0[5] —** General purpose digital input/output pin.
										I/O	**I2S_RX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
										O	**CAN_TD2 —** CAN2 transmitter output.
										I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
										-	**R —** Function reserved.
										I	**CMP_RESET —** Comparator reset.
										-	**R —** Function reserved.
										O	**LCD_VD[1] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[0]	196	A3	B5	136	95	76	A3	[3]	I; PU	I/O	**P1[0] —** General purpose digital input/output pin.
										O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
										I/O	**SSP2_SCK —** Serial clock for SSP2.
P1[1]	194	B5	A5	135	94	75	B4	[3]	I; PU	I/O	**P1[1] —** General purpose digital input/output pin.
										O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT3 —** Match output for Timer 3, channel 3.
										I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
P1[2]	185	D9	B7	-	-	-	-	[3]	I; PU	I/O	**P1[2] —** General purpose digital input/output pin.
										O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
										O	**SD_CLK —** Clock output line for SD card interface.
										O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
P1[3]	177	A10	A9	-	-	-	-	[3]	I; PU	I/O	**P1[3] —** General purpose digital input/output pin.
										O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
										I/O	**SD_CMD —** Command line for SD card interface.
										O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
P1[4]	192	A5	C6	133	93	74	B5	[3]	I; PU	I/O	**P1[4] —** General purpose digital input/output pin.
										O	**ENET_TX_EN —** Ethernet transmit data enable (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT2 —** Match output for Timer 3, channel 2.
										I/O	**SSP2_MISO —** Master In Slave Out for SSP2.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[9]	188	A6	D7	131	91	72	A4	[3]	I; PU	I/O	**P1[9] —** General purpose digital input/output pin.
										I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P1[10]	186	C8	A7	129	90	71	A5	[3]	I; PU	I/O	**P1[10] —** General purpose digital input/output pin.
										I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P1[11]	163	A14	A12	-	-	-	-	[3]	I; PU	I/O	**P1[11] —** General purpose digital input/output pin.
										I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
										I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]	157	A16	A14	-	-	-	-	[3]	I; PU	I/O	**P1[12] —** General purpose digital input/output pin.
										I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
										I/O	**SD_DAT[3] —** Data line 3 for SD card interface.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										-	**R —** Function reserved.
										O	**CMP1_OUT —** Comparator 1, output.
P1[13]	147	D16	D14	-	-	-	-	[3]	I; PU	I/O	**P1[13] —** General purpose digital input/output pin.
										I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[27]	88	T12	M9	61	43	-	-	[3]	I; PU	I/O	**P1[27] —** General purpose digital input/output pin.
										I	**$\overline{\text{USB\_INT1}}$ —** USB port 1 OTG transceiver interrupt (OTG transceiver).
										I	**$\overline{\text{USB\_OVRCR1}}$ —** USB port 1 Over-Current status.
										I	**T0_CAP1 —** Capture input for Timer 0, channel 1.
										O	**CLKOUT —** Selectable clock output.
										-	**R —** Function reserved.
										O	**LCD_VD[13] —** LCD data.
										O	**LCD_VD[21] —** LCD data.
P1[28]	90	T13	P10	63	44	35	J8	[3]	I; PU	I/O	**P1[28] —** General purpose digital input/output pin.
										I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).
										I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
										O	**T0_MAT0 —** Match output for Timer 0, channel 0.
										O	**MC_2A —** Motor control PWM channel 2, output A.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										O	**LCD_VD[14] —** LCD data.
										O	**LCD_VD[22] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[31]	39	N2	-	-	-	-	-	[3]	I; PU	I/O	**P2[31] —** General purpose digital input/output pin.
										O	**EMC_DQM3 —** Data mask 3 used with SDRAM and static devices.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT3 —** Match output for Timer 3, channel 3.
P3[0] to P3[31]										I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block.
P3[0]	197	B4	D6	137	-	-	-	[3]	I; PU	I/O	**P3[0] —** General purpose digital input/output pin.
										I/O	**EMC_D[0] —** External memory data line 0.
P3[1]	201	B3	E6	140	-	-	-	[3]	I; PU	I/O	**P3[1] —** General purpose digital input/output pin.
										I/O	**EMC_D[1] —** External memory data line 1.
P3[2]	207	B1	A2	144	-	-	-	[3]	I; PU	I/O	**P3[2] —** General purpose digital input/output pin.
										I/O	**EMC_D[2] —** External memory data line 2.
P3[3]	3	E4	G5	2	-	-	-	[3]	I; PU	I/O	**P3[3] —** General purpose digital input/output pin.
										I/O	**EMC_D[3] —** External memory data line 3.
P3[4]	13	F2	D3	9	-	-	-	[3]	I; PU	I/O	**P3[4] —** General purpose digital input/output pin.
										I/O	**EMC_D[4] —** External memory data line 4.
P3[5]	17	G1	E3	12	-	-	-	[3]	I; PU	I/O	**P3[5] —** General purpose digital input/output pin.
										I/O	**EMC_D[5] —** External memory data line 5.
P3[6]	23	J1	F4	16	-	-	-	[3]	I; PU	I/O	**P3[6] —** General purpose digital input/output pin.
										I/O	**EMC_D[6] —** External memory data line 6.
P3[7]	27	L1	G3	19	-	-	-	[3]	I; PU	I/O	**P3[7] —** General purpose digital input/output pin.
										I/O	**EMC_D[7] —** External memory data line 7.
P3[8]	191	D8	A6	-	-	-	-	[3]	I; PU	I/O	**P3[8] —** General purpose digital input/output pin.
										I/O	**EMC_D[8] —** External memory data line 8.

7.11.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.12 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.12.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.

7.14 LCD controller

Remark: The LCD controller is available on parts LPC4088.

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.14.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.15 Ethernet

Remark: The Ethernet block is available on parts LPC4088/78/76.

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex

7.16 USB interface

Remark: The USB Device/Host/OTG controller is available on parts LPC4088/78/76. The USB Device-only controller is available on part LPC4074/72.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

See Section 13.1 for details on typical USB interfacing solutions.

7.16.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.16.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC408x/7x can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.16.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

7.16.2.1 Features

- OHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.37.4 APB interface

The APB peripherals are split into two separate APB buses in order to distribute the bus bandwidth and thereby reducing stalls caused by contention between the CPU and the GPDMA controller.

7.37.5 AHB multilayer matrix

The LPC408x/7x use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M4 to the flash memory, the main (32 kB) static RAM, and the Boot ROM. The GPDMA can also access all of these memories. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

7.37.6 External interrupt inputs

The LPC408x/7x include up to 30 edge sensitive interrupt inputs combined with one level sensitive external interrupt input as selectable pin function. The external interrupt input can optionally be used to wake up the processor from Power-down mode.

7.37.7 Memory mapping control

The Cortex-M4 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M4 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC408x/7x is configured for 128 total interrupts.

7.38 Debug control

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail		–0.5	+4.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			–0.5	+4.6	V
V_{DDA}	analog 3.3 V pad supply voltage			–0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		–0.5	+4.6	V

Table 7. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{i(VREFP)}$	input voltage on pin VREFP			–0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		–0.5	+5.1	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD(3V3)} \geq 2.4V$	[2]	–0.5	+5.5	V
		$V_{DD(3V3)} = 0$ V		–0.5	+3.6	V
		other I/O pins	[2][3]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[4]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	-	4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on the required shelf lifetime. Please refer to the JEDEC spec for further details.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

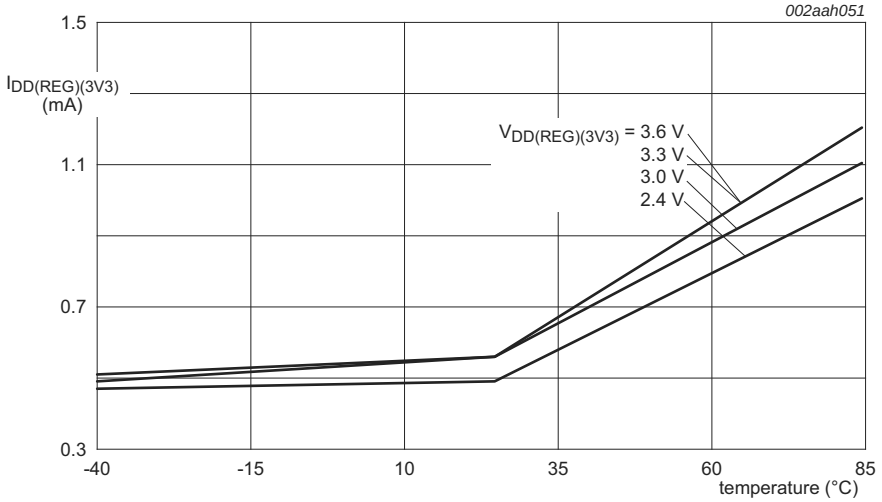
9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

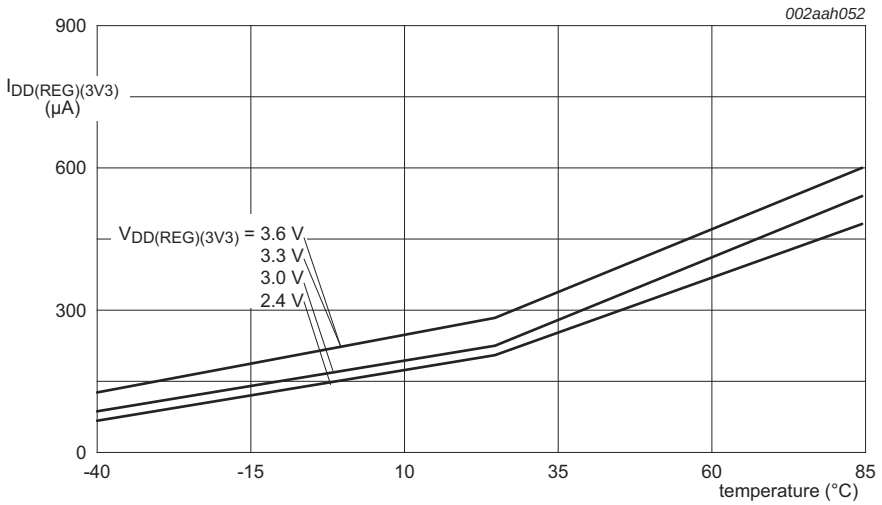
- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

10.1 Power consumption



Conditions: BOD disabled.

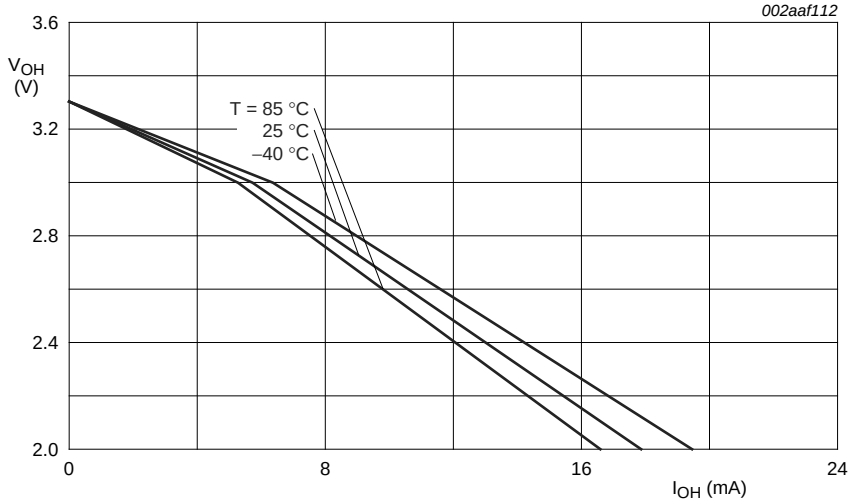
Fig 12. Deep-sleep mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature



Conditions: BOD disabled.

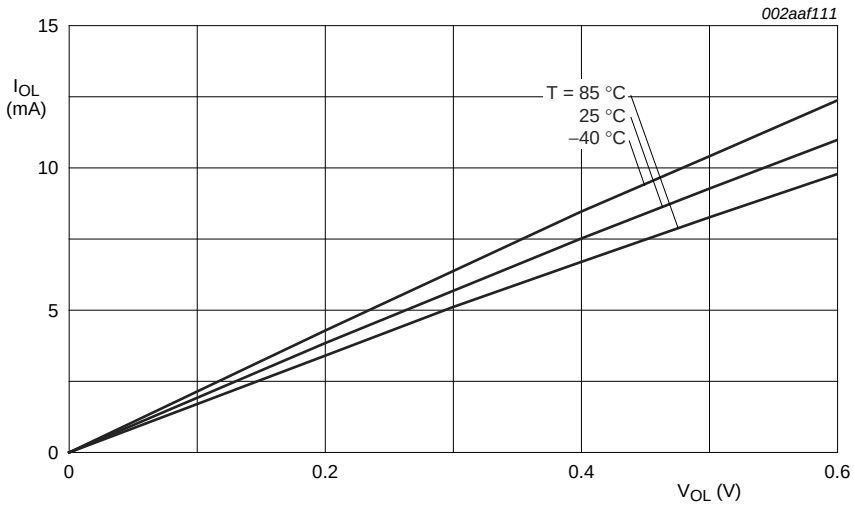
Fig 13. Power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature

10.3 Electrical pin characteristics



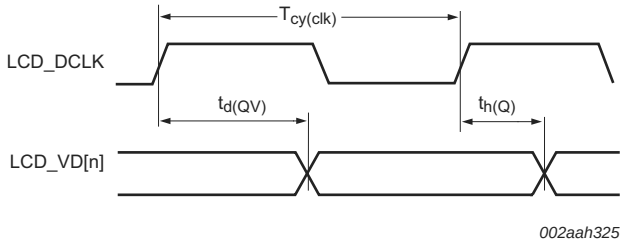
Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 15. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 16. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



The LCD panel clock is shown with the default polarity. The clock can be inverted via the IPC bit in the LCD_POL register. Typically, the LCD panel uses the falling edge of the LCD_DCLK to sample the data.

Fig 29. LCD timing

11.10 SD/MMC

Remark: The SD/MMC card interface is available on parts LPC4088/78/76.

Table 26. Dynamic characteristics: SD/MMC

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	25	MHz
		on pin SD_CLK; identification mode		25	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DAT[3:0] as outputs	-	23	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DAT[3:0] as outputs	3.5	-	ns

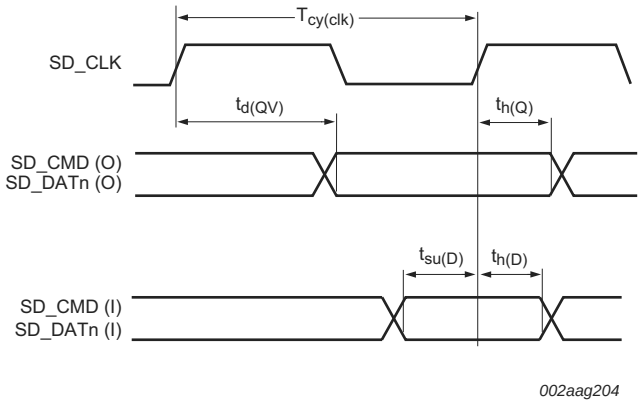
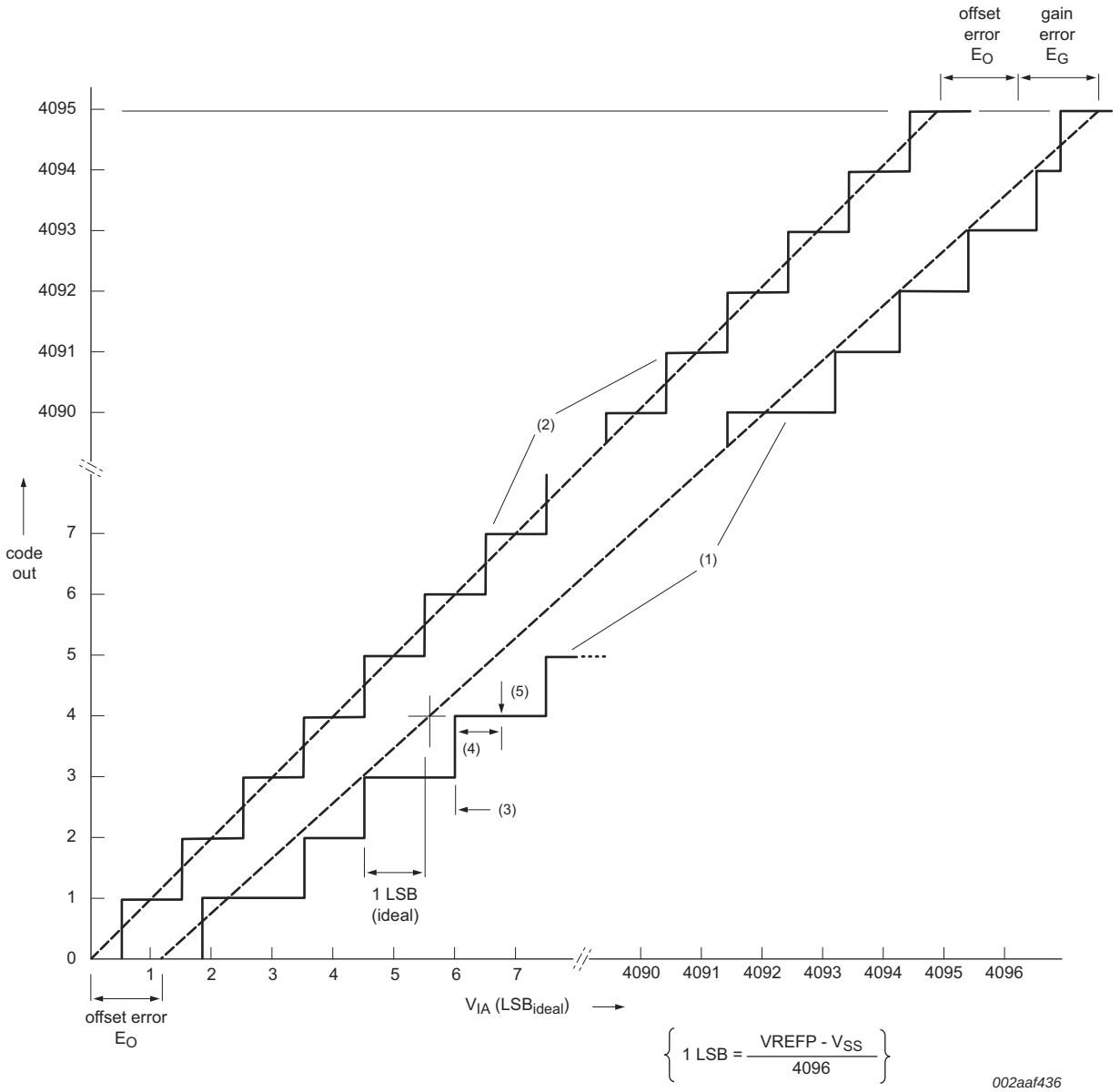


Fig 30. SD/MMC timing



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 32. 12-bit ADC characteristics

Table 33. Comparator voltage ladder reference static characteristics
V_{DDA} = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal V_{DDA} supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		–0.45	–0.5	–0.55	%
		decimal code = 16		–0.99	–1.1	–1.21	%
		decimal code = 24		–1.26	–1.4	–1.54	%
		decimal code = 30		–1.35	–1.5	–1.65	%
		decimal code = 31		–1.35	–1.5	–1.65	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		0.44	0.4	0.36	%
		decimal code = 16		–0.18	–0.2	–0.22	%
		decimal code = 24		–0.45	–0.5	–0.55	%
		decimal code = 30		–0.54	–0.6	–0.66	%
		decimal code = 31		–0.45	–0.5	–0.55	%

[1] Measured on typical silicon samples with a 2 kHz input signal and overdrive < 100 μV. Power switched off to all analog peripherals except the comparator.

13. Application information

13.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC4088 and LPC4078/76 and as device-only controller on parts LPC4074/72.

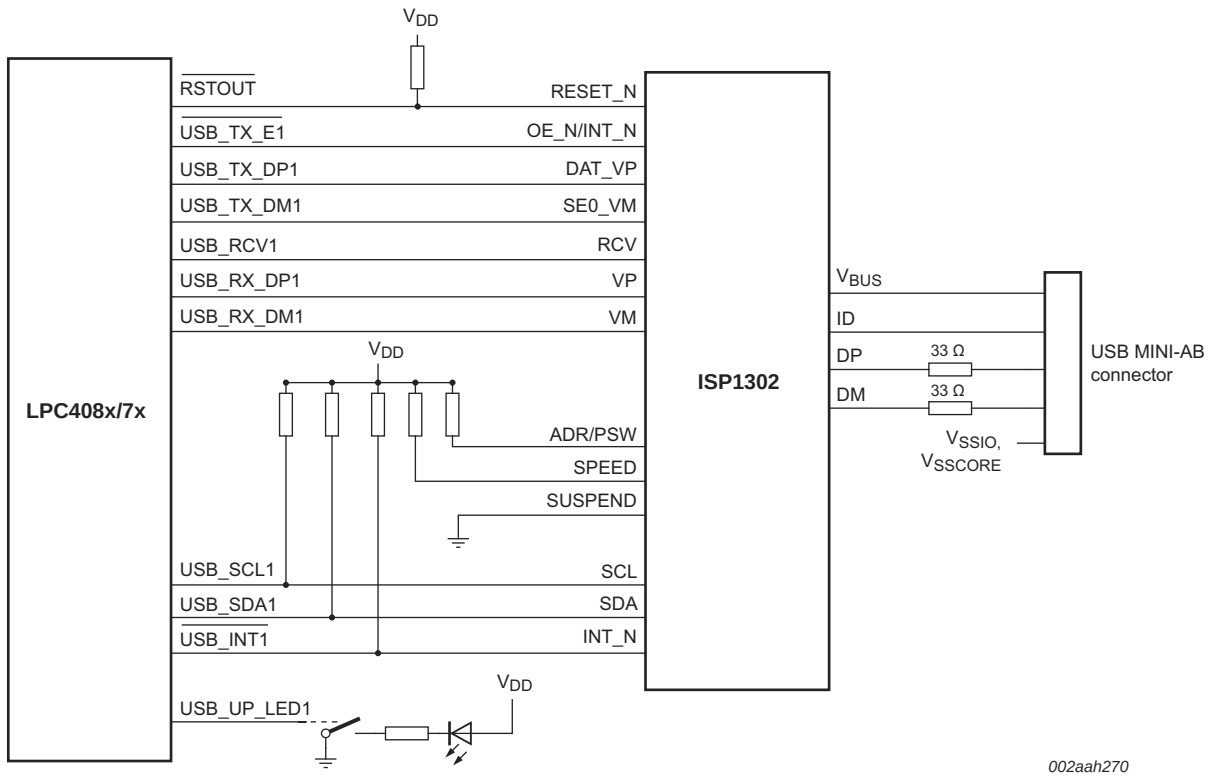


Fig 37. USB OTG port configuration: VP_VM mode

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 40), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 41 and in Table 34 and Table 35. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 41 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

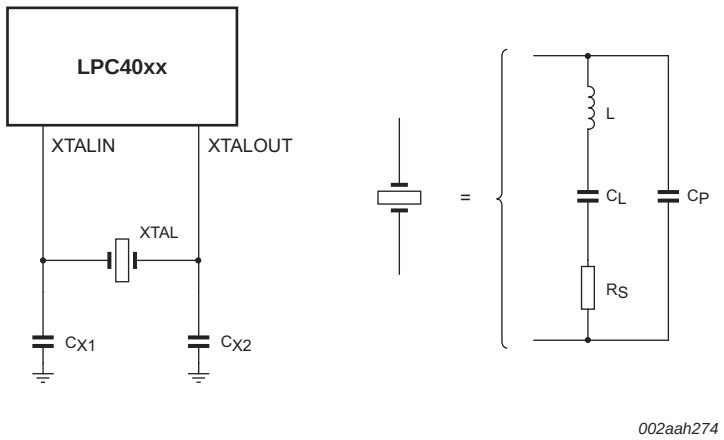


Fig 41. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 34. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 35. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

13.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.

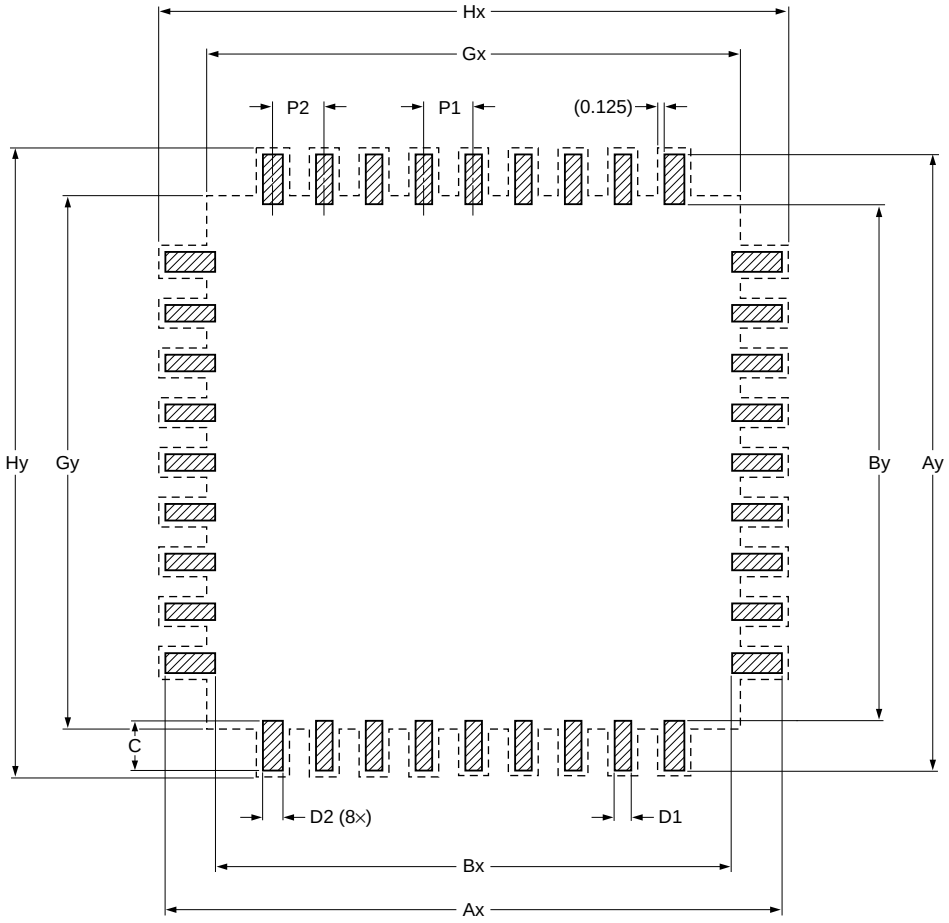
13.4 Standard I/O pin configuration

Figure 42 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver: Open-drain mode enabled/disabled.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Analog input.

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 54. Reflow soldering of the LQFP144 package

21. Contents

continued >>