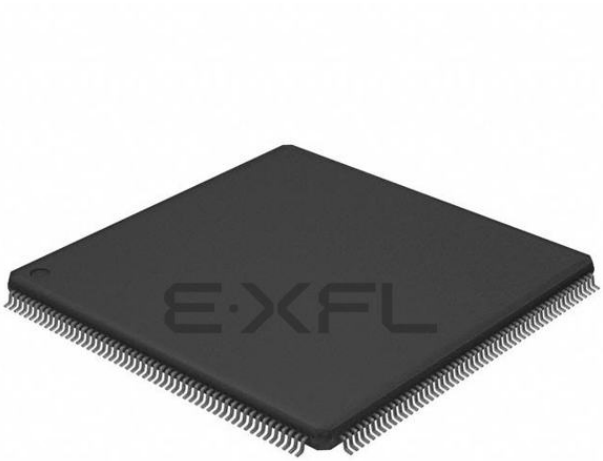

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4088fbd208-551

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[4]	168	B12	A11	116	81	-	-	[3]	I; PU	I/O	**P0[4] —** General purpose digital input/output pin.
										I/O	**I2S_RX_SCK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
										I	**CAN_RD2 —** CAN2 receiver input.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I/O	**CMP_ROSC —** Comparator relaxation oscillator for 555 timer applications.
										-	**R —** Function reserved.
										O	**LCD_VD[0] —** LCD data.
P0[5]	166	C12	B11	115	80	-	-	[3]	I; PU	I/O	**P0[5] —** General purpose digital input/output pin.
										I/O	**I2S_RX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
										O	**CAN_TD2 —** CAN2 transmitter output.
										I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
										-	**R —** Function reserved.
										I	**CMP_RESET —** Comparator reset.
										-	**R —** Function reserved.
										O	**LCD_VD[1] —** LCD data.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[14]	184	A7	D8	128	89	70	C6	[3]	I; PU	I/O	**P1[14] —** General purpose digital input/output pin.
										I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I	**CMP0_IN[0] —** Comparator 0, input 0.
P1[15]	182	A8	A8	126	88	69	B6	[3]	I; PU	I/O	**P1[15] —** General purpose digital input/output pin.
										I	**ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
										-	**R —** Function reserved.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
P1[16]	180	D10	B8	125	87	-	-	[3]	I; PU	I/O	**P1[16] —** General purpose digital input/output pin.
										O	**ENET_MDC —** Ethernet MIIM clock.
										O	**I2S_TX_MCLK —** I2S transmit master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[1] —** Comparator 0, input 1.
P1[17]	178	A9	C9	123	86	-	-	[3]	I; PU	I/O	**P1[17] —** General purpose digital input/output pin.
										I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
										O	**I2S_RX_MCLK —** I2S receive master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[2] —** Comparator 0, input 2.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[18]	66	P7	L5	46	32	25	K4	[3]	I; PU	I/O	**P1[18] —** General purpose digital input/output pin.
										O	**USB_UP_LED1 —** It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
										I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
										-	**R —** Function reserved.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P1[19]	68	U6	P5	47	33	26	J4	[3]	I; PU	I/O	**P1[19] —** General purpose digital input/output pin.
										O	**USB_TX_E1 —** Transmit Enable signal for USB port 1 (OTG transceiver).
										O	**USB_PPWR1 —** Port Power enable signal for USB port 1.
										I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
										O	**MC_0A —** Motor control PWM channel 0, output A.
										I/O	**SSP1_SCK —** Serial clock for SSP1.
										O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[31]	39	N2	-	-	-	-	-	[3]	I; PU	I/O	**P2[31] —** General purpose digital input/output pin.
										O	**EMC_DQM3 —** Data mask 3 used with SDRAM and static devices.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT3 —** Match output for Timer 3, channel 3.
P3[0] to P3[31]										I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block.
P3[0]	197	B4	D6	137	-	-	-	[3]	I; PU	I/O	**P3[0] —** General purpose digital input/output pin.
										I/O	**EMC_D[0] —** External memory data line 0.
P3[1]	201	B3	E6	140	-	-	-	[3]	I; PU	I/O	**P3[1] —** General purpose digital input/output pin.
										I/O	**EMC_D[1] —** External memory data line 1.
P3[2]	207	B1	A2	144	-	-	-	[3]	I; PU	I/O	**P3[2] —** General purpose digital input/output pin.
										I/O	**EMC_D[2] —** External memory data line 2.
P3[3]	3	E4	G5	2	-	-	-	[3]	I; PU	I/O	**P3[3] —** General purpose digital input/output pin.
										I/O	**EMC_D[3] —** External memory data line 3.
P3[4]	13	F2	D3	9	-	-	-	[3]	I; PU	I/O	**P3[4] —** General purpose digital input/output pin.
										I/O	**EMC_D[4] —** External memory data line 4.
P3[5]	17	G1	E3	12	-	-	-	[3]	I; PU	I/O	**P3[5] —** General purpose digital input/output pin.
										I/O	**EMC_D[5] —** External memory data line 5.
P3[6]	23	J1	F4	16	-	-	-	[3]	I; PU	I/O	**P3[6] —** General purpose digital input/output pin.
										I/O	**EMC_D[6] —** External memory data line 6.
P3[7]	27	L1	G3	19	-	-	-	[3]	I; PU	I/O	**P3[7] —** General purpose digital input/output pin.
										I/O	**EMC_D[7] —** External memory data line 7.
P3[8]	191	D8	A6	-	-	-	-	[3]	I; PU	I/O	**P3[8] —** General purpose digital input/output pin.
										I/O	**EMC_D[8] —** External memory data line 8.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P3[19]	161	B14	-	-	-	-	-	[3]	I; PU	I/O	**P3[19] —** General purpose digital input/output pin.
										I/O	**EMC_D[19] —** External memory data line 19.
										O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
P3[20]	167	A13	-	-	-	-	-	[3]	I; PU	I/O	**P3[20] —** General purpose digital input/output pin.
										I/O	**EMC_D[20] —** External memory data line 20.
										O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
										I	**U1_DSR —** Data Set Ready input for UART1.
P3[21]	175	C10	-	-	-	-	-	[3]	I; PU	I/O	**P3[21] —** General purpose digital input/output pin.
										I/O	**EMC_D[21] —** External memory data line 21.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
P3[22]	195	C6	-	-	-	-	-	[3]	I; PU	I/O	**P3[22] —** General purpose digital input/output pin.
										I/O	**EMC_D[22] —** External memory data line 22.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										I	**U1_RI —** Ring Indicator input for UART1.
P3[23]	65	T6	M4	45	-	-	-	[3]	I; PU	I/O	**P3[23] —** General purpose digital input/output pin.
										I/O	**EMC_D[23] —** External memory data line 23.
										I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
										I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
P3[24]	58	R5	N3	40	-	-	-	[3]	I; PU	I/O	**P3[24] —** General purpose digital input/output pin.
										I/O	**EMC_D[24] —** External memory data line 24.
										O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
										I	**T0_CAP1 —** Capture input for Timer 0, channel 1.

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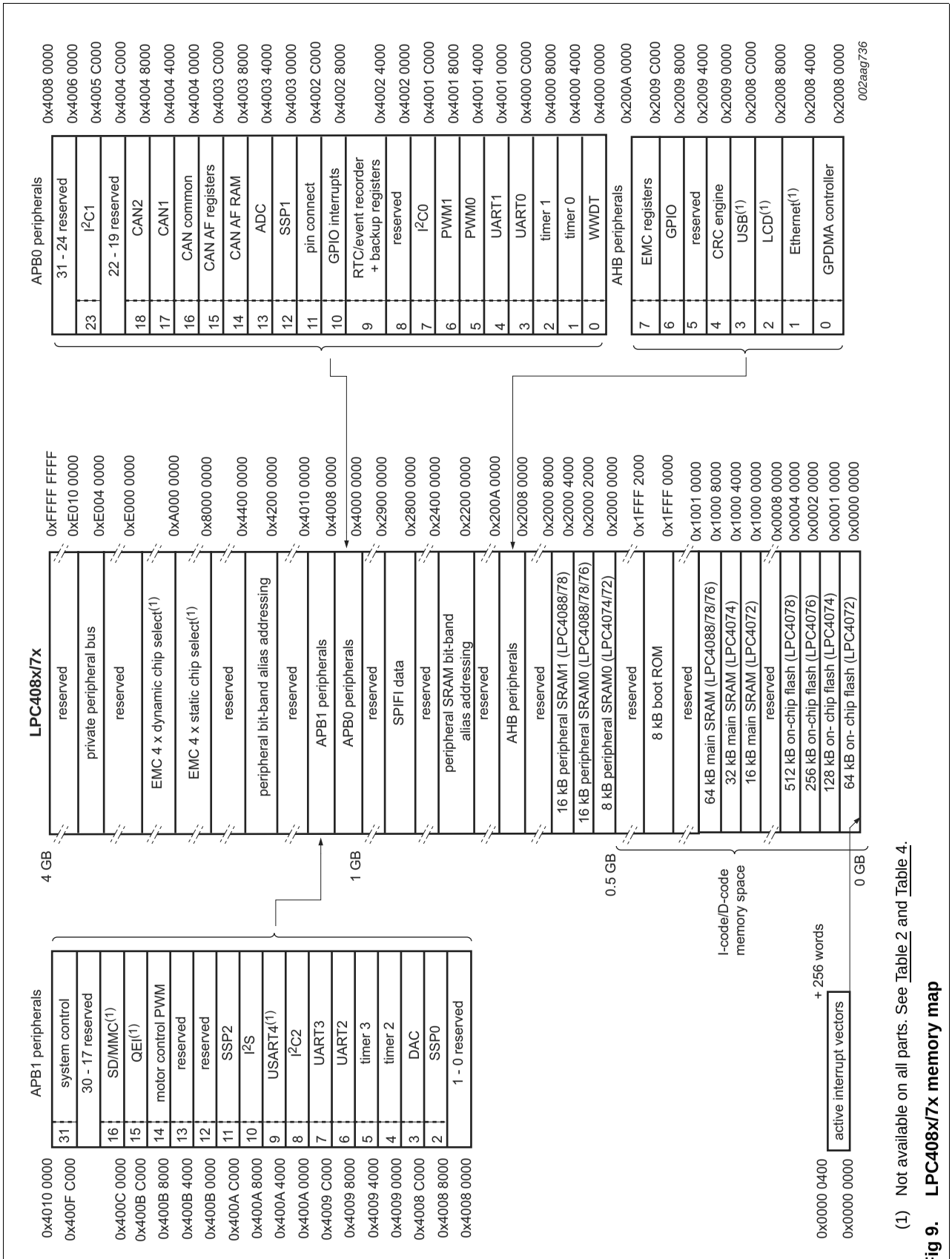

(1) Not available on all parts. See Table 2 and Table 4.

Fig 9. LPC408x/7x memory map

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- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M4 bit banding.
- Support for use with the GPDMA controller.

Additionally, any pin on Port 0 and Port 2 providing a digital function can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake up the chip from Power-down mode.

7.18.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Pull-up/pull-down resistor configuration and open-drain configuration can be programmed through the pin connect block for each GPIO pin.

7.19 12-bit ADC

The LPC408x/7x contain one ADC. It is a single 12-bit successive approximation ADC with eight channels and DMA support.

7.19.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among eight pins.
- Power-down mode.
- Measurement range V_{SS} to VREFP.
- 12-bit conversion rate: up to 400 kHz.
- Individual channels can be selected for conversion.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.
- DMA support.

7.20 10-bit DAC

The LPC408x/7x contain one DAC. The DAC allows to generate a variable analog output. The maximum output value of the DAC is VREFP.

7.20.1 Features

- 10-bit DAC.
- Resistor string architecture.

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7.24.1 Features

- Maximum SSP speed of 33 Mbit/s (master) or 10 Mbit/s (slave).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.
- DMA transfers supported by GPDMA.

7.25 I^2C-bus serial I/O controllers

The LPC408x/7x contain three I^2C-bus controllers.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial Data Line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.25.1 Features

- All I^2C-bus controllers can use standard GPIO pins with bit rates of up to 400 kbit/s (Fast I^2C-bus). The I^2C0-bus interface uses special open-drain pins with bit rates of up to 400 kbit/s.
- The I^2C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s for I2C0 using pins P5[2] and P5[3].
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- Both I^2C-bus controllers support multiple address recognition and a bus monitor mode.

7.26 I^2S-bus serial I/O controllers

The LPC408x/7x contain one I^2S-bus interface. The I^2S-bus provides a standard communication interface for digital audio applications.

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7.36.4.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins and/or the I/O power via the $V_{DD(3V3)}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC408x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.36.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC. This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.36.5 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.36.6 Power domains

The LPC408x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC408x/7x, I/O pads are powered by $V_{DD(3V3)}$, while $V_{DD(REG)(3V3)}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC408x/7x application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

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Table 8. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 9. Thermal resistance (LQFP packages)

T_{amb} = −40 °C to +85 °C unless otherwise specified.

		Thermal resistance value (°C/W): ±15 %		
		LQFP80	**LQFP144**	**LQFP208**
θja				
	JEDEC (4.5 in × 4 in)			
	0 m/s	41	31	27
	1 m/s	35	28	25
	2.5 m/s	32	26	24
	Single-layer (4.5 in × 3 in)			
	0 m/s	61	43	35
	1 m/s	47	35	31
	2.5 m/s	43	33	29
θjc		7.8	9.2	10.5
θjb		11.6	13.5	15.2

Table 10. Thermal resistance value (TFBGA packages)

T_{amb} = −40 °C to +85 °C unless otherwise specified.

		Thermal resistance value (°C/W): ±15 %	
		TFBGA180	**TFBGA208**
θja			
	JEDEC (4.5 in × 4 in)		
	0 m/s	47	43
	1 m/s	39	37
	2.5 m/s	35	33
	8-layer (4.5 in × 3 in)		
	0 m/s	39	37
	1 m/s	35	33
	2.5 m/s	31	30
θjc		8.5	7.4
θjb		13	16

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Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{CM}	differential common mode voltage range	includes V_{DI} range	[20]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[20]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	[20]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	[20]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[20]	-	-	20	pF
Oscillator pins (see Section 13.2)							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	-	3.6	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD((3V3)}$ ≤ 3.6 V. Guaranteed by design.

[3] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[5] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[6] Boost control bits in the PBOOST register set to 0x0 (see *LPC408x/7x User manual*).

[7] Boost control bits in the PBOOST register set to 0x3 (see *LPC408x/7x User manual*).

[8] IRC running at 12 MHz; main oscillator and PLL disabled; PCLK = CCLK/4.

[9] BOD disabled.

[10] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 0; T_{amb} = 25 °C.

[11] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[12] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[13] V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[14] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[15] Including voltage on outputs in 3-state mode.

[16] $V_{DD(3V3)}$ supply voltages must be present.

[17] 3-state outputs go into 3-state mode in Deep power-down mode.

[18] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[19] To V_{SS}.

[20] 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

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Table 18. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY, CLKOUT0DLY and CLKOUT1DLY)

T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V.Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbols	Parameter	Five bit value for each delay in EMCDLYCTL[1]	Min	Typ	Max	Unit
t_{cmddly}, t_{fbdly}, $t_{clk0dly}$, $t_{clk1dly}$	delay time	b00000	0.0	0.0	0.0	ns
		b00001	0.1	0.1	0.2	ns
		b00010	0.2	0.3	0.5	ns
		b00011	0.3	0.4	0.7	ns
		b00100	0.5	0.8	1.3	ns
		b00101	0.6	0.9	1.5	ns
		b00110	0.7	1.1	1.8	ns
		b00111	0.8	1.2	2.0	ns
		b01000	1.2	1.8	2.9	ns
		b01001	1.3	1.9	3.1	ns
		b01010	1.4	2.0	3.4	ns
		b01011	1.5	2.1	3.6	ns
		b01100	1.7	2.6	4.2	ns
		b01101	1.8	2.7	4.4	ns
		b01110	1.9	2.9	4.7	ns
		b01111	2.0	3.0	4.9	ns
		b10000	2.4	3.7	6.0	ns
		b10001	2.5	3.8	6.2	ns
		b10010	2.6	4.0	6.5	ns
		b10011	2.7	4.1	6.7	ns
		b10100	2.9	4.5	7.3	ns
		b10101	3.0	4.6	7.5	ns
		b10110	3.1	4.8	7.8	ns
		b10111	3.2	4.9	8.0	ns
		b11000	3.6	5.4	8.9	ns
		b11001	3.7	5.5	9.1	ns
		b11010	3.8	5.7	9.4	ns
		b11011	3.9	5.8	9.6	ns
		b11100	4.1	6.2	10.2	ns
		b11101	4.2	6.3	10.4	ns
		b11110	4.3	6.6	10.7	ns
		b11111	4.4	6.7	10.9	ns

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0. See the *LPC408x/7x user manual* for details.

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11.6 SSP interface

Table 22. Dynamic characteristics: SSP pins in SPI mode

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
SSP master						
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	30	-	ns
		when only transmitting		30	-	ns
t_{DS}	data set-up time	in SPI mode	[2]	14.8	-	ns
t_{DH}	data hold time	in SPI mode	[2]	2	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	6.3	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	−2.4	-	ns
SSP slave						
$T_{cy(clk)}$	clock cycle time		[3]	100	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	14.8	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	2	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	$3*T_{cy(PCLK)} + 6.3$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	−2.4	-	ns

[1] The minimum clock cycle time, and therefore the maximum frequency of the SSP in master mode, is limited by the pin electronics to the value given. The SSP block should not be configured to generate a clock faster than that. At and below the maximum frequency, $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] T_{amb} = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$. The maximum clock rate in slave mode is 1/12th of the PCLK rate.

[4] T_{amb} = 25 °C; $V_{DD(3V3)}$ = 3.3 V.

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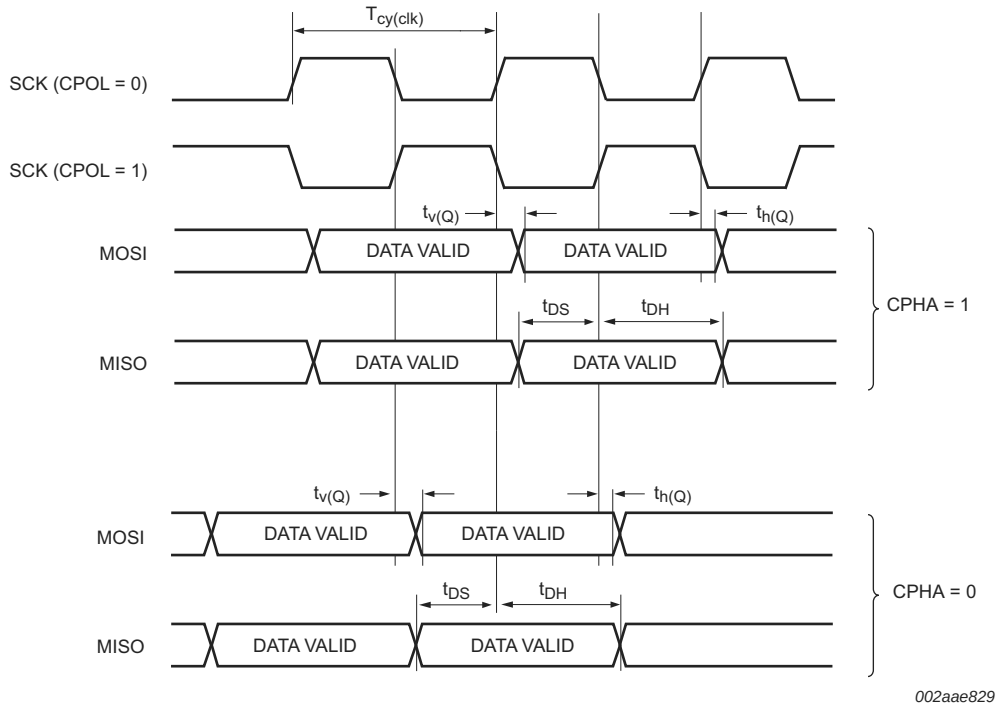

Fig 24. SSP master timing in SPI mode

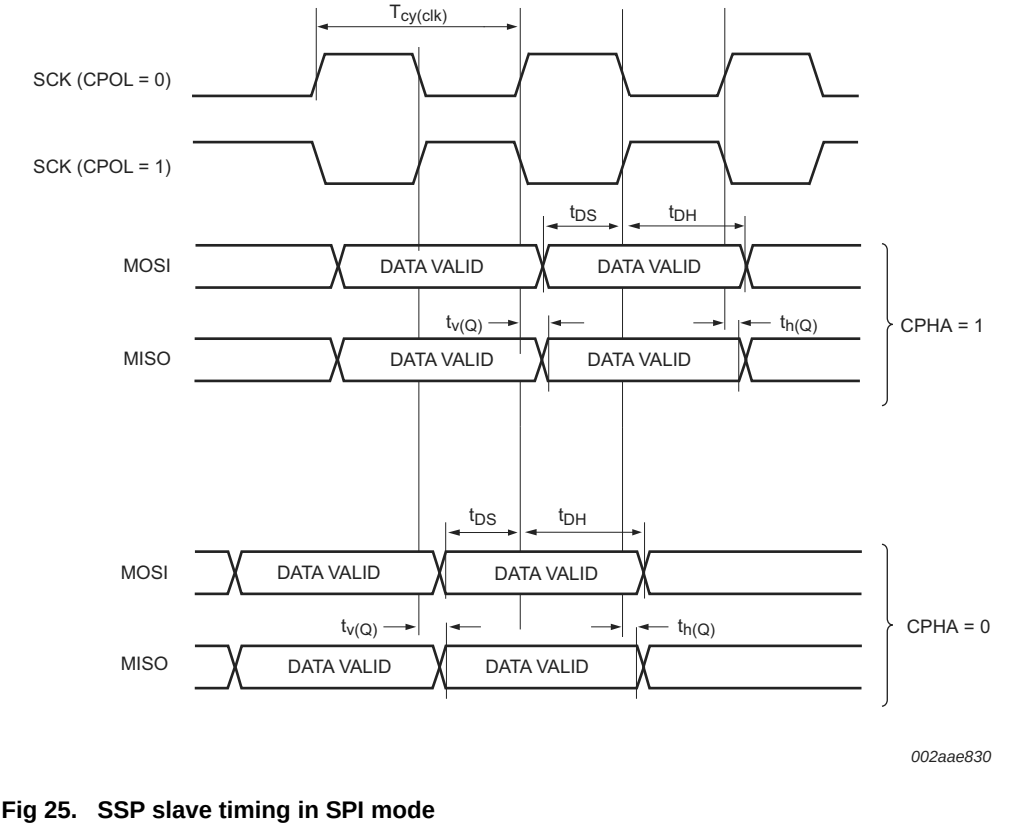

Fig 25. SSP slave timing in SPI mode

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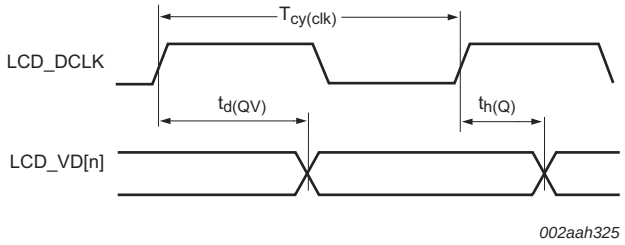

The LCD panel clock is shown with the default polarity. The clock can be inverted via the IPC bit in the LCD_POL register. Typically, the LCD panel uses the falling edge of the LCD_DCLK to sample the data.

Fig 29. LCD timing

11.10 SD/MMC

Remark: The SD/MMC card interface is available on parts LPC4088/78/76.

Table 26. Dynamic characteristics: SD/MMC

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	25	MHz
		on pin SD_CLK; identification mode		25	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DAT[3:0] as outputs	-	23	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DAT[3:0] as outputs	3.5	-	ns

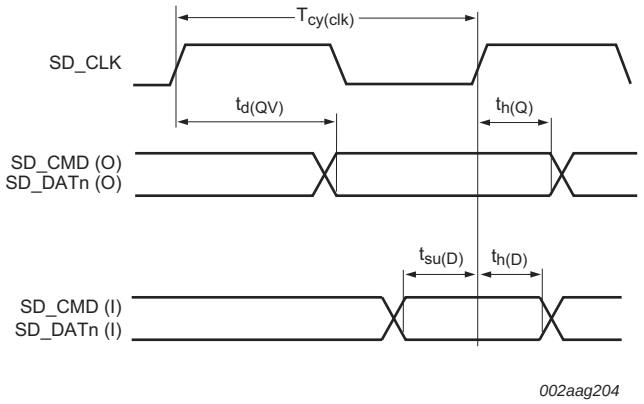

Fig 30. SD/MMC timing

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11.11 SPIFI

Table 27. Dynamic characteristics: SPIFI

T_{amb} = −40 °C to 85 °C; 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V; C_L = 30 pF. Values guaranteed by design.

Symbol	Parameter	Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	11.8	-	ns
t_{DS}	data set-up time	4.8	-	ns
t_{DH}	data hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	8.8	ns
$t_{h(Q)}$	data output hold time	3	-	ns

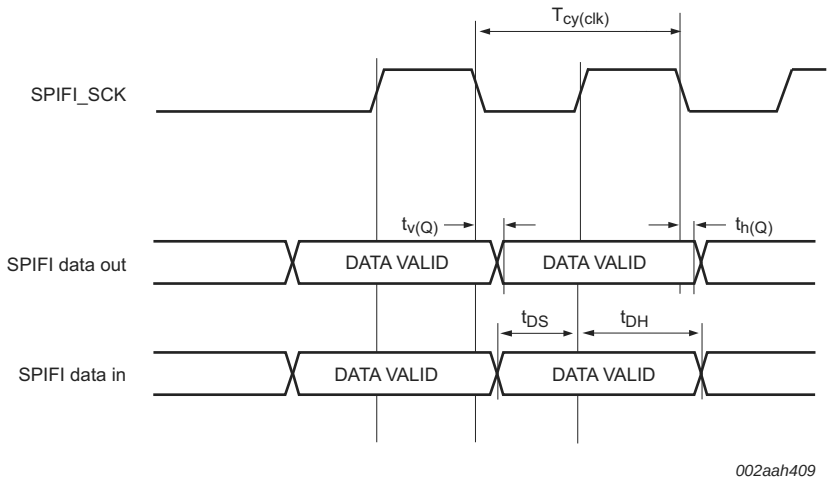

Fig 31. SPIFI timing (Mode 0)

12. Characteristics of the analog peripherals

12.1 ADC electrical characteristics

Table 28. 12-bit ADC characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
12-bit resolution							
E_D	differential linearity error		[2][3][4]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	-	±6	LSB
E_O	offset error		[2][6]	-	-	±5	LSB
E_G	gain error		[2][7]	-	-	±5	LSB
E_T	absolute error		[2][8]	-	-	< ±8	LSB
$f_{clk(ADC)}$	ADC clock frequency			-	-	12.4	MHz

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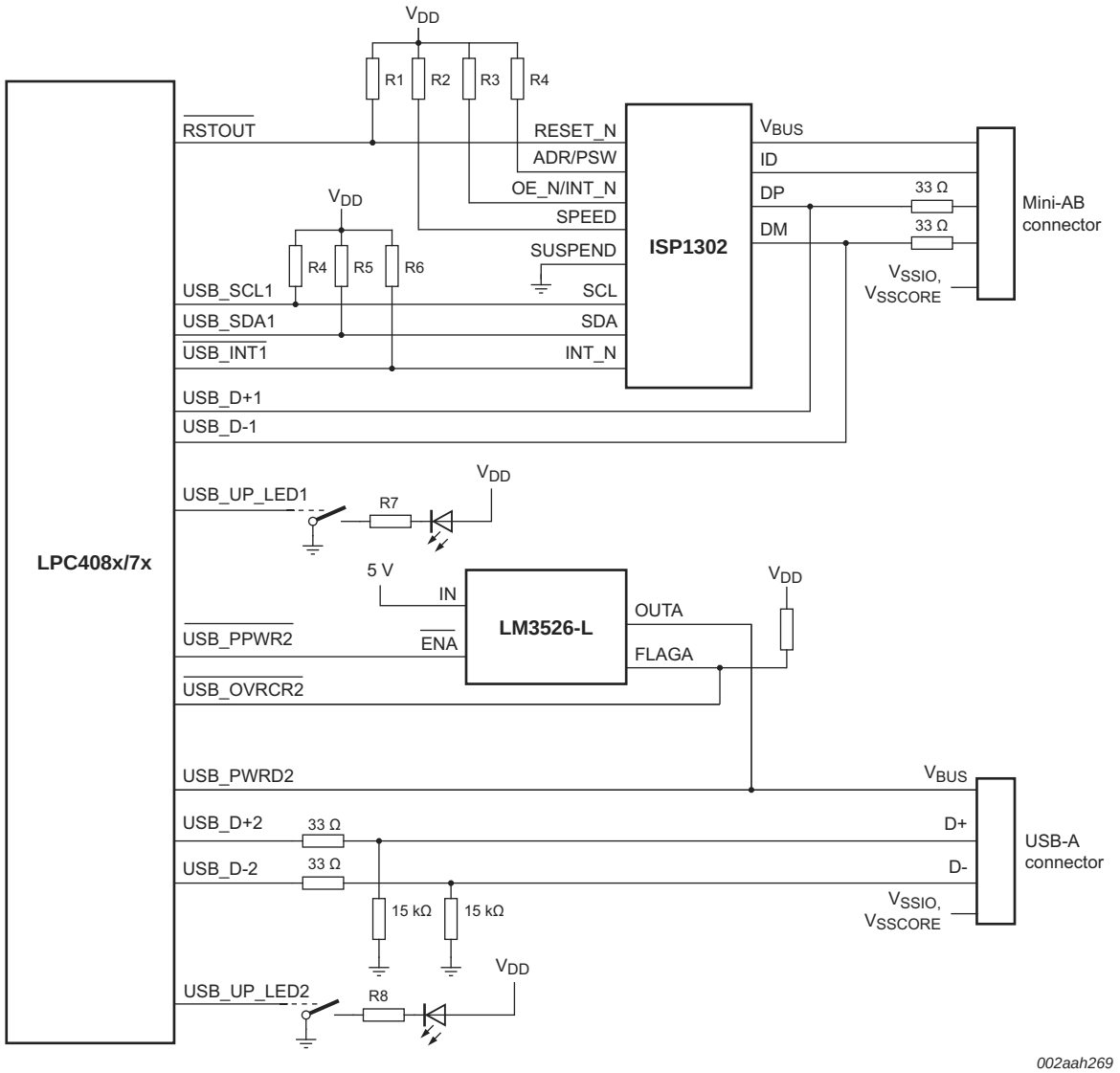

Fig 36. USB OTG port configuration: port 1 OTG dual-role device, port 2 host

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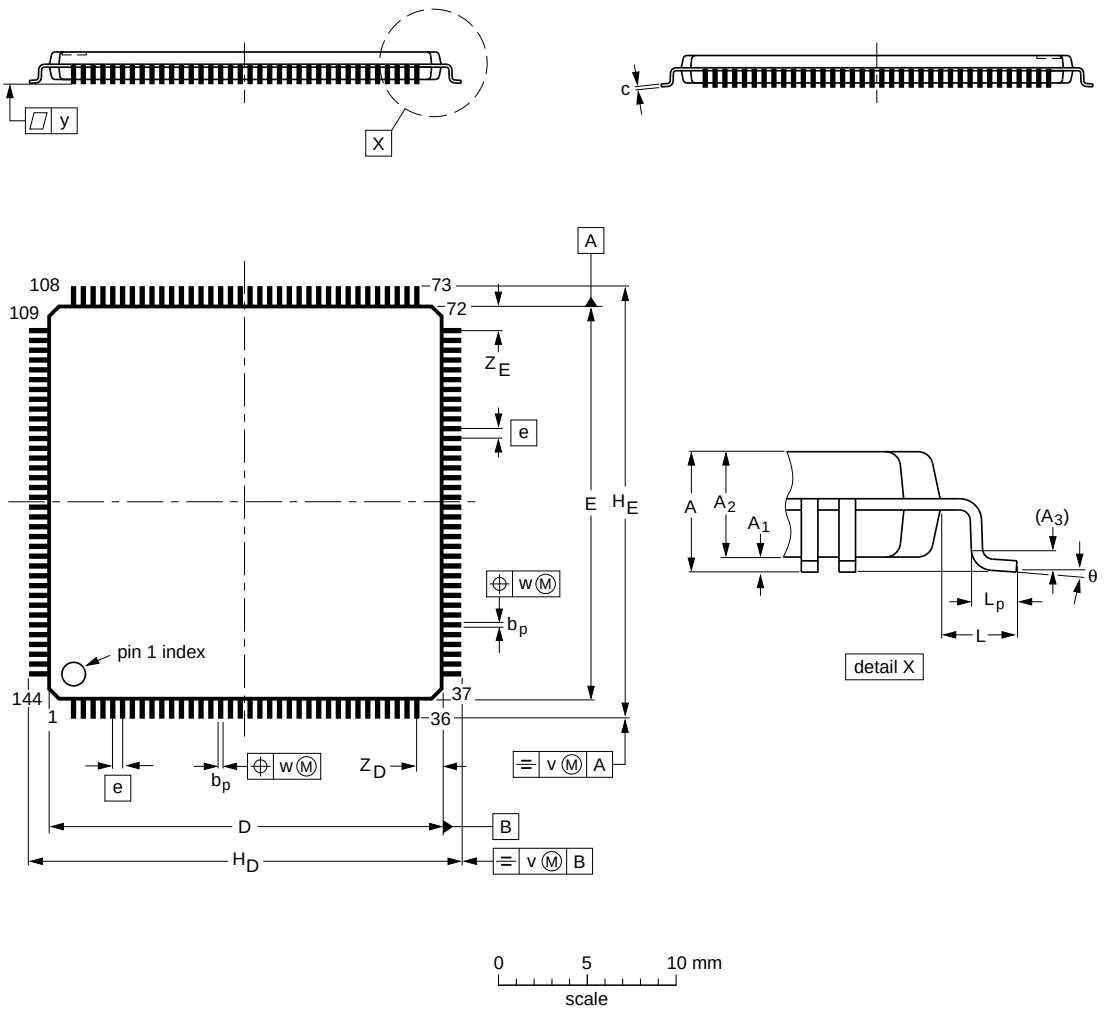
LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 48. Package outline SOT486-1 (LQFP144)

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