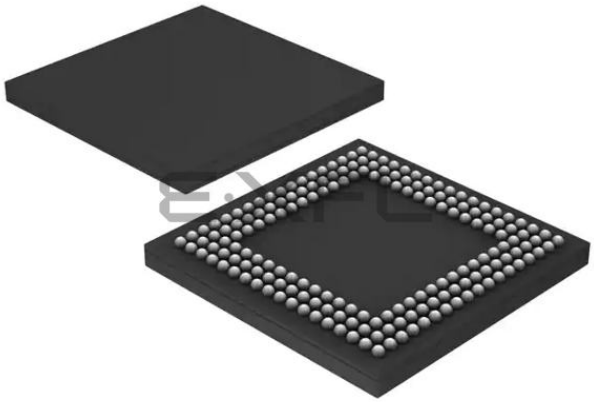


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4088fet180-551

- Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
- Three SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
- Three enhanced I^2C-bus interfaces, one with a true open-drain output supporting the full I^2C-bus specification and Fast-mode Plus with data rates of 1 Mbit/s, two with standard port pins. Enhancements include multiple address recognition and monitor mode.
- I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- CAN controller with two channels.

- Digital peripherals:
  - SD/MMC memory card interface.
  - Up to 165 General Purpose I/O (GPIO) pins depending on the packaging, with configurable pull-up/down resistors, open-drain mode, and repeater mode. All GPIOs are located on an AHB bus for fast access and support Cortex-M4 bit-banding. GPIOs can be accessed by the General Purpose DMA Controller. Any pin of ports 0 and 2 can be used to generate an interrupt.
  - Two external interrupt inputs configurable as edge/level sensitive. All pins on port 0 and port 2 can be used as edge sensitive interrupt sources.
  - Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input. Specific timer events can be selected to generate DMA requests.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - Two standard PWM/timer blocks with external count input option.
  - One motor control PWM with support for three-phase motor control.
  - Real-Time Clock (RTC) with a separate power domain. The RTC is clocked by a dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers, allowing system status to be stored when the rest of the chip is powered off. Battery power can be supplied from a standard 3 V lithium button cell. The RTC will continue working when the battery voltage drops to as low as 2.1 V. An RTC interrupt can wake up the CPU from any reduced power mode.
  - Event Recorder that can capture the clock value when an event occurs on any of three inputs. The event identification and the time it occurred are stored in registers. The Event Recorder is located in the RTC power domain and can therefore operate as long as there is RTC power.
  - Windowed Watchdog Timer (WWDT). Windowed operation, dedicated internal oscillator, watchdog warning interrupt, and safety features.
  - CRC Engine block can calculate a CRC on supplied data using one of three standard polynomials. The CRC engine can be used in conjunction with the DMA controller to generate a CRC without CPU involvement in the data transfer.
- Analog peripherals:
  - 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 400 kHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[4]	168	B12	A11	116	81	-	-	[3]	I; PU	I/O	**P0[4] —** General purpose digital input/output pin.
										I/O	**I2S_RX_SCK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
										I	**CAN_RD2 —** CAN2 receiver input.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I/O	**CMP_ROSC —** Comparator relaxation oscillator for 555 timer applications.
										-	**R —** Function reserved.
										O	**LCD_VD[0] —** LCD data.
P0[5]	166	C12	B11	115	80	-	-	[3]	I; PU	I/O	**P0[5] —** General purpose digital input/output pin.
										I/O	**I2S_RX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
										O	**CAN_TD2 —** CAN2 transmitter output.
										I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
										-	**R —** Function reserved.
										I	**CMP_RESET —** Comparator reset.
										-	**R —** Function reserved.
										O	**LCD_VD[1] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[13]	45	R2	J5	32	-	-	-	[5]	I; PU	I/O	**P0[13] —** General purpose digital input/output pin.
										O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
										I	**ADC0_IN[7] —** A/D converter 0, input 7. When configured as an ADC input, the digital function of the pin must be disabled.
P0[14]	69	T7	M5	48	-	-	-	[3]	I; PU	I/O	**P0[14] —** General purpose digital input/output pin.
										O	**USB_HSTEN2 —** Host Enabled status for USB port 2.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
P0[15]	128	J16	H13	89	62	47	F9	[3]	I; PU	I/O	**P0[15] —** General purpose digital input/output pin.
										O	**U1_TXD —** Transmitter output for UART1.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[2] —** Data bit 0 for SPIFI.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[5]	156	A17	B13	-	-	-	-	[3]	I; PU	I/O	**P1[5] —** General purpose digital input/output pin.
										O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
										O	**SD_PWR —** Power Supply Enable for external SD card power supply.
										O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
										-	**R —** Function reserved.
										I	**CMP1_IN[1] —** Comparator 1, input 1.
P1[6]	171	B11	B10	-	-	-	-	[3]	I; PU	I/O	**P1[6] —** General purpose digital input/output pin.
										I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
										I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
										O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
										-	**R —** Function reserved.
										I	**CMP0_IN[3] —** Comparator 0, input 3.
P1[7]	153	D14	C13	-	-	-	-	[3]	I; PU	I/O	**P1[7] —** General purpose digital input/output pin.
										I	**ENET_COL —** Ethernet Collision detect (MII interface).
										I/O	**SD_DAT[1] —** Data line 1 for SD card interface.
										O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
										-	**R —** Function reserved.
										I	**CMP1_IN[0] —** Comparator 1, input 0.
P1[8]	190	C7	B6	132	92	73	C5	[3]	I; PU	I/O	**P1[8] —** General purpose digital input/output pin.
										I	**ENET_CRS (ENET_CRS_DV) —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
										-	**R —** Function reserved.
										O	**T3_MAT1 —** Match output for Timer 3, channel 1.
										I/O	**SSP2_SSEL —** Slave Select for SSP2.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[9]	188	A6	D7	131	91	72	A4	[3]	I; PU	I/O	**P1[9] —** General purpose digital input/output pin.
										I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P1[10]	186	C8	A7	129	90	71	A5	[3]	I; PU	I/O	**P1[10] —** General purpose digital input/output pin.
										I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P1[11]	163	A14	A12	-	-	-	-	[3]	I; PU	I/O	**P1[11] —** General purpose digital input/output pin.
										I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
										I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]	157	A16	A14	-	-	-	-	[3]	I; PU	I/O	**P1[12] —** General purpose digital input/output pin.
										I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
										I/O	**SD_DAT[3] —** Data line 3 for SD card interface.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										-	**R —** Function reserved.
										O	**CMP1_OUT —** Comparator 1, output.
P1[13]	147	D16	D14	-	-	-	-	[3]	I; PU	I/O	**P1[13] —** General purpose digital input/output pin.
										I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[29]	92	U14	N10	64	45	36	K8	[3]	I; PU	I/O	**P1[29] —** General purpose digital input/output pin.
										I/O	**USB_SDA1 —** USB port 1 I^2C serial data (OTG transceiver).
										I	**PWM1_CAP1 —** Capture input for PWM1, channel 1.
										O	**T0_MAT1 —** Match output for Timer 0, channel 1.
										O	**MC_2B —** Motor control PWM channel 2, output B.
										O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
										O	**LCD_VD[15] —** LCD data.
										O	**LCD_VD[23] —** LCD data.
P1[30]	42	P2	K3	30	21	18	J2	[5]	I; PU	I/O	**P1[30] —** General purpose digital input/output pin.
										I	**USB_PWRD2 —** Power Status for USB port 2.
										I	**USB_VBUS —** Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur.
										I	**ADC0_IN[4] —** A/D converter 0, input 4. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2C0_SDA —** I^2C0 data input/output (this pin does not use a specialized I2C pad.
										O	**U3_OE —** RS-485/EIA-485 output enable signal for UART3.
P1[31]	40	P1	K2	28	20	17	H2	[5]	I; PU	I/O	**P1[31] —** General purpose digital input/output pin.
										I	**$\overline{\text{USB\_OVRCR2}}$ —** Over-Current status for USB port 2.
										I/O	**SSP1_SCK —** Serial Clock for SSP1.
										I	**ADC0_IN[5] —** A/D converter 0, input 5. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin does not use a specialized I2C pad.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[3]	144	E16	E13	100	70	55	C10	[3]	I; PU	I/O	**P2[3] —** General purpose digital input/output pin.
										O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
										O	**T2_MAT2 —** Match output for Timer 2, channel 2.
										-	**R —** Function reserved.
										O	**TRACEDATA[2] —** Trace data, bit 2.
										-	**R —** Function reserved.
										O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
P2[4]	142	D17	E14	99	69	54	C9	[3]	I; PU	I/O	**P2[4] —** General purpose digital input/output pin.
										O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
										I	**U1_DSR —** Data Set Ready input for UART1.
										O	**T2_MAT1 —** Match output for Timer 2, channel 1.
										-	**R —** Function reserved.
										O	**TRACEDATA[1] —** Trace data, bit 1.
										-	**R —** Function reserved.
										O	**LCD_ENAB_M —** STN AC bias drive or TFT data enable output.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[5]	140	F16	F12	97	68	53	D10	[3]	I; PU	I/O	**P2[5] —** General purpose digital input/output pin.
										O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										O	**T2_MAT0 —** Match output for Timer 2, channel 0.
										-	**R —** Function reserved.
										O	**TRACEDATA[0] —** Trace data, bit 0.
										-	**R —** Function reserved.
										O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
P2[6]	138	E17	F13	96	67	52	E8	[3]	I; PU	I/O	**P2[6] —** General purpose digital input/output pin.
										I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
										I	**U1_RI —** Ring Indicator input for UART1.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.
										O	**TRACECLK —** Trace clock.
										O	**LCD_VD[0] —** LCD data.
										O	**LCD_VD[4] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P4[28]	170	C11	D10	118	82	65	B7	[3]	I; PU	I/O	**P4[28] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_BLS2}}$ —** LOW active Byte Lane select signal 2.
										O	**U3_TXD —** Transmitter output for UART3.
										O	**T2_MAT0 —** Match output for Timer 2, channel 0.
										-	**R —** Function reserved.
										O	**LCD_VD[6] —** LCD data.
										O	**LCD_VD[10] —** LCD data.
										O	**LCD_VD[2] —** LCD data.
P4[29]	176	B10	B9	122	85	68	A6	[3]	I; PU	I/O	**P4[29] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3.
										I	**U3_RXD —** Receiver input for UART3.
										O	**T2_MAT1 —** Match output for Timer 2, channel 1.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										O	**LCD_VD[7] —** LCD data.
										O	**LCD_VD[11] —** LCD data.
										O	**LCD_VD[3] —** LCD data.
P4[30]	187	B7	C7	130	-	-	-	[3]	I; PU	I/O	**P4[30] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_CS0}}$ —** LOW active Chip Select 0 signal.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**CMP0_OUT —** Comparator 0, output.
P4[31]	193	A4	E7	134	-	-	-	[3]	I; PU	I/O	**P4[31] —** General purpose digital input/output pin.
										O	**$\overline{\text{EMC\_CS1}}$ —** LOW active Chip Select 1 signal.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
RTCX2	36	L2	J3	25	18	15	G2	[14] [15]		O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
USB_D−2	52	U1	N2	37	-	-	-	[9]		I/O	USB port 2 bidirectional D− line.
VBAT	38	M3	K1	27	19	16	H1			I	RTC power supply: 3.3 V on this pin supplies power to the RTC.
$V_{DD(REG)(3V3)}$	26, 86, 174	H4, P11, D11	G1, N9, E9	18, 60, 121	13, 42, 84	34, 67	K7, C7			S	3.3 V regulator supply voltage: This is the power supply for the on-chip voltage regulator that supplies internal logic.
V_{DDA}	20	G4	F2	14	10	8	E3			S	Analog 3.3 V pad supply voltage: This can be connected to the same supply as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. Tie this pin to 3.3 V if the ADC and DAC are not used.
$V_{DD(3V3)}$	15, 60, 71, 89, 112, 125, 146, 165, 181, 198	G3, P6, P8, U13, P17, K16, C17, B13, C9, D7	E2, L4, K8, L11, J14, E12, E10, C5	41, 62, 77, 102, 114, 138	28, 54, 71, 96	21, 42, 56, 77	K2, H7, D8, C4			S	3.3 V supply voltage: This is the power supply voltage for I/O other than pins in the VBAT domain.
VREFP	24	K1	G2	17	12	10	E1			S	ADC positive reference voltage: This should be the same voltage as V_{DDA}, but should be isolated to minimize noise and error. The voltage level on this pin is used as a reference for ADC and DAC. Tie this pin to 3.3 V if the ADC and DAC are not used.

[9] Not 5 V tolerant. Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[10] 5 V tolerant pad with 5 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[11] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 1 MHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[12] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[13] This pad can be powered from VBAT.

[14] Pad provides special analog functionality. A 32 kHz crystal oscillator must be used with the RTC. An external clock (32 kHz) can't be used to drive the RTCX1 pin.

[15] If the RTC is not used, these pins can be left floating.

[16] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses are faster than the system bus and are used similarly to Tightly Coupled Memory (TCM) interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

The LPC408x/7x use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 processor is running at frequencies of up to 120 MHz. The processor executes the Thumb-2 instruction set for optimal performance and code size, including hardware division, single-cycle multiply, and bit-field manipulation. A Memory Protection Unit (MPU) supporting eight regions is included.

7.3 ARM Cortex-M4 Floating Point Unit (FPU)

Remark: The FPU is available on parts LP4088/78/76.

The FPU supports single-precision floating-point computation functionality in compliance with the ANSI/IEEE Standard 754-2008. The FPU provides add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also performs a variety of conversions between fixed-point, floating-point, and integer data formats.

7.4 On-chip flash program memory

The LPC408x/7x contain up to 512 kB of on-chip flash program memory. A new two-port flash accelerator maximizes performance for use with the two fast AHB-Lite buses.

controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.29.1 Features

- LPC408x/7x has two PWM blocks with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

7.30 Motor control PWM

The LPC408x/7x contain one motor control PWM.

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.33.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source is a dedicated watchdog oscillator, which is always running if the watchdog timer is enabled.

7.34 RTC and backup registers

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC on the LPC408x/7x is designed to have extremely low power consumption, i.e. less than 1 μA. The RTC will typically run from the main chip power supply conserving battery power while the rest of the device is powered up. When operating from a battery, the RTC will continue working down to 2.1 V. Battery power can be provided from a standard 3 V lithium button cell.

An ultra-low power 32 kHz oscillator will provide a 1 Hz clock to the time counting portion of the RTC, moving most of the power consumption out of the time counting function.

The RTC includes a calibration mechanism to allow fine-tuning the count rate in a way that will provide less than 1 second per day error when operated at a constant voltage and temperature.

The RTC contains a small set of backup registers (20 bytes) for holding data while the main part of the LPC408x/7x is powered off.

The RTC includes an alarm function that can wake up the LPC408x/7x from all reduced power modes with a time resolution of 1 s.

7.34.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.

7.36.3 Wake-up timer

The LPC408x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.36.4 Power control

The LPC408x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC408x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

7.36.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

Table 7. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{i(VREFP)}$	input voltage on pin VREFP			–0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		–0.5	+5.1	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD(3V3)} \geq 2.4V$	[2]	–0.5	+5.5	V
		$V_{DD(3V3)} = 0$ V		–0.5	+3.6	V
		other I/O pins	[2][3]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[4]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	-	4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on the required shelf lifetime. Please refer to the JEDEC spec for further details.

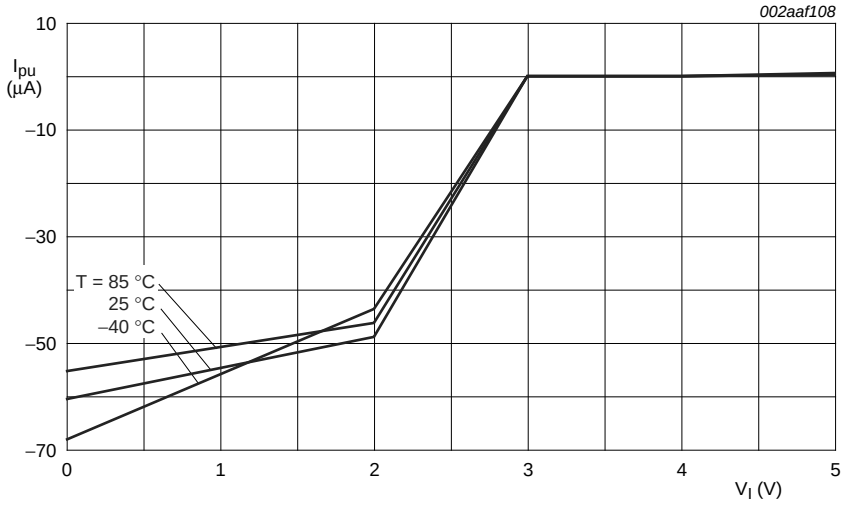
[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

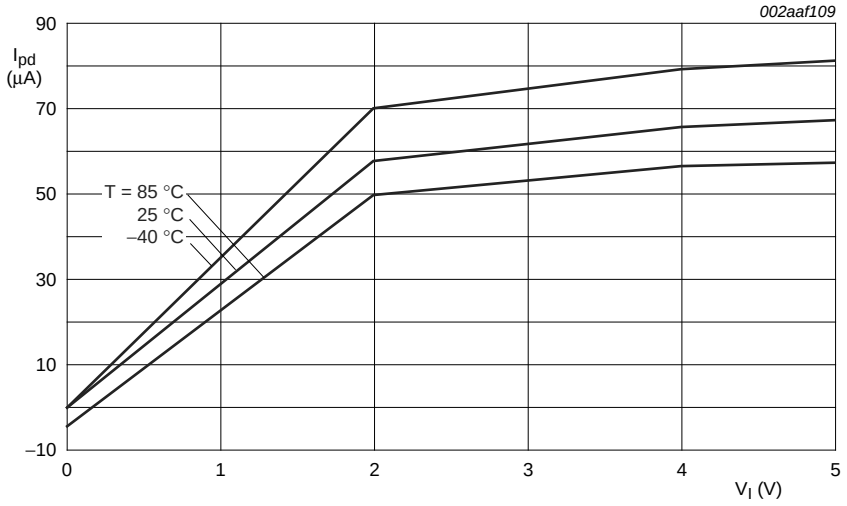
$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 17. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 18. Typical pull-down current I_{pd} versus input voltage V_I

[2] Parameters specified for 40 % of $V_{DD(3V3)}$ for rising edges and 60 % of $V_{DD(3V3)}$ for falling edges.

[3] $T_{cy(clk)}$ = 1/EMC_CLK (see *LPC408x/7x User manual*).

[4] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[5] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[6] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

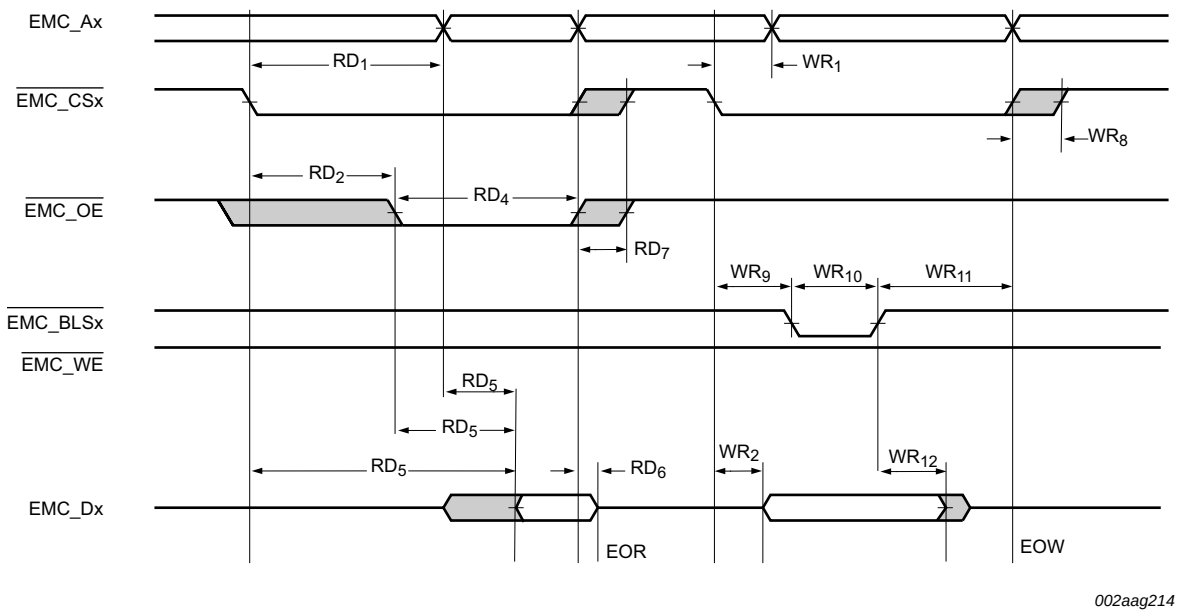


Fig 19. External static memory read/write access (PB = 0)

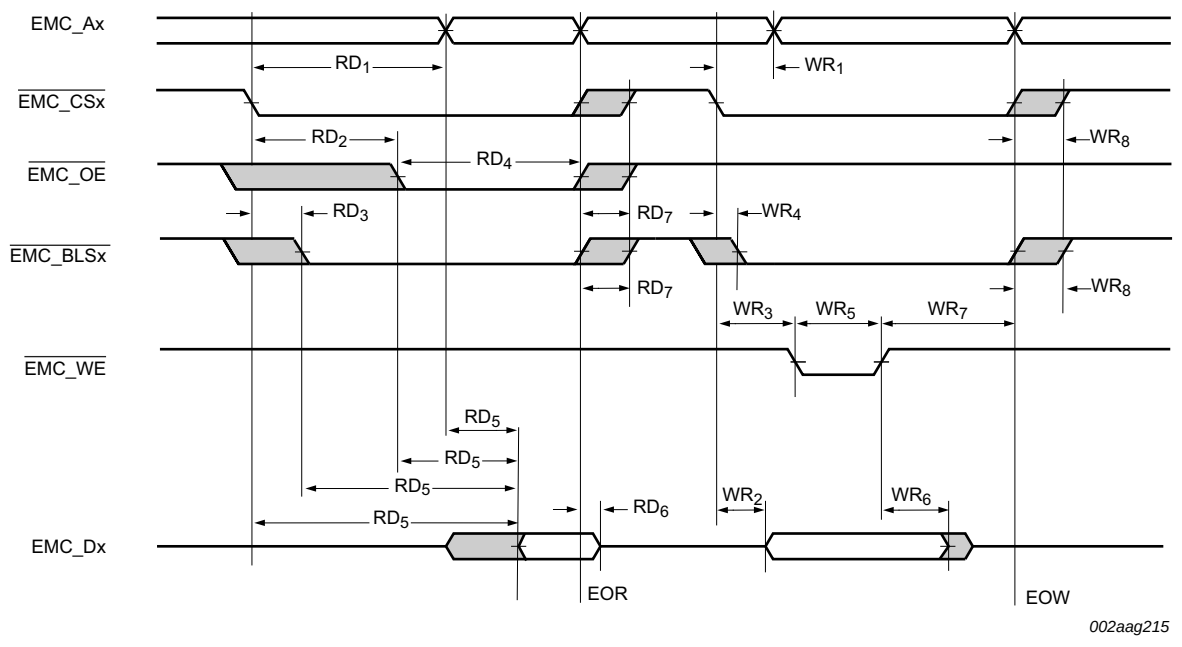


Fig 20. External static memory read/write access (PB =1)

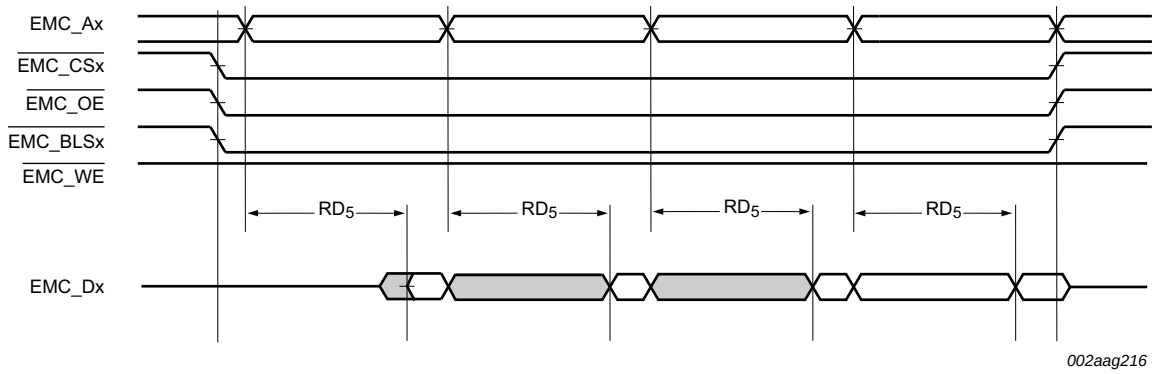


Fig 21. External static memory burst read cycle

Table 33. Comparator voltage ladder reference static characteristics
V_{DDA} = 3.3 V; T_{amb} = -40 °C to + 85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal V_{DDA} supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		–0.45	–0.5	–0.55	%
		decimal code = 16		–0.99	–1.1	–1.21	%
		decimal code = 24		–1.26	–1.4	–1.54	%
		decimal code = 30		–1.35	–1.5	–1.65	%
		decimal code = 31		–1.35	–1.5	–1.65	%
$E_{V(O)}$	output voltage error	External VDDCMP supply					
		decimal code = 00		0	0	0	%
		decimal code = 08		0.44	0.4	0.36	%
		decimal code = 16		–0.18	–0.2	–0.22	%
		decimal code = 24		–0.45	–0.5	–0.55	%
		decimal code = 30		–0.54	–0.6	–0.66	%
		decimal code = 31		–0.45	–0.5	–0.55	%

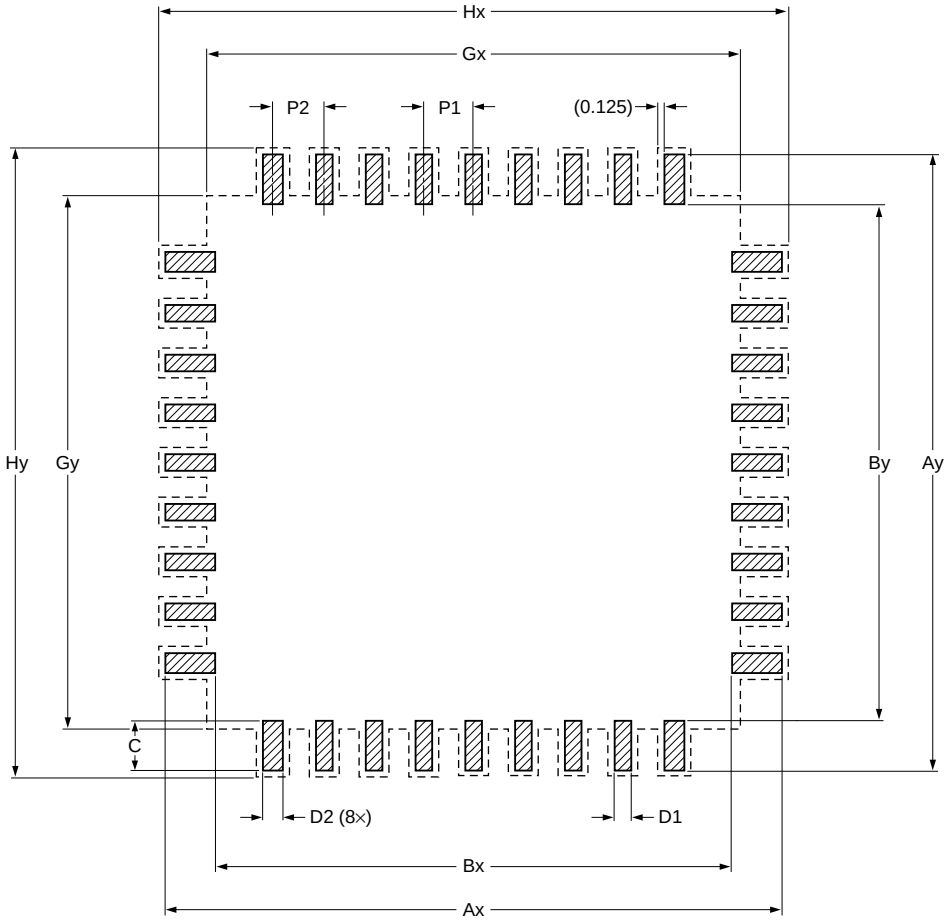
[1] Measured on typical silicon samples with a 2 kHz input signal and overdrive < 100 μV. Power switched off to all analog peripherals except the comparator.

13. Application information

13.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC4088 and LPC4078/76 and as device-only controller on parts LPC4074/72.

Footprint information for reflow soldering of LQFP80 package **SOT315-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	15.300	15.300	12.300	12.300	1.500	0.280	0.400	12.500	12.500	15.550	15.550

sot315-1_fr

Fig 56. Reflow soldering of the LQFP80 package