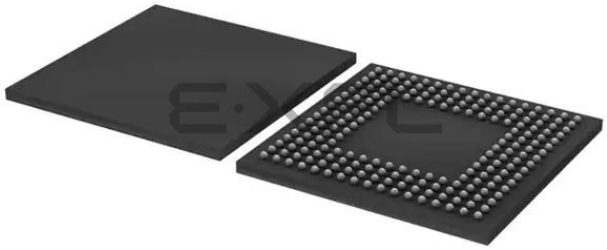

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4032 x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4088fet208-551

- Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
- Three SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
- Three enhanced I^2C-bus interfaces, one with a true open-drain output supporting the full I^2C-bus specification and Fast-mode Plus with data rates of 1 Mbit/s, two with standard port pins. Enhancements include multiple address recognition and monitor mode.
- I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- CAN controller with two channels.

- Digital peripherals:
  - SD/MMC memory card interface.
  - Up to 165 General Purpose I/O (GPIO) pins depending on the packaging, with configurable pull-up/down resistors, open-drain mode, and repeater mode. All GPIOs are located on an AHB bus for fast access and support Cortex-M4 bit-banding. GPIOs can be accessed by the General Purpose DMA Controller. Any pin of ports 0 and 2 can be used to generate an interrupt.
  - Two external interrupt inputs configurable as edge/level sensitive. All pins on port 0 and port 2 can be used as edge sensitive interrupt sources.
  - Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input. Specific timer events can be selected to generate DMA requests.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - Two standard PWM/timer blocks with external count input option.
  - One motor control PWM with support for three-phase motor control.
  - Real-Time Clock (RTC) with a separate power domain. The RTC is clocked by a dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers, allowing system status to be stored when the rest of the chip is powered off. Battery power can be supplied from a standard 3 V lithium button cell. The RTC will continue working when the battery voltage drops to as low as 2.1 V. An RTC interrupt can wake up the CPU from any reduced power mode.
  - Event Recorder that can capture the clock value when an event occurs on any of three inputs. The event identification and the time it occurred are stored in registers. The Event Recorder is located in the RTC power domain and can therefore operate as long as there is RTC power.
  - Windowed Watchdog Timer (WWDT). Windowed operation, dedicated internal oscillator, watchdog warning interrupt, and safety features.
  - CRC Engine block can calculate a CRC on supplied data using one of three standard polynomials. The CRC engine can be used in conjunction with the DMA controller to generate a CRC without CPU involvement in the data transfer.
- Analog peripherals:
  - 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 400 kHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.

- 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support.
- Two analog comparators.

- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
  - Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
  - Brownout detect with separate threshold for interrupt and forced reset.
  - On-chip Power-On Reset (POR).
- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1 % accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, LQFP144, TFBGA80, and LQFP80 package.

3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[10]	98	T15	L10	69	48	39	K9	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
										O	**U2_TXD —** Transmitter output for UART2.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[5] —** LCD data.
P0[11]	100	R14	P12	70	49	40	K10	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
										I	**U2_RXD —** Receiver input for UART2.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT1 —** Match output for Timer 3, channel 1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[10] —** LCD data.
P0[12]	41	R1	J4	29	-	-	-	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
										I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[20]	120	M17	K14	83	58	-	-	[3]	I; PU	I/O	**P0[20] —** General purpose digital input/output pin.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_CMD —** Command line for SD card interface.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[14] —** LCD data.
P0[21]	118	M16	K11	82	57	-	-	[3]	I; PU	I/O	**P0[21] —** General purpose digital input/output pin.
										I	**U1_RI —** Ring Indicator input for UART1.
										O	**SD_PWR —** Power Supply Enable for external SD card power supply.
										O	**U4_OE —** RS-485/EIA-485 output enable signal for UART4.
										I	**CAN_RD1 —** CAN1 receiver input.
										I/O	**U4_SCLK —** USART 4 clock input or output in synchronous mode.
P0[22]	116	N17	L14	80	56	44	H10	[6]	I; PU	I/O	**P0[22] —** General purpose digital input/output pin.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
										O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
										O	**CAN_TD1 —** CAN1 transmitter output.
										O	**SPIFI_CLK —** Clock output for SPIFI.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[9]	188	A6	D7	131	91	72	A4	[3]	I; PU	I/O	**P1[9] —** General purpose digital input/output pin.
										I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P1[10]	186	C8	A7	129	90	71	A5	[3]	I; PU	I/O	**P1[10] —** General purpose digital input/output pin.
										I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P1[11]	163	A14	A12	-	-	-	-	[3]	I; PU	I/O	**P1[11] —** General purpose digital input/output pin.
										I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
										I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]	157	A16	A14	-	-	-	-	[3]	I; PU	I/O	**P1[12] —** General purpose digital input/output pin.
										I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
										I/O	**SD_DAT[3] —** Data line 3 for SD card interface.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										-	**R —** Function reserved.
										O	**CMP1_OUT —** Comparator 1, output.
P1[13]	147	D16	D14	-	-	-	-	[3]	I; PU	I/O	**P1[13] —** General purpose digital input/output pin.
										I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P2[24]	53	P5	P1	-	-	-	-	[3]	I; PU	I/O	**P2[24] —** General purpose digital input/output pin.
										O	**EMC_CKE0 —** SDRAM clock enable 0.
P2[25]	54	R4	P2	-	-	-	-	[3]	I; PU	I/O	**P2[25] —** General purpose digital input/output pin.
										O	**EMC_CKE1 —** SDRAM clock enable 1.
P2[26]	57	T4	-	-	-	-	-	[3]	I; PU	I/O	**P2[26] —** General purpose digital input/output pin.
										O	**EMC_CKE2 —** SDRAM clock enable 2.
										I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P2[27]	47	P3	-	-	-	-	-	[3]	I; PU	I/O	**P2[27] —** General purpose digital input/output pin.
										O	**EMC_CKE3 —** SDRAM clock enable 3.
										I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
										O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P2[28]	49	P4	M2	-	-	-	-	[3]	I; PU	I/O	**P2[28] —** General purpose digital input/output pin.
										O	**EMC_DQM0 —** Data mask 0 used with SDRAM and static devices.
P2[29]	43	N3	L1	-	-	-	-	[3]	I; PU	I/O	**P2[29] —** General purpose digital input/output pin.
										O	**EMC_DQM1 —** Data mask 1 used with SDRAM and static devices.
P2[30]	31	L4	-	-	-	-	-	[3]	I; PU	I/O	**P2[30] —** General purpose digital input/output pin.
										O	**EMC_DQM2 —** Data mask 2 used with SDRAM and static devices.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT2 —** Match output for Timer 3, channel 2.

Table 4. LPC408x/7x memory usage and details

Address range	General Use	Address range details and description	
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 to 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)
		0x9000 0000 to 0x93FF FFFF	Static memory chip select 1 (up to 64 MB)
		0x9800 0000 to 0x9BFF FFFF	Static memory chip select 2 (up to 64 MB)
		0x9C00 0000 to 0x9FFF FFFF	Static memory chip select 3 (up to 64 MB)
		Four dynamic memory chip selects:	
		0xA000 0000 to 0xAFFF FFFF	Dynamic memory chip select 0 (up to 256 MB)
		0xB000 0000 to 0xBFFF FFFF	Dynamic memory chip select 1 (up to 256 MB)
		0xC000 0000 to 0xCFFF FFFF	Dynamic memory chip select 2 (up to 256 MB)
		0xD000 0000 to 0xDFFF FFFF	Dynamic memory chip select 3 (up to 256 MB)
0xE000 0000 to 0xE00F FFFF	Cortex-M4 Private Peripheral Bus	0xE000 0000 to 0xE00F FFFF	Cortex-M4 related functions, includes the NVIC and System Tick Timer.

The LPC408x/7x incorporate several distinct memory regions, shown in the following figures. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

7.9 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.9.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC408x/7x, the NVIC supports 40 vectored interrupts.
- 32 programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.9.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on port 0 and port 2 regardless of the selected function can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

7.10 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupts being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

7.11 External Memory Controller (EMC)

Remark: The EMC is available for parts LPC4088/78/76. Supported memory size and type and EMC bus width vary for different packages (see Table 2). The EMC pin configuration for each part is shown in Table 5.

Table 5. External memory controller pin configuration

Parts	Data bus pins	Address bus pins	Control pins	
			SRAM	**SDRAM**
LPC4088FBD208 LPC4088FET208 LPC4078FBD208 LPC4078FET208	EMC_D[31:0]	EMC_A[25:0]	$\overline{\text{EMC\_BLS}}$[3:0], $\overline{\text{EMC\_CS}}$[3:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC4088FET180 LPC4078FET180 LPC4076FET180	EMC_D[15:0]	EMC_A[19:0]	$\overline{\text{EMC\_BLS}}$[1:0], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	$\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_DYCS}}$[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC4088FBD144 LPC4078FBD144 LPC4076FBD144	EMC_D[7:0]	EMC_A[15:0]	$\overline{\text{EMC\_BLS}}$[3:2], $\overline{\text{EMC\_CS}}$[1:0], $\overline{\text{EMC\_OE}}$, $\overline{\text{EMC\_WE}}$	not available

The LPC408x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

7.11.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.12 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.12.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.

- Buffered output.
- Power-down mode.
- Selectable output drive.
- Dedicated conversion timer.
- DMA support.

7.21 Comparator

Remark: The comparator is available on parts LPC4088/7876.

Two embedded comparators are available to compare the voltage levels on external pins or against internal voltages. Up to four voltages on external pins and several internal reference voltages are selectable on each comparator. Additionally, two of the external inputs can be selected to drive an input common on both comparators.

7.21.1 Features

- Up to five selectable external sources per comparator; fully configurable on either positive or negative comparator input channels.
- 0.9 V internal band gap reference voltage selectable as either positive or negative input on each comparator.
- 32-stage voltage ladder internal reference for selectable voltages on each comparator; configurable on either positive or negative comparator input.
- Voltage ladder source voltage is selectable from an external pin or the 3.3 V analog voltage supply.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Relaxation oscillator circuitry output, for a 555 style timer operation.
- Individual comparator outputs can be connected to I/O pins.
- Separate interrupt for each comparator.
- Edge and level comparator outputs connect to two timers allowing edge counting while a level match has been asserted or measuring the time between two voltage trip points.

7.22 UART0/1/2/3 and USART4

Remark: UART0/1/2/3 are available on all parts. USART4 is available on parts LPC4088/78/76.

The LPC408x/7x contain five UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.22.1 Features

- Maximum UART data bit rate of 7.5 MBit/s.

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto-baud capability.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode and multiprocessor addressing.
- All UARTs have DMA support for both transmit and receive.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- USART4 includes an IrDA mode to support infrared communication.
- USART4 supports synchronous mode and a smart card mode conforming to ISO7816-3.

7.23 SPIFI

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M4 processor with little performance penalty compared to parallel flash devices with higher pin count.

The entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels.

SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.23.1 Features

- Quad SPI Flash Interface (SPIFI) interface to external flash.
- Transfer rates of up to SPIFI_CLK/2 bytes per second.
- Code in the serial flash memory can be executed as if it was in the CPU's internal memory space. This is accomplished by mapping the external flash memory directly into the CPU memory space.
- Supports 1-, 2-, and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Supported by a driver library available from NXP Semiconductors.

7.24 SSP serial I/O controller

The LPC408x/7x contain three SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

The I^2S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I^2S connection has one master, which is always the master, and one slave. The I^2S interface on the LPC408x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.26.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I^2S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S input and I^2S output.

7.27 CAN controller and acceptance filters

The LPC408x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.27.1 Features

- Dual-channel CAN controller and bus.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[15][16] [17]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.45$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.45	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[18]	-	-	−50	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[18]	-	-	60	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[19]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[20]	-	-	±10	µA
V_{BUS}	bus supply voltage		[20]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[20]	0.2	-	-	V

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{CM}	differential common mode voltage range	includes V_{DI} range	[20]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[20]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	[20]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	[20]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[20]	-	-	20	pF
Oscillator pins (see Section 13.2)							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	-	3.6	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD((3V3)}$ ≤ 3.6 V. Guaranteed by design.

[3] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[5] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[6] Boost control bits in the PBOOST register set to 0x0 (see *LPC408x/7x User manual*).

[7] Boost control bits in the PBOOST register set to 0x3 (see *LPC408x/7x User manual*).

[8] IRC running at 12 MHz; main oscillator and PLL disabled; PCLK = CCLK/4.

[9] BOD disabled.

[10] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 0; T_{amb} = 25 °C.

[11] On pin VBAT; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[12] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[13] V_{DDA} = 3.3 V; T_{amb} = 25 °C.

[14] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[15] Including voltage on outputs in 3-state mode.

[16] $V_{DD(3V3)}$ supply voltages must be present.

[17] 3-state outputs go into 3-state mode in Deep power-down mode.

[18] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[19] To V_{SS}.

[20] 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

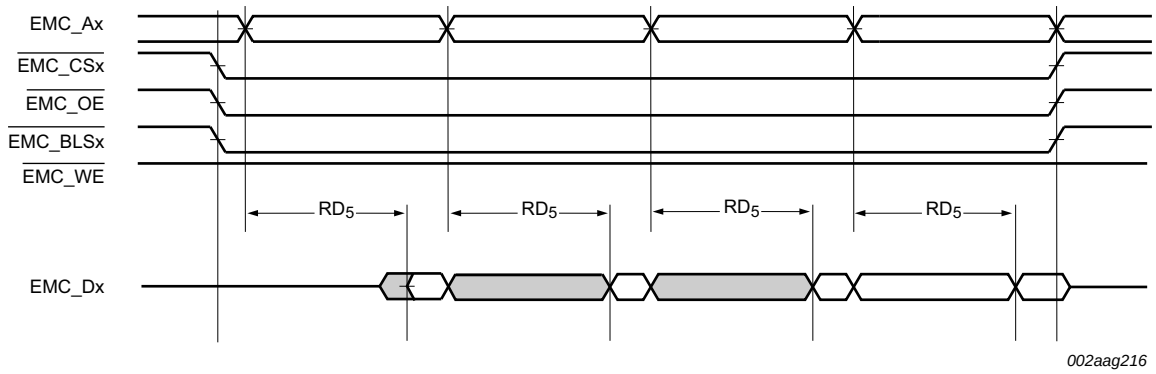


Fig 21. External static memory burst read cycle

11.3 External clock

Table 19. Dynamic characteristic: external clock (see Figure 40)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency	1	-	25	MHz
$T_{cy(clk)}$	clock cycle time	40	-	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

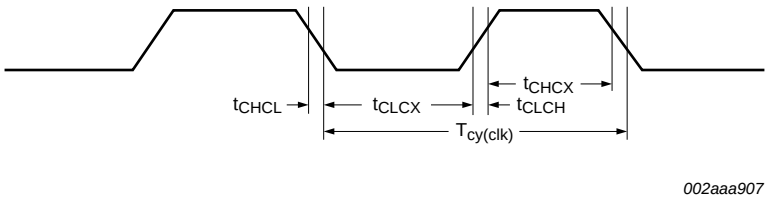


Fig 23. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Internal oscillators

Table 20. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	11.88	12	12.12	MHz
$f_{i(RTC)}$	RTC input frequency	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 I/O pins

Table 21. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pin. For details, see the LPC408x/7x IBIS model available on the NXP website.

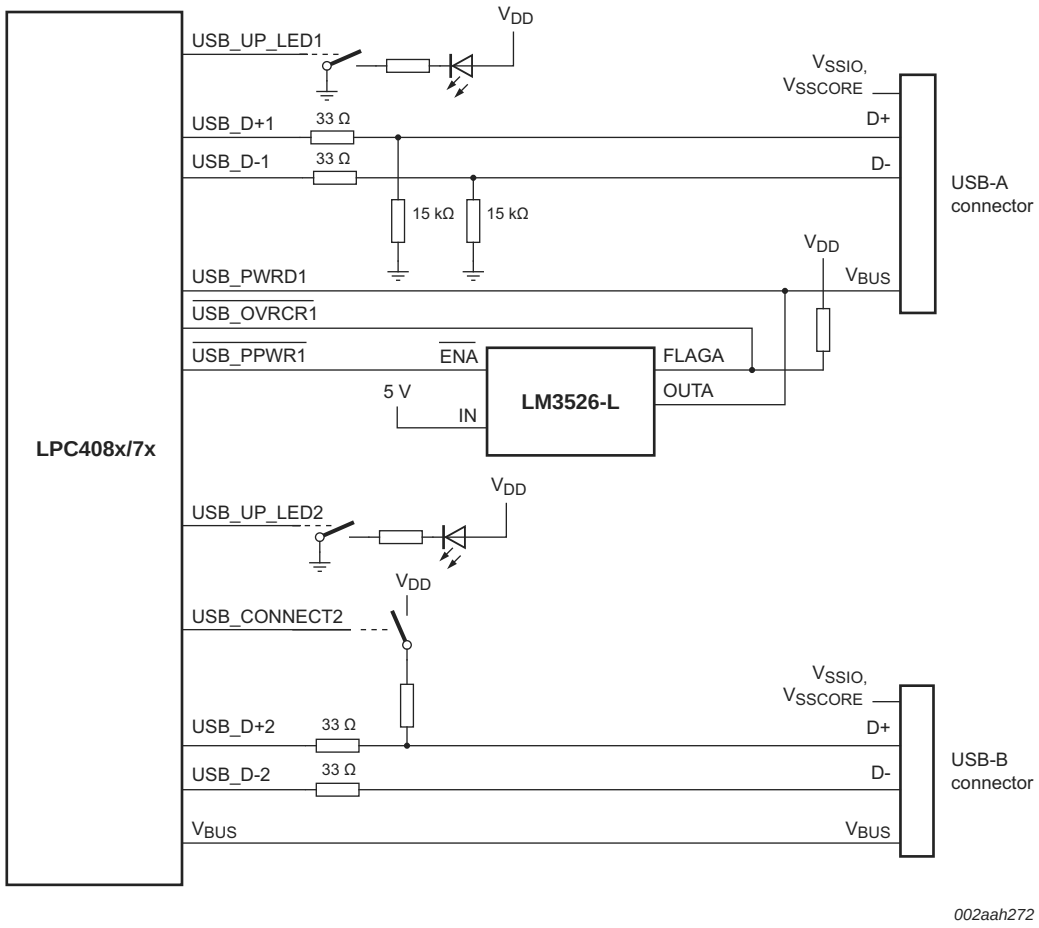


Fig 39. USB device port configuration: port 1 host and port 2 device

13.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

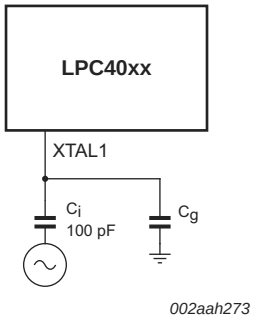


Fig 40. Slave mode operation of the on-chip oscillator

To eliminate the loss of time counts in the RTC due to voltage swing or ramp rate of the $\overline{\text{RESET}}$ signal, connect an RC filter between the $\overline{\text{RESET}}$ pin and the external reset input.

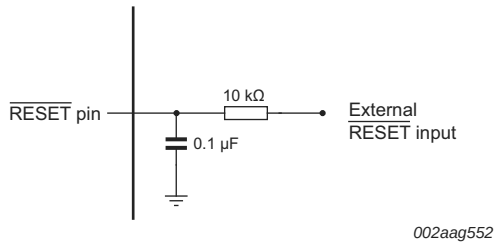
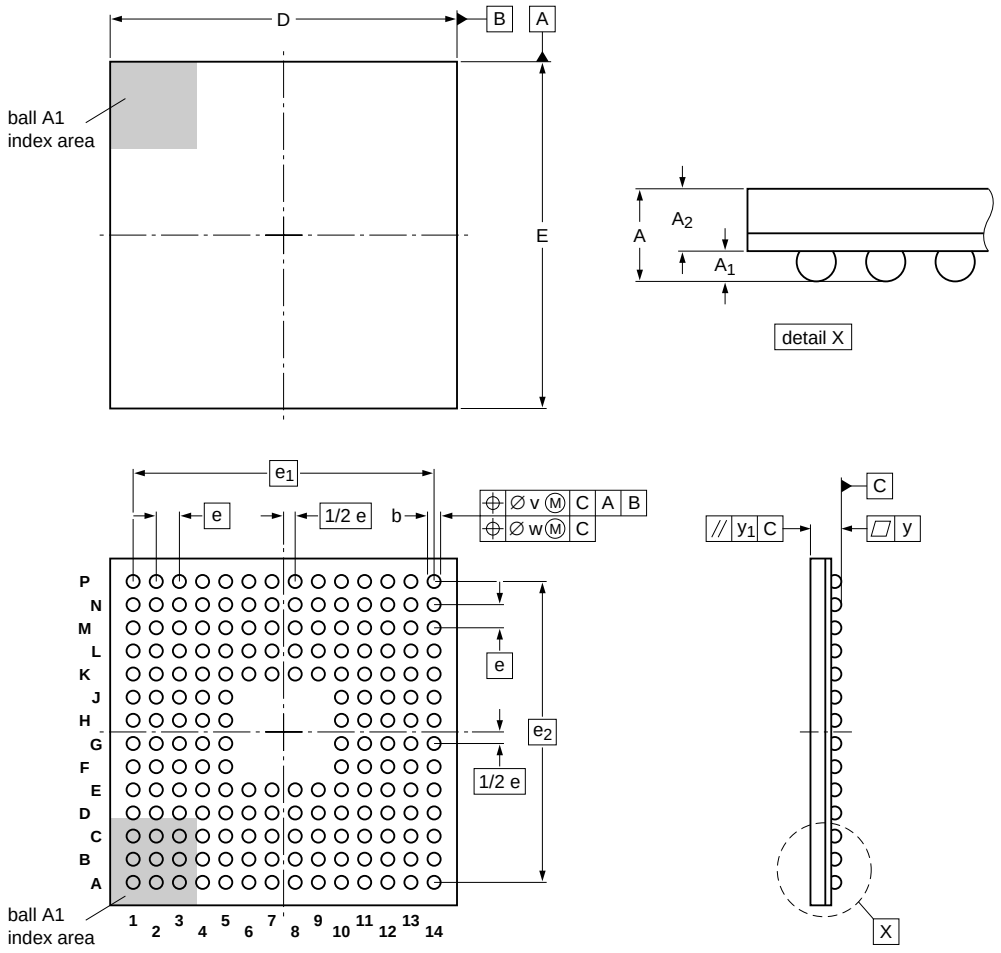


Fig 44. Reset input with RC filter

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



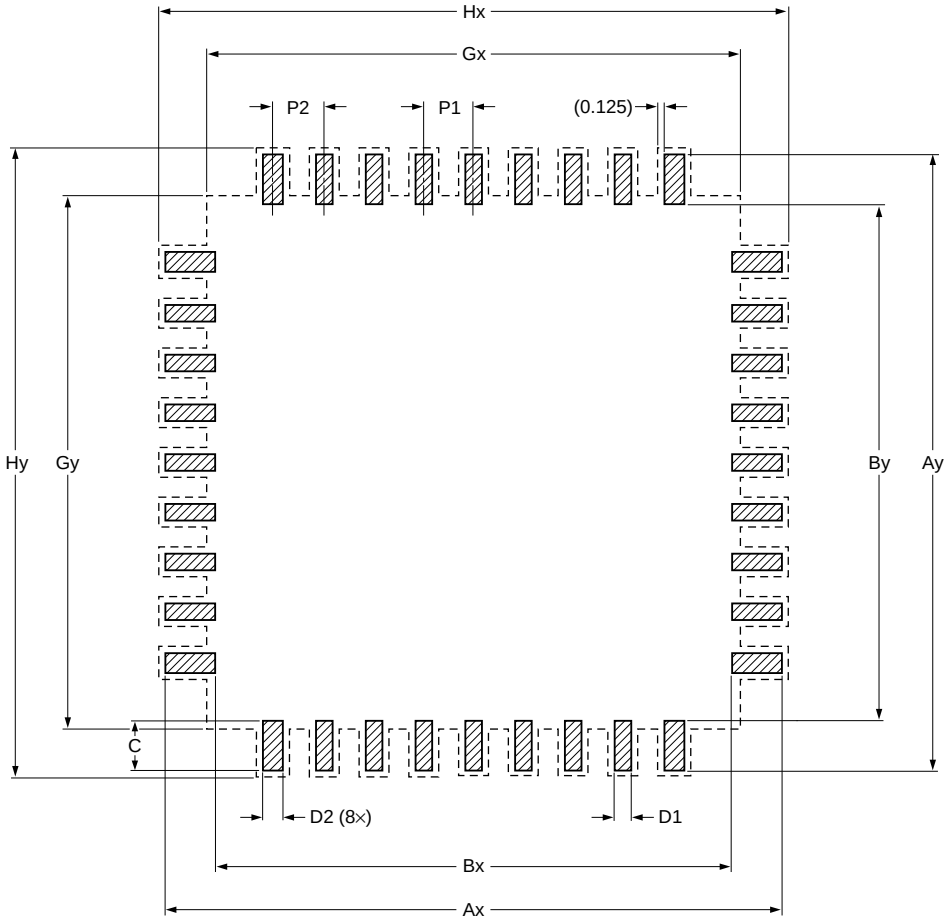
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 47. Package outline SOT570-3 (TFBGA180)

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 55. Reflow soldering of the LQFP100 package