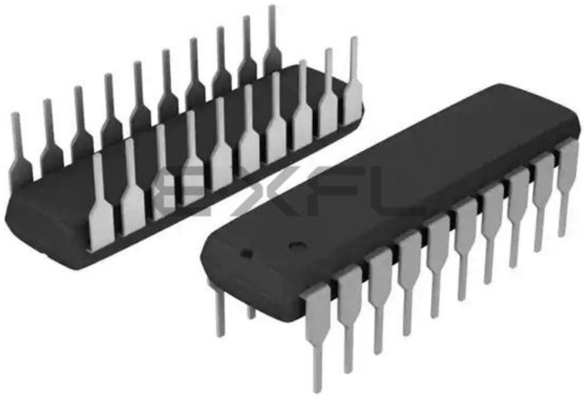


Welcome to E-XFL.COM

Understanding Embedded - PLDs (Programmable Logic Devices)

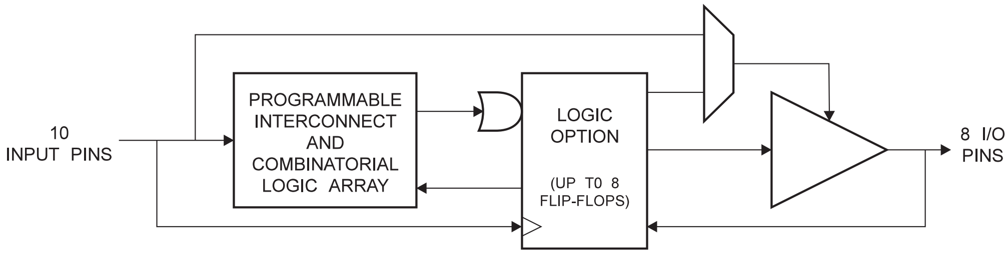
Embedded - PLDs, or Programmable Logic Devices, are a type of digital electronic component used to build reconfigurable digital circuits. Unlike fixed-function logic devices, PLDs can be programmed to perform specific functions by the user. This flexibility allows designers to customize the logic to meet the exact needs of their applications, making PLDs a crucial component in modern embedded systems.

Applications of Embedded - PLDs (Programmable Logic Devices)

The versatility of PLDs makes them suitable for a wide range of applications. In consumer electronics, PLDs are used to enhance the functionality and performance of

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Number of Macrocells	8
Voltage - Input	5V
Speed	12 ns
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf16v8cz-12pc

Figure 1-1. Block Diagram



2. Pin Configuration and Pinouts

Table 2-1. Pinouts - All Pinouts Top View

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bi-directional Buffers
$\overline{OE}$	Output Enable
VCC	+5V Supply

Figure 2-1. TSSOP

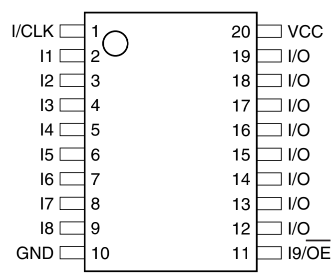


Figure 2-2. DIP/SOIC

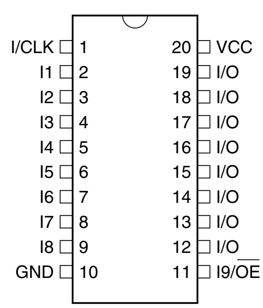
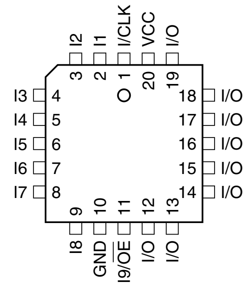


Figure 2-3. PLCC



3. Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V[1]
Programming Voltage with Respect to Ground	-2.0V to +14.0V[1]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

4. DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5V ±5%	5V ±10%

4.1 DC Characteristics

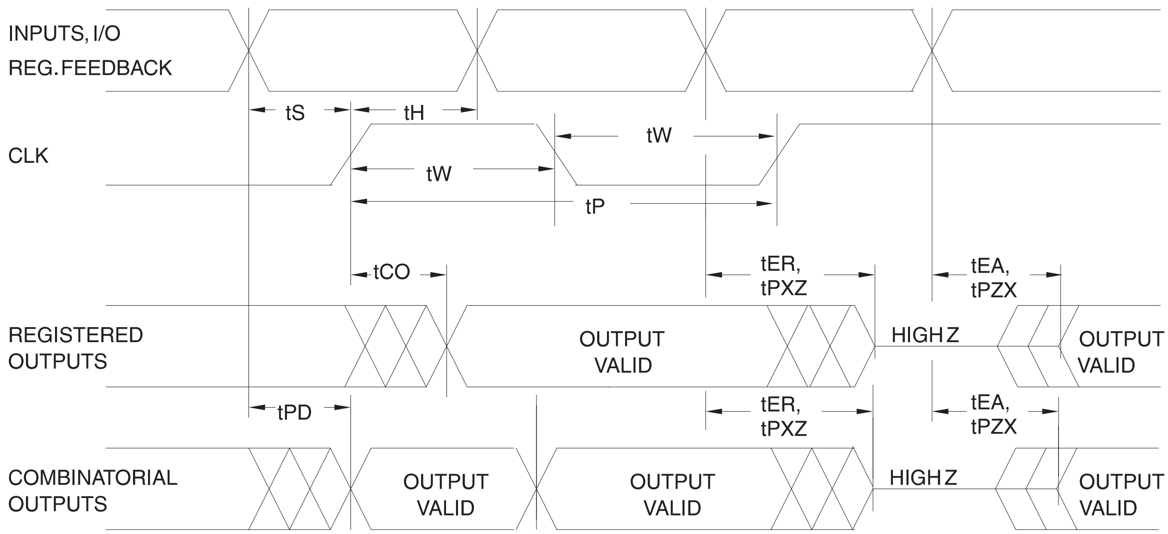
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(Max)				-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$				10	µA
I_{CC1}	Power Supply Current	15 MHz, V_{CC} = Max, V_{IN} = 0, V_{CC}, Outputs Open	Com			95	mA
			Ind.			105	mA
I_{CC}[1]	Power Supply Current, Standby Mode	0 MHz, V_{CC} = Max, V_{IN} = 0, V_{CC}, Outputs Open	Com.		5		µA
			Ind		5		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V; V_{CC}= 5V; TA = 25°C				-150	mA
V_{IL}	Input Low Voltage	Min < V_{CC} < Max		-0.5		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage	V_{CC} = Min, All Outputs I_{OL} = -16 mA	Com, Ind.			0.5	V

4.1 DC Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} = Min I_{OL} = -3.2 mA		2.4			V
I_{OL}	Output Low Current	V_{CC} = Min	Com.	24			mA
			Ind.	12			
I_{OH}	Output High Current	V_{CC} = Min	Com., Ind.	4			mA

Note: 1. All I_{CC} parameters measured with outputs open. Data is based on Atmel test patterns. Reading may vary with pattern.

4.2 AC Waveforms[1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

4.3 AC Characteristics

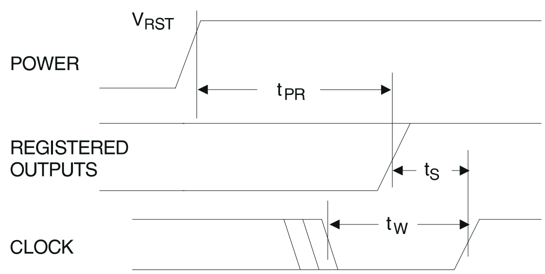
Symbol	Parameter	-12		-15		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-registered Output	3	12	3	15	ns
t_{CF}	Clock to Feedback		6		8	ns
t_{CO}	Clock to Output	2	8	2	10	ns
t_S	Input or Feedback Setup Time	10		12		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	12		16		ns
t_W	Clock Width	6		8		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$		55		45	MHz
	Internal Feedback $1/(t_S + t_{CF})$		62		50	MHz
	No Feedback $1/(t_P)$		83		62	MHz
t_{EA}	Input to Output Enable – Product Term	3	12	3	15	ns
t_{ER}	Input to Output Disable – Product Term	2	15	2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable	2	12	2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable	1.5	12	1.5	15	ns

4.5 Power-up Reset

The ATF16V8CZ's registers are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic, from below 0.7V,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

4.6 Preload of Registered Outputs

The ATF16V8CZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by approved programmers.

5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8CZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

6. Input and I/O Pin-keeper Circuits

The ATF16V8CZ contains internal input and I/O pin-keeper circuits. These circuits allow each ATF16V8CZ pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 µA.

Figure 6-1. Input Diagram

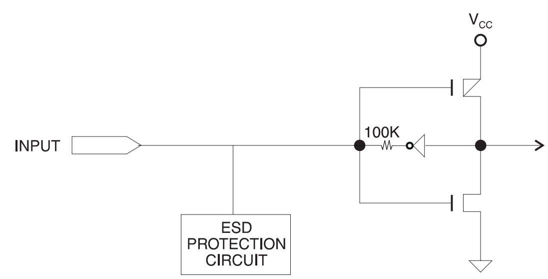


Figure 6-2. I/O Diagram

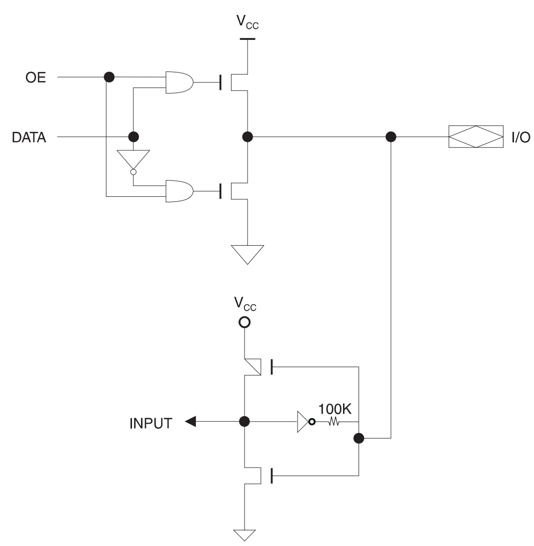
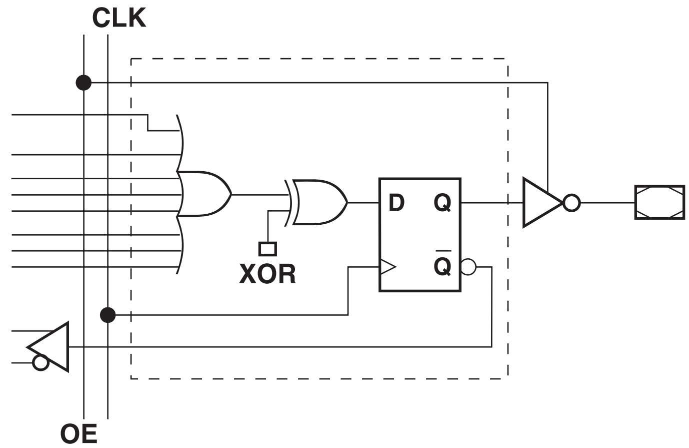


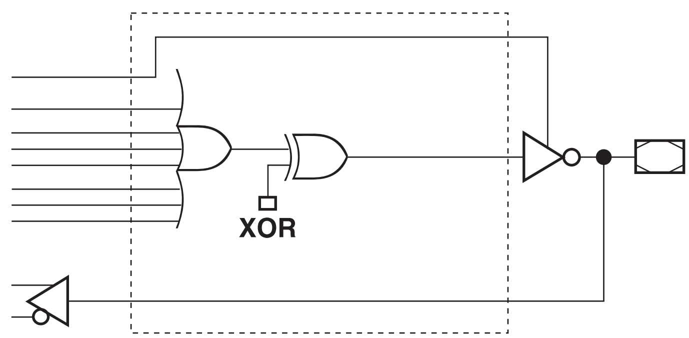
Figure 8-1. Registered Configuration for Registered Mode[(1)(2)]



Notes: 1. Pin 1 controls common CLK for the registered outputs.
Pin 11 controls common $\overline{OE}$ for the registered outputs.
Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.

2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 8-2. Combinatorial Configuration for Registered Mode[(1)(2)]



Notes: 1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.

2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 8-3. Registered Mode Logic Diagram

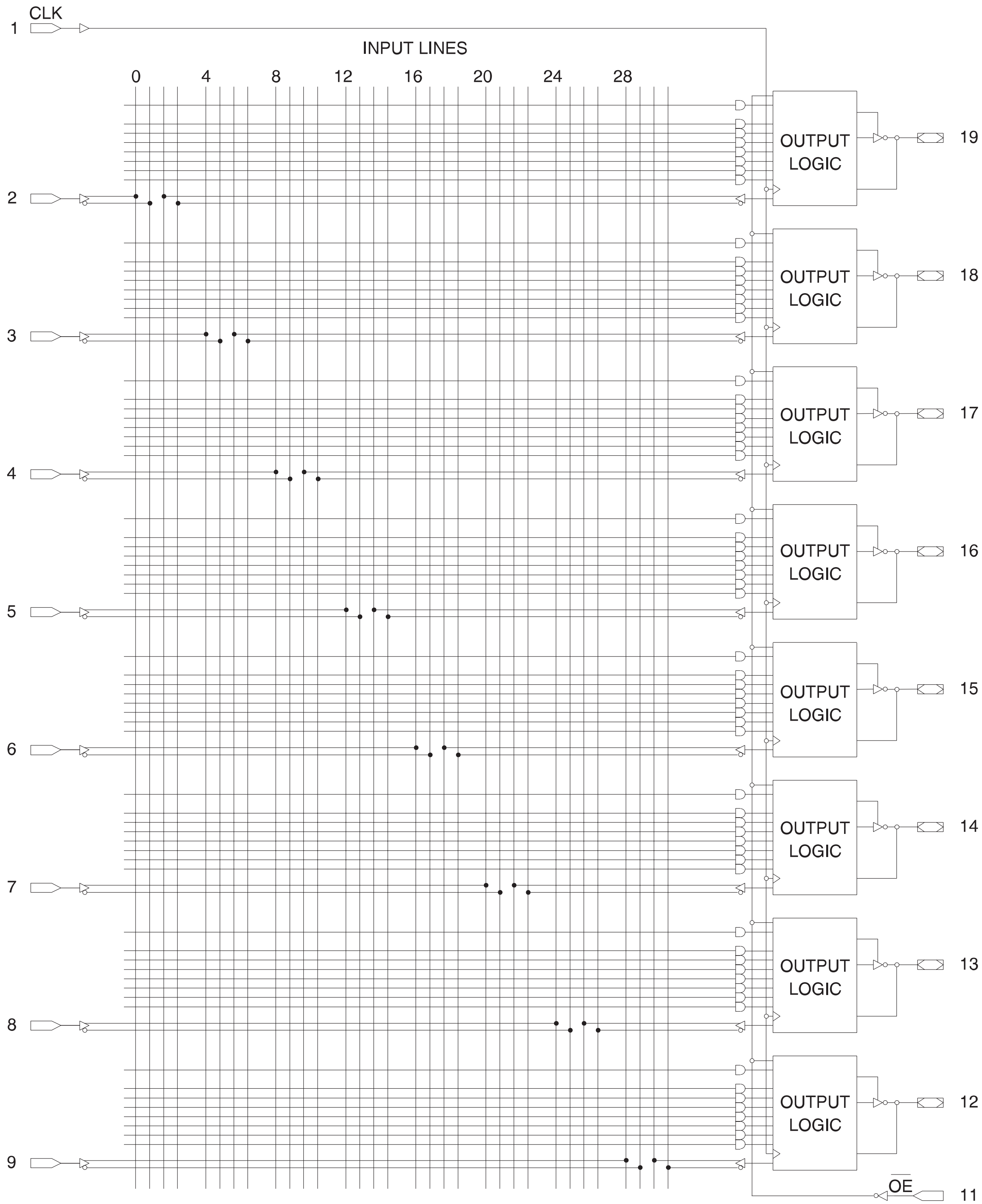


Figure 9-2. Complex Mode Logic Diagram

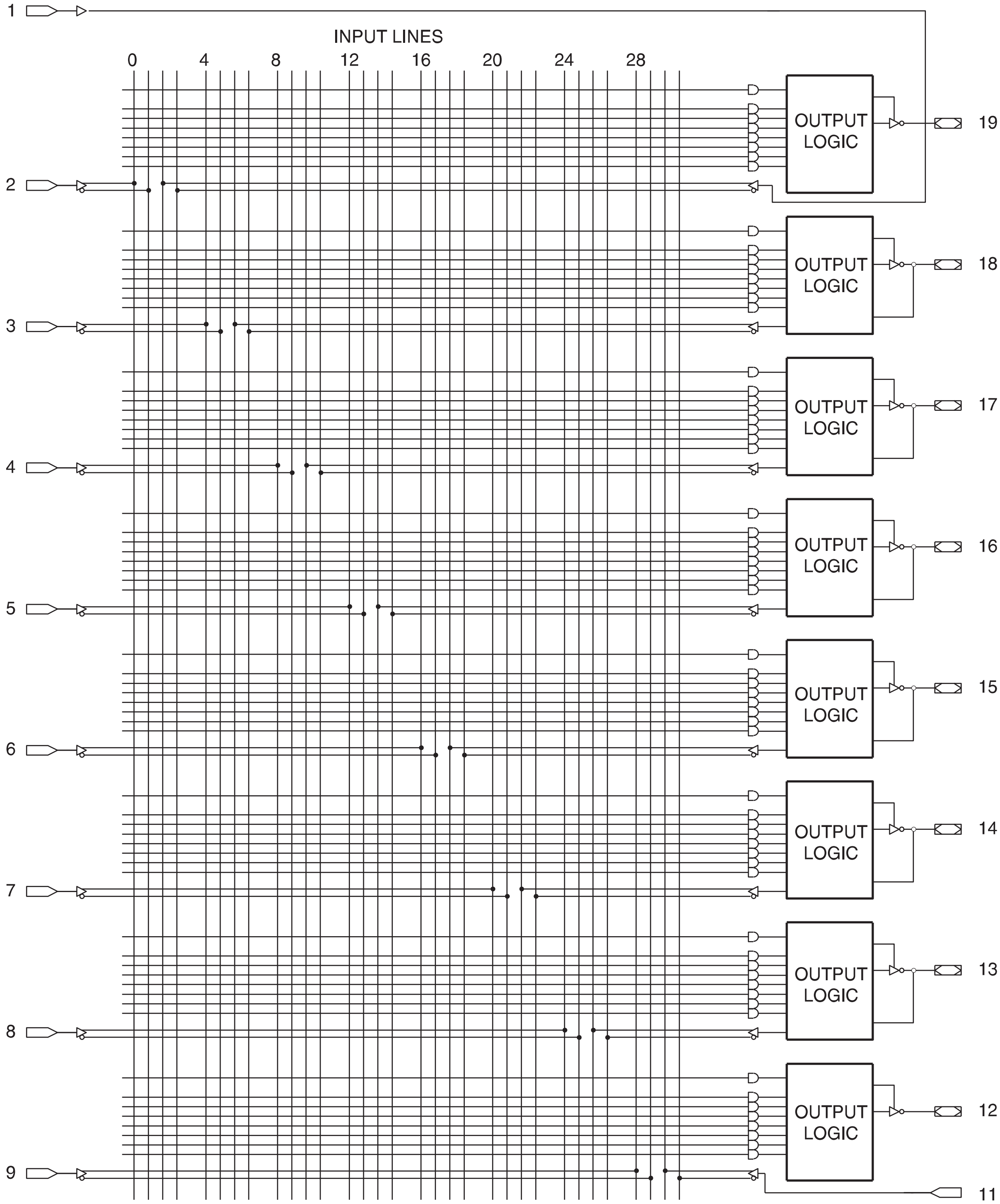
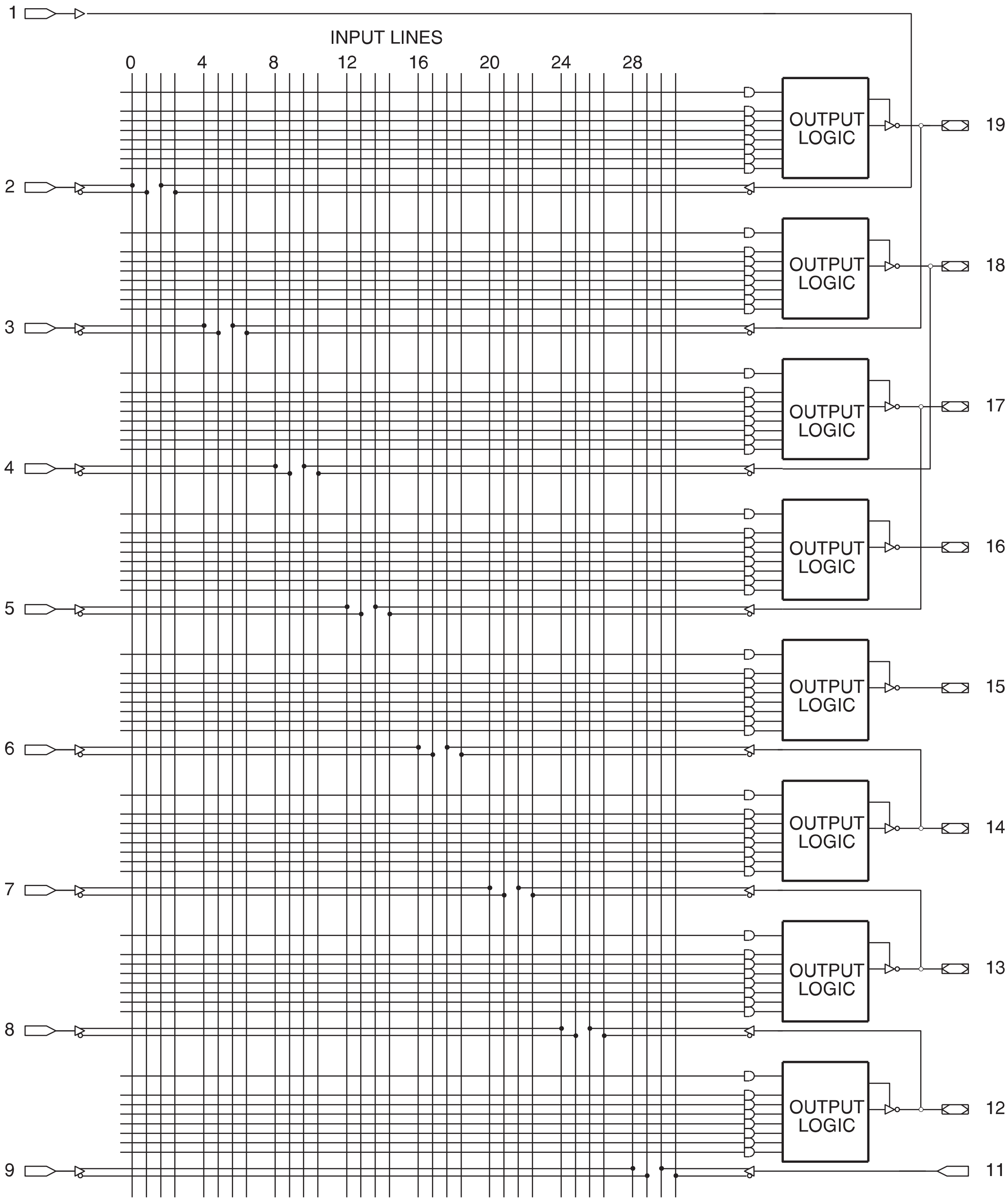
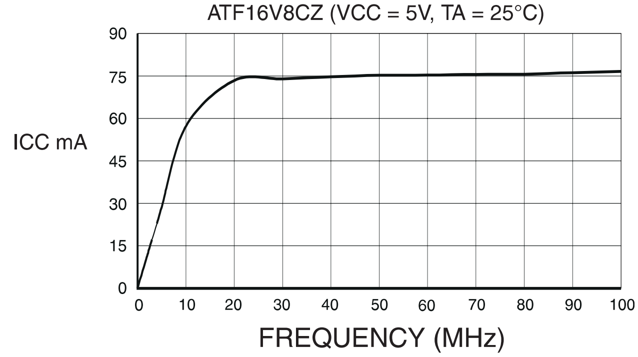


Figure 9-3. Simple Mode Logic Diagram

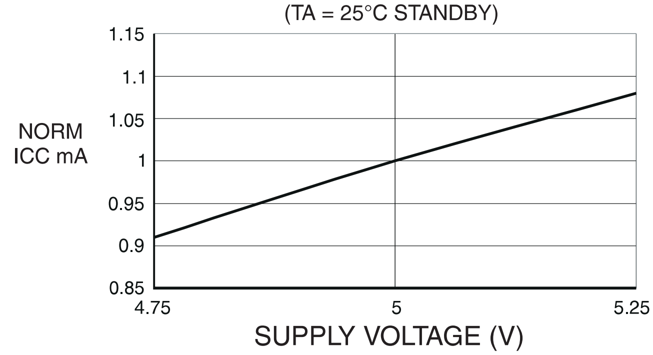


9.1 Test Characterization Data

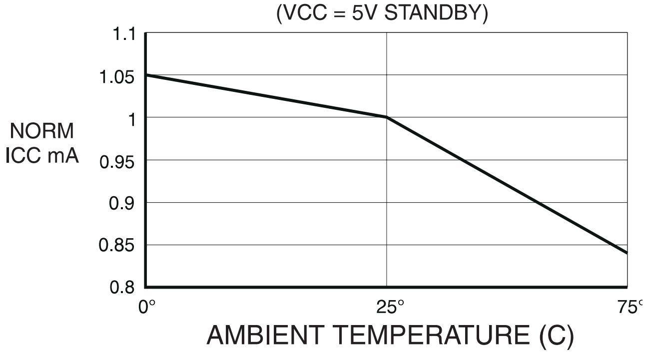
SUPPLY CURRENT
VS. INPUT FREQUENCY
ATF16V8CZ (VCC = 5V, TA = 25°C)



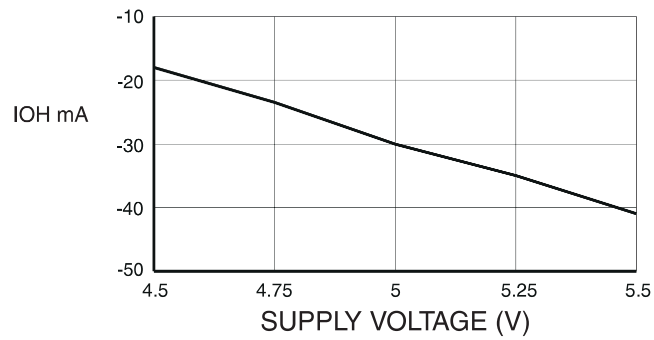
NORMALIZED SUPPLY CURRENT
VS. SUPPLY VOLTAGE
(TA = 25°C STANDBY)



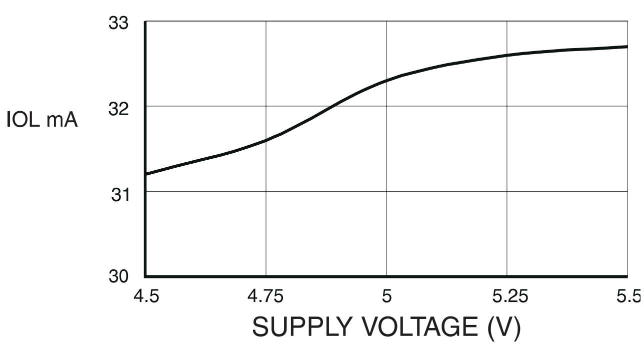
NORMALIZED SUPPLY CURRENT
VS. AMBIENT TEMPERATURE
(VCC = 5V STANDBY)



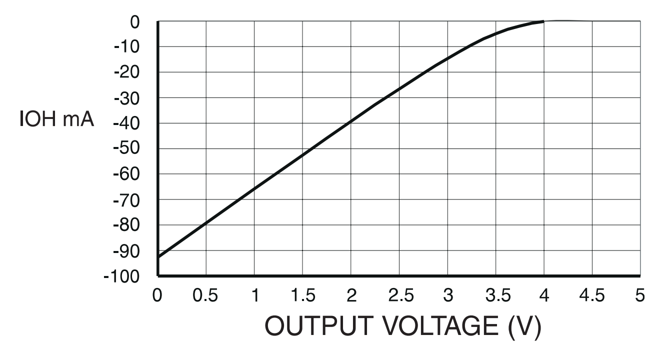
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (VOH = 2.4V, TA = 25°C)



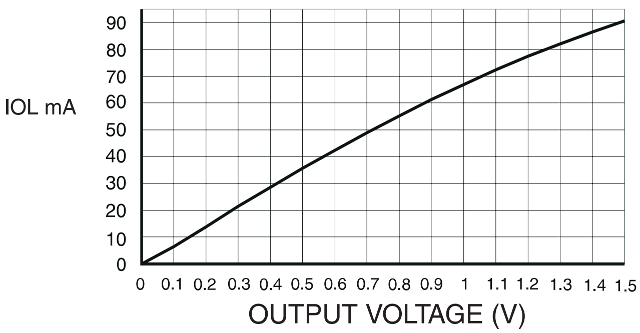
OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE (TA = 25°C, VOL = 0.45V)



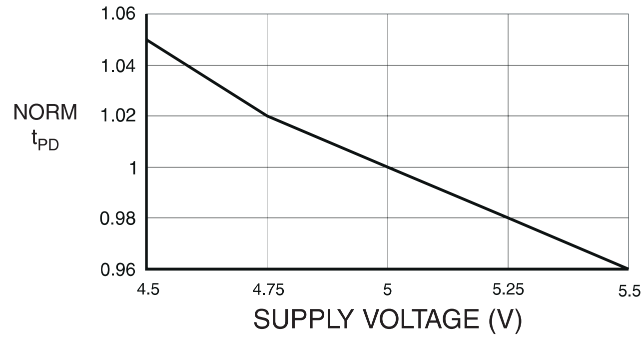
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE (VOH = 2.4V, TA = 25°C)



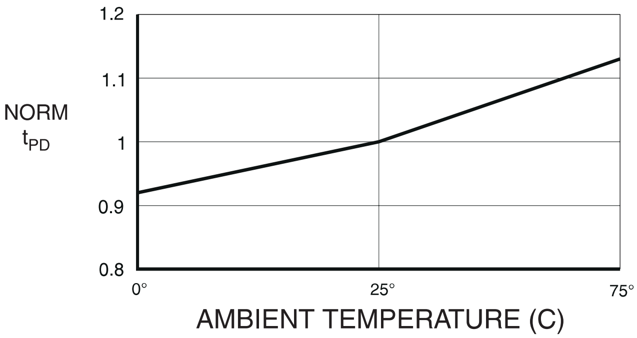
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



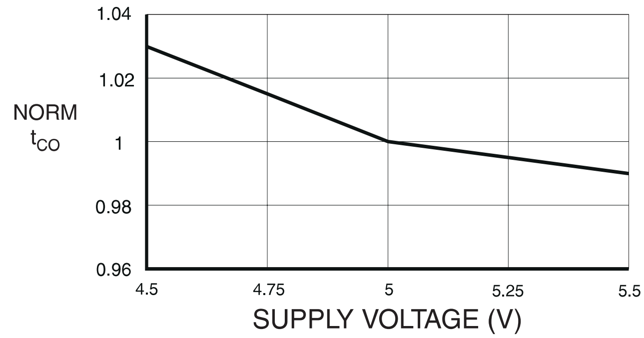
NORMALIZED t_{PD}
VS. SUPPLY VOLTAGE (TA = 25°C)



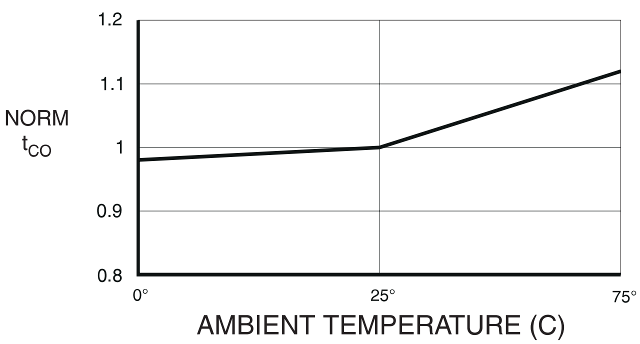
NORMALIZED t_{PD}
VS. AMBIENT TEMPERATURE (TA = 25°C)



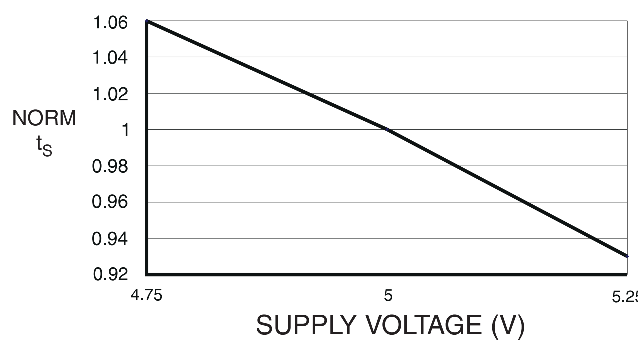
NORMALIZED t_{CO}
VS. SUPPLY VOLTAGE (TA = 25°C)

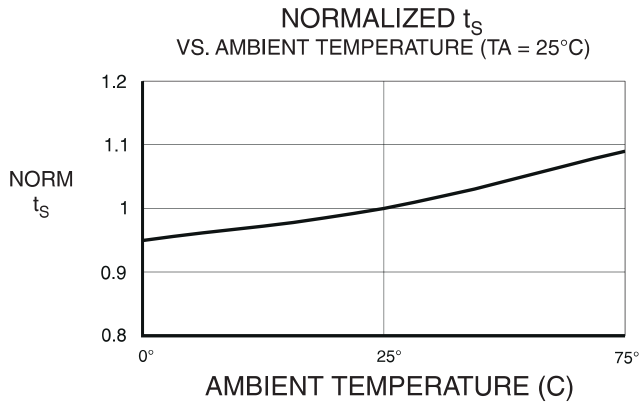


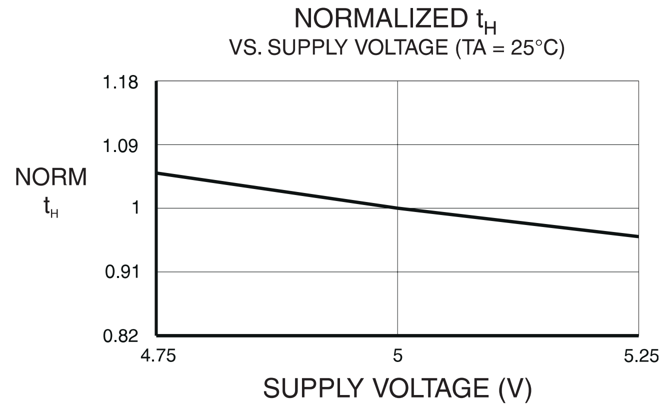
NORMALIZED t_{CO}
VS. AMBIENT TEMPERATURE (VCC = 5V)

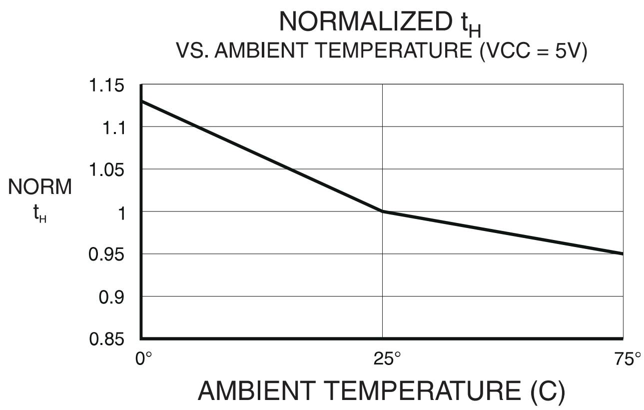


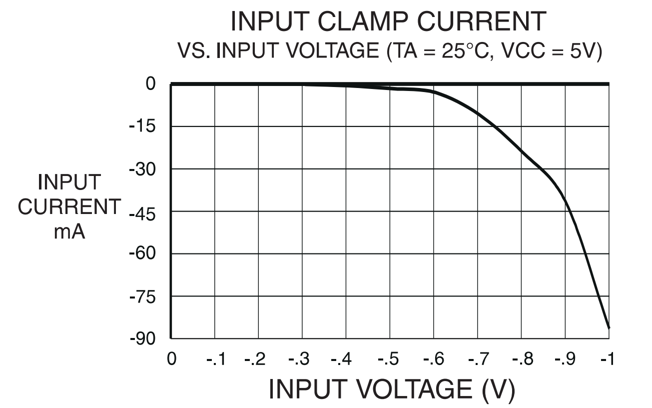
NORMALIZED t_S
VS. SUPPLY VOLTAGE (TA = 25C)

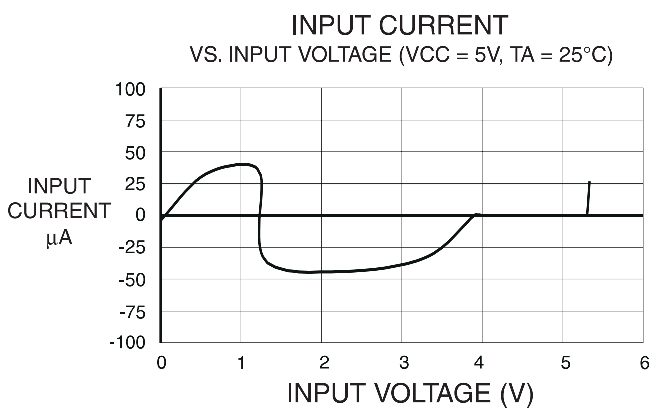



NORMALIZED tS
VS. AMBIENT TEMPERATURE (TA = 25°C)
1.2
1.1
1
0.9
0.8
NORM
tS
0°
25°
75°
AMBIENT TEMPERATURE (C)


NORMALIZED tH
VS. SUPPLY VOLTAGE (TA = 25°C)
1.18
1.09
1
0.91
0.82
NORM
tH
4.75
5
5.25
SUPPLY VOLTAGE (V)


NORMALIZED tH
VS. AMBIENT TEMPERATURE (VCC = 5V)
1.15
1.1
1.05
1
0.95
0.9
0.85
NORM
tH
0°
25°
75°
AMBIENT TEMPERATURE (C)


INPUT CLAMP CURRENT
VS. INPUT VOLTAGE (TA = 25°C, VCC = 5V)
0
-15
-30
-45
-60
-75
-90
INPUT
CURRENT
mA
0
-.1
-.2
-.3
-.4
-.5
-.6
-.7
-.8
-.9
-1
INPUT VOLTAGE (V)


INPUT CURRENT
VS. INPUT VOLTAGE (VCC = 5V, TA = 25°C)
100
75
50
25
0
-25
-50
-75
-100
INPUT
CURRENT
µA
0
1
2
3
4
5
6
INPUT VOLTAGE (V)

10. Ordering Information

10.1 Standard Package Options

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
12	10	8	ATF16V8CZ-12JC	20J	Commercial (0°C to 70°C)
			ATF16V8CZ-12PC	20P3	
			ATF16V8CZ-12SC	20S	
			ATF16V8CZ-12XC	20X	
15	12	10	ATF16V8CZ-15JC	20J	Commercial (0°C to 70°C)
			ATF16V8CZ-15PC	20P3	
			ATF16V8CZ-15SC	20S	
			ATF16V8CZ-15XC	20X	
	12	10	ATF16V8CZ-15JI	20J	Industrial (-40°C to 85°C)
			ATF16V8CZ-15PI	20P3	
			ATF16V8CZ-15SI	20S	
			ATF16V8CZ-15XI	20X	

Note: Shaded parts are being obsoleted in Q3-05 and being replaced by Green parts.

10.2 Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

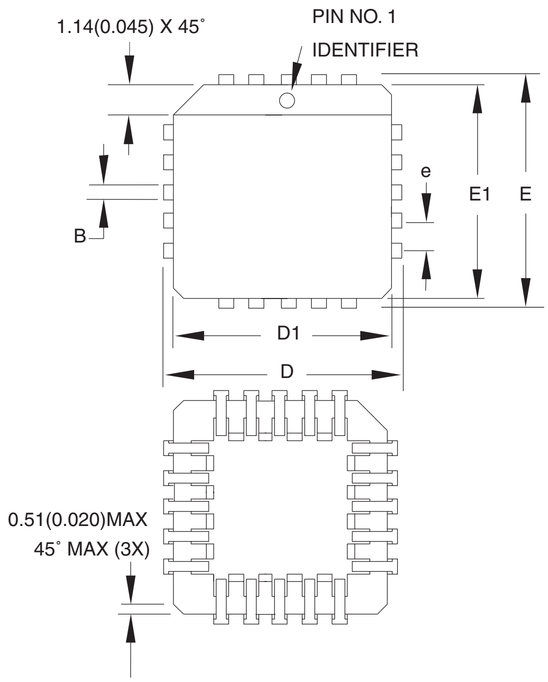
10.3 Green Package Options (Pb/Halide-free/RoHS Compliant)

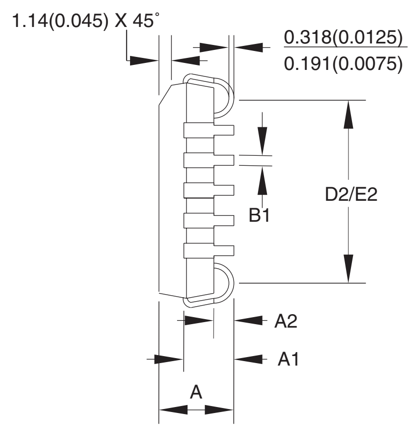
t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	12	10	ATF16V8CZ-15JU	20J	Industrial (-40°C to 85°C)
			ATF16V8CZ-15PU	20P3	
			ATF16V8CZ-15SU	20S	
			ATF16V8CZ-15XU	20X	

Package Type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-wing Small Outline (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

11. Package Information

11.1 20J – PLCC





COMMON DIMENSIONS
(Unit of Measure = mm)

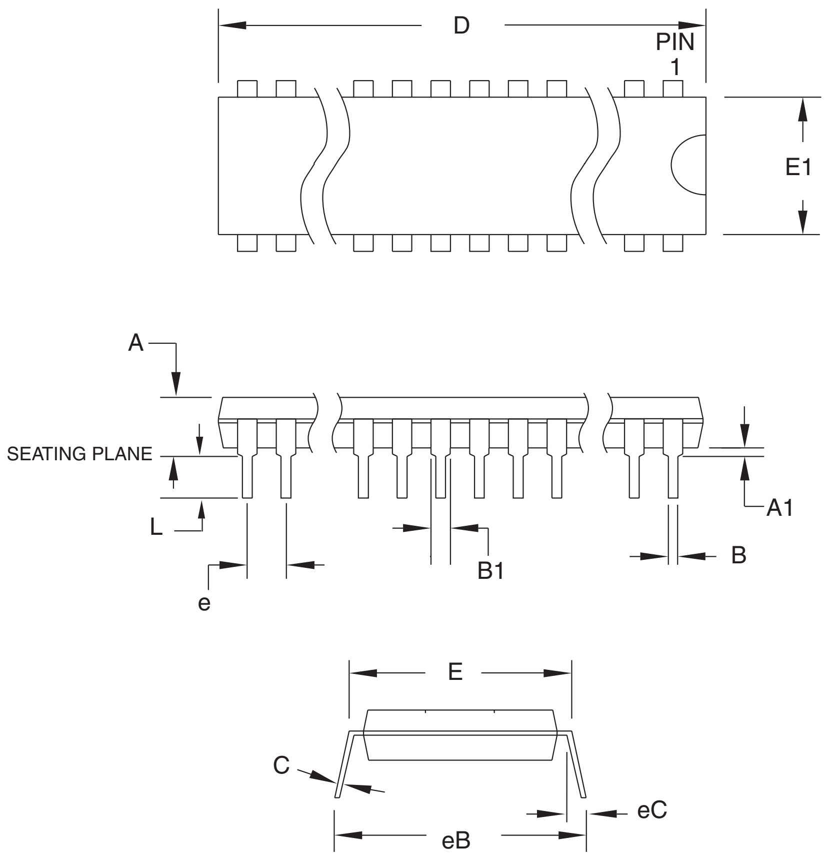
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

11.2 20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

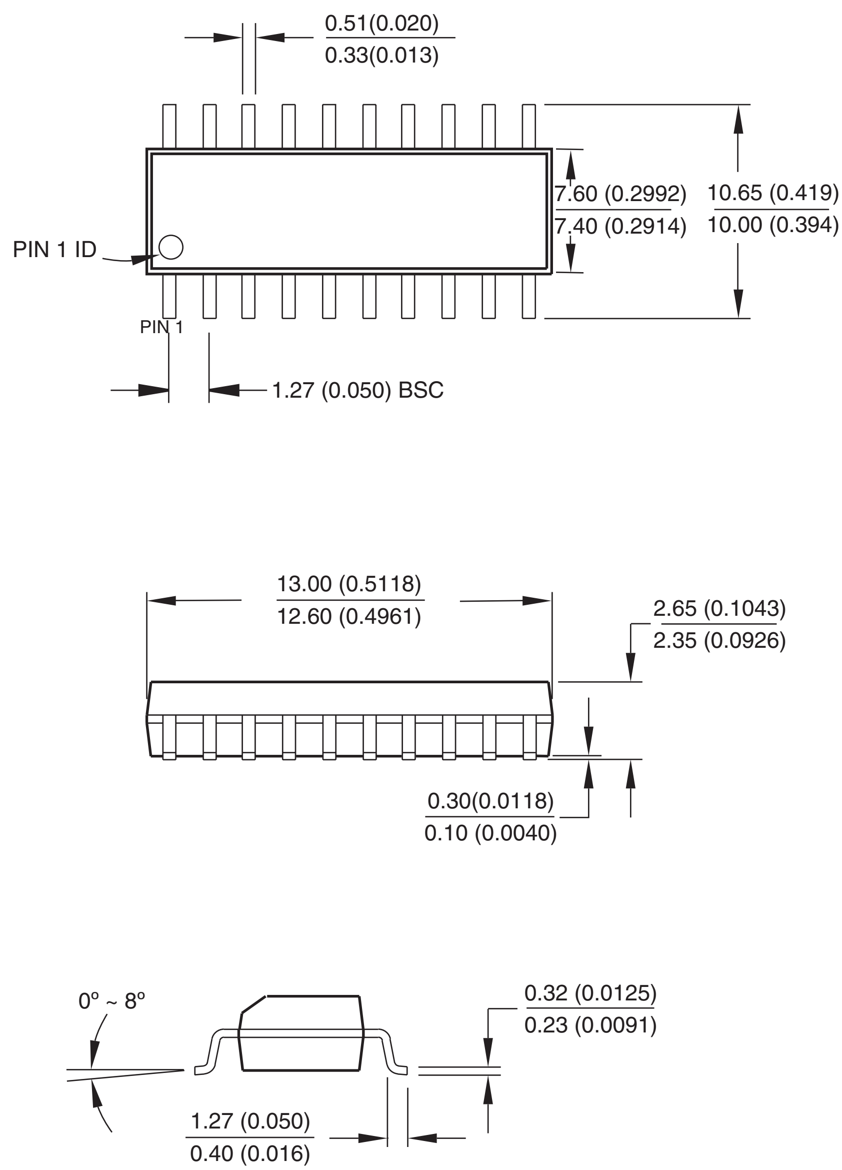
Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/23/04

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

11.3 20S – SOIC

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
JEDEC Standard MS-013

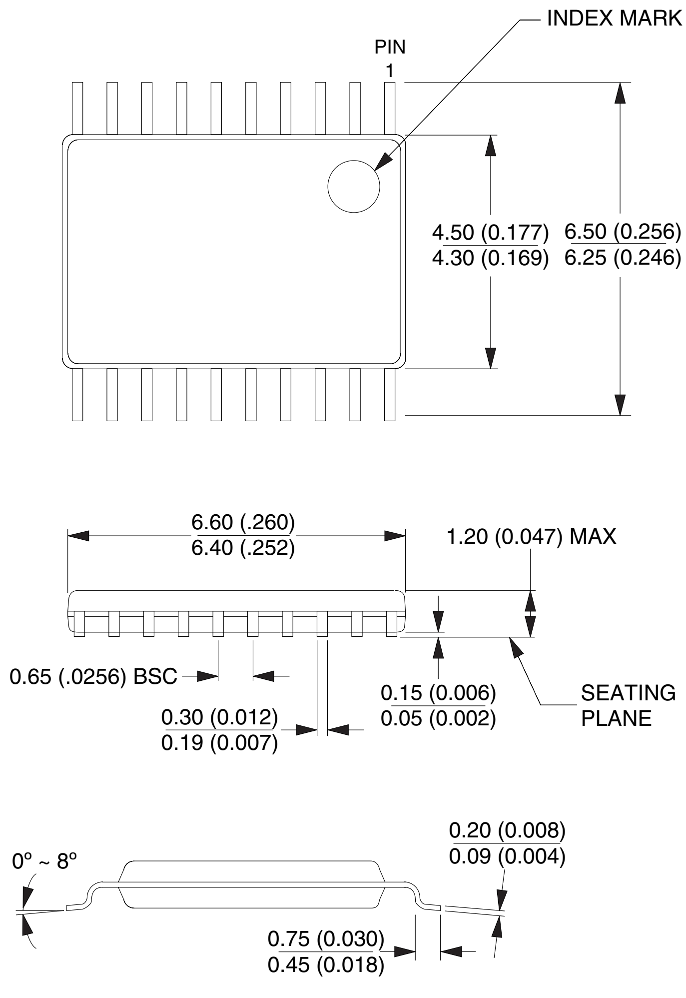


10/23/03

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **20S**, 20-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC)	**DRAWING NO.** 20S	**REV.** B

11.4 20X – TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC



10/23/03

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

12. Revision History

12.1 0453H

1. Green Package options added in 2005.

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