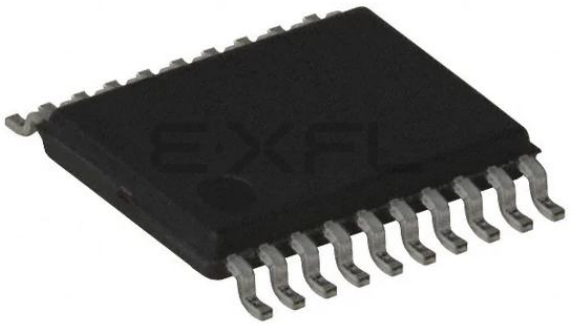


Welcome to E-XFL.COM

Understanding Embedded - PLDs (Programmable Logic Devices)

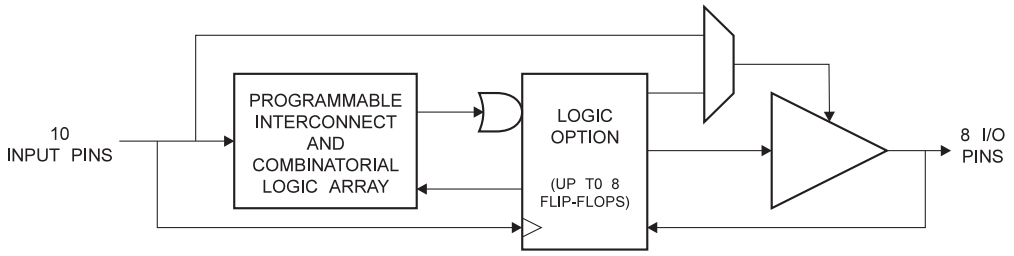
Embedded - PLDs, or Programmable Logic Devices, are a type of digital electronic component used to build reconfigurable digital circuits. Unlike fixed-function logic devices, PLDs can be programmed to perform specific functions by the user. This flexibility allows designers to customize the logic to meet the exact needs of their applications, making PLDs a crucial component in modern embedded systems.

Applications of Embedded - PLDs (Programmable Logic Devices)

The versatility of PLDs makes them suitable for a wide range of applications. In consumer electronics, PLDs are used to enhance the functionality and performance of

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Number of Macrocells	8
Voltage - Input	5V
Speed	12 ns
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf16v8cz-12xc

Figure 1-1. Block Diagram



2. Pin Configuration and Pinouts

Table 2-1. Pinouts - All Pinouts Top View

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bi-directional Buffers
$\overline{OE}$	Output Enable
VCC	+5V Supply

Figure 2-1. TSSOP

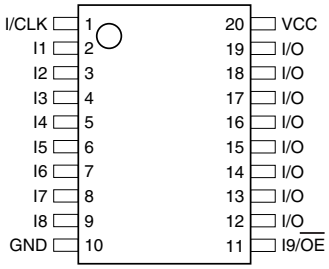
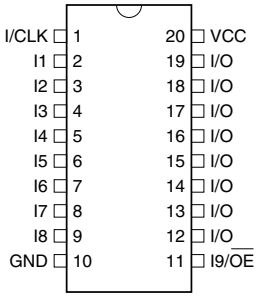
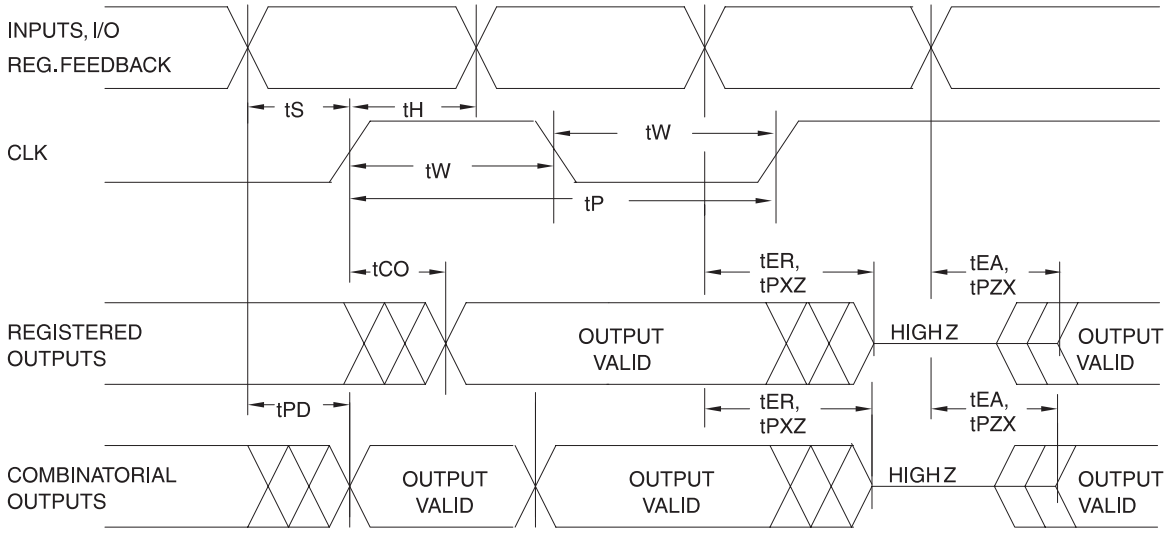


Figure 2-2. DIP/SOIC



4.2 AC Waveforms[1]



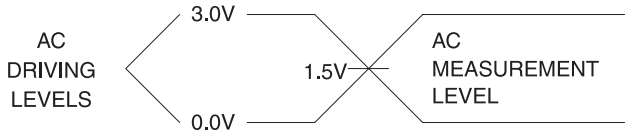
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

4.3 AC Characteristics

Symbol	Parameter	-12		-15		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-registered Output	3	12	3	15	ns
t_{CF}	Clock to Feedback		6		8	ns
t_{CO}	Clock to Output	2	8	2	10	ns
t_S	Input or Feedback Setup Time	10		12		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	12		16		ns
t_W	Clock Width	6		8		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$		55		45	MHz
	Internal Feedback $1/(t_S + t_{CF})$		62		50	MHz
	No Feedback $1/(t_P)$		83		62	MHz
t_{EA}	Input to Output Enable – Product Term	3	12	3	15	ns
t_{ER}	Input to Output Disable – Product Term	2	15	2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable	2	12	2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable	1.5	12	1.5	15	ns

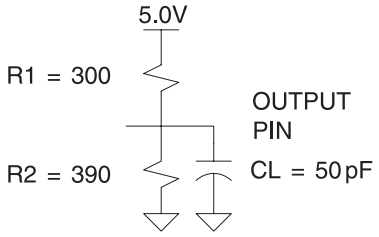
4.4 Input Test Waveforms

4.4.1 Input Test Waveforms and Measurement Levels



t_R, t_F < 1.5 ns (10% to 90%)

4.4.2 Output Test Loads



Note: Similar devices are tested with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible devices.

4.4.3 Pin Capacitance

Table 4-1. Pin Capacitance (f = 1 MHz, T = 25°C[1])

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

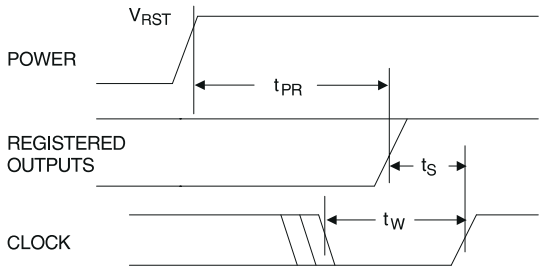
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

4.5 Power-up Reset

The ATF16V8CZ's registers are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic, from below 0.7V,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

4.6 Preload of Registered Outputs

The ATF16V8CZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by approved programmers.

5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8CZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

7. Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8CZ architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8CZ can be configured in one of three different modes. Each mode makes the ATF16V8CZ look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8CZ universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8CZ can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

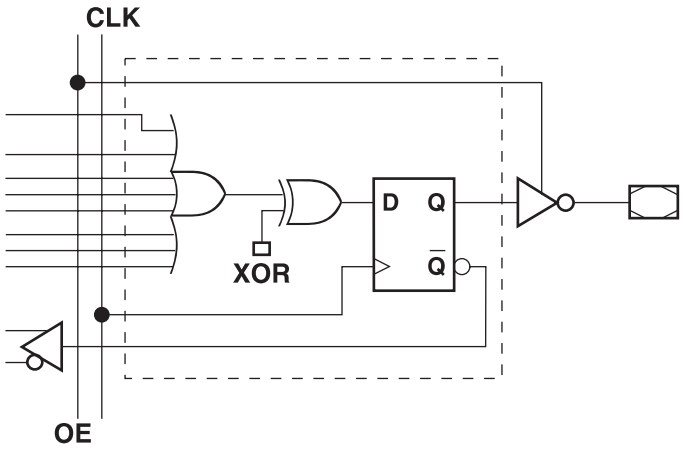
Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the content of the ATF16V8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the security fuse.

Table 7-1. Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16C8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8A
LOG/iC	GAL16V8_R(1)	GAL16V8_C7(1)	GAL16V8_C8(1)	GAL16V8
OrCAD-PLD	“Registered”	“Complex”	“Simple”	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

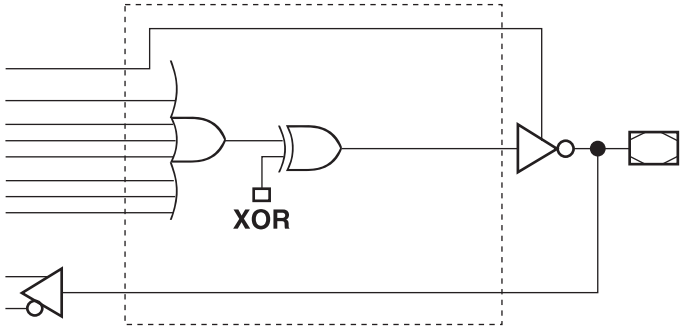
Notes: 1. Only applicable for version 3.4 or lower.

Figure 8-1. Registered Configuration for Registered Mode[1][2]



Notes:
1. Pin 1 controls common CLK for the registered outputs.
   Pin 11 controls common $\overline{OE}$ for the registered outputs.
   Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 8-2. Combinatorial Configuration for Registered Mode[1][2]



Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

8.2 ATF16V8CZ Complex Mode

PAL Device Emulation/PAL Replacement. In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

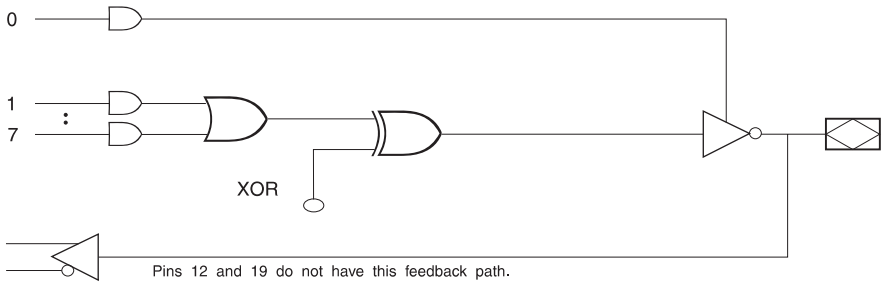
Combinatorial applications with an $\overline{OE}$ requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8

16H8

16P8

Figure 8-4. Complex Mode Option



9. ATF16V8CZ Simple Mode

PAL Device Emulation/PAL Replacement. In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without $\overline{OE}$ control. The following simple PALs can be emulated using this mode:

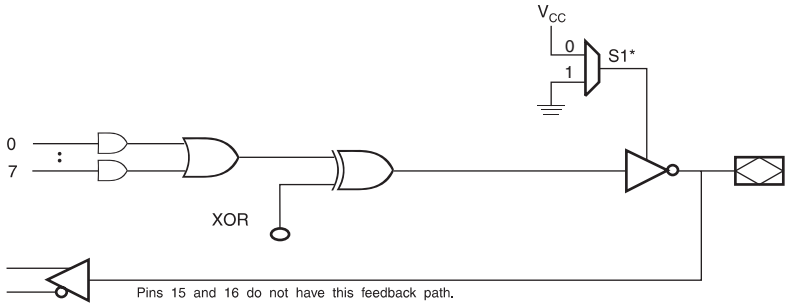
10L8 10H8 10P8

12L6 12H6 12P6

14L4 14H4 14P4

16L2 16H2 16P2

Figure 9-1. Simple Mode Option



* - Pins 15 and 16 are always enabled.

Figure 9-2. Complex Mode Logic Diagram

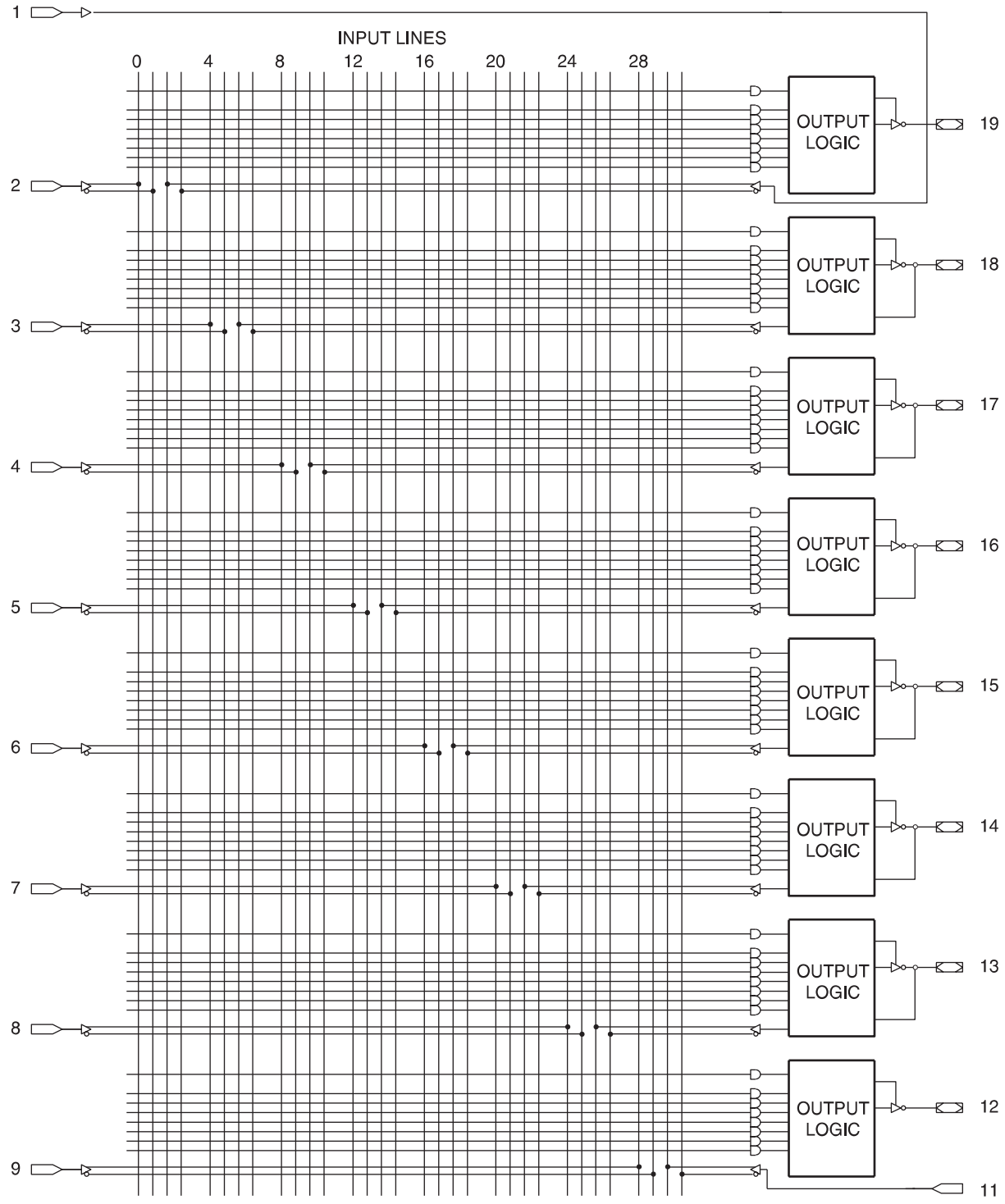
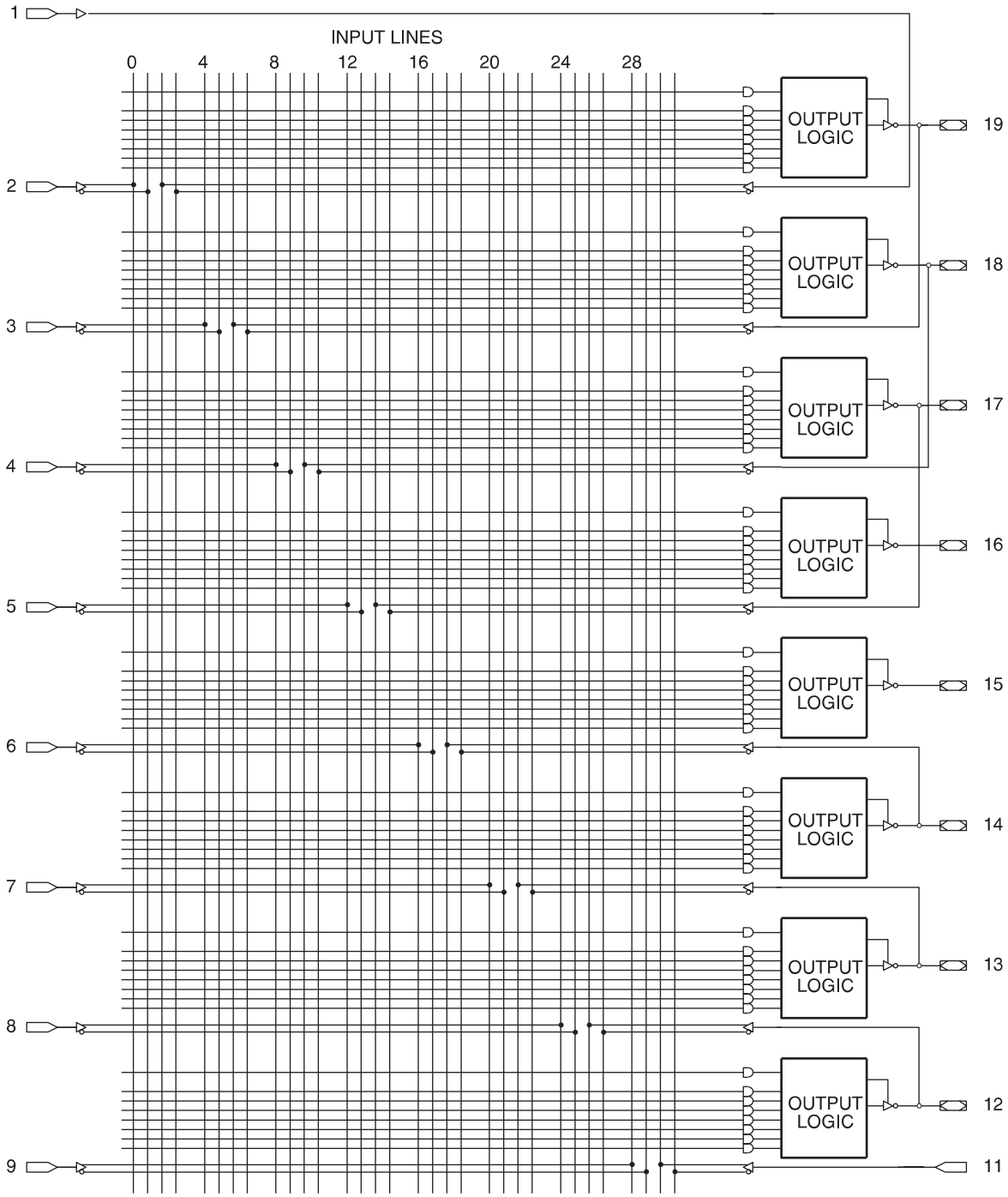
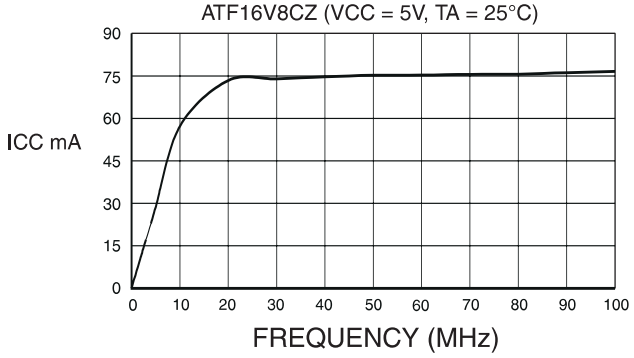


Figure 9-3. Simple Mode Logic Diagram

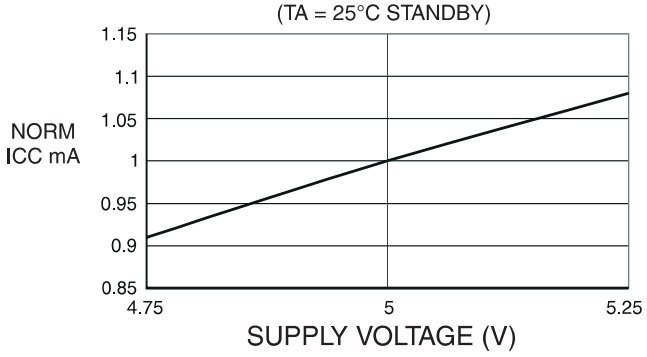


9.1 Test Characterization Data

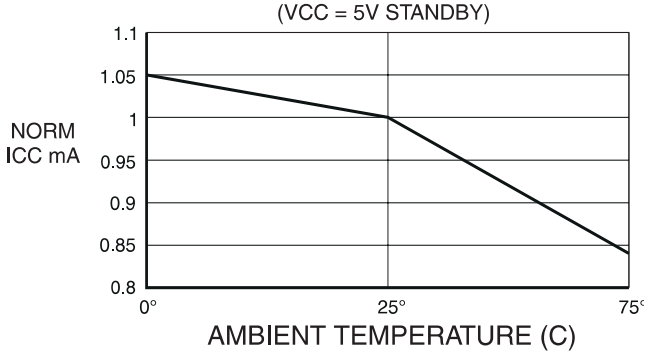
SUPPLY CURRENT
VS. INPUT FREQUENCY
ATF16V8CZ (VCC = 5V, TA = 25°C)



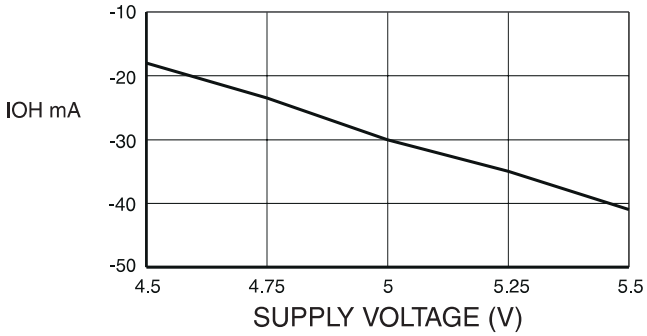
NORMALIZED SUPPLY CURRENT
VS. SUPPLY VOLTAGE
(TA = 25°C STANDBY)



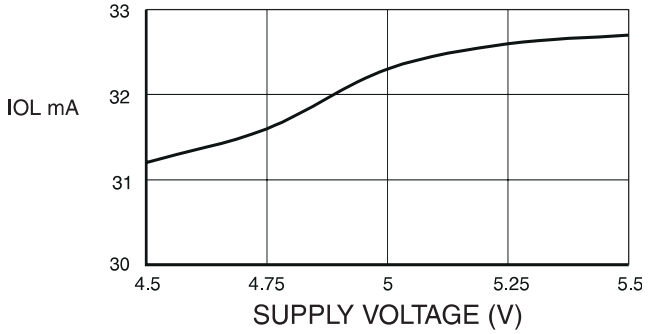
NORMALIZED SUPPLY CURRENT
VS. AMBIENT TEMPERATURE
(VCC = 5V STANDBY)



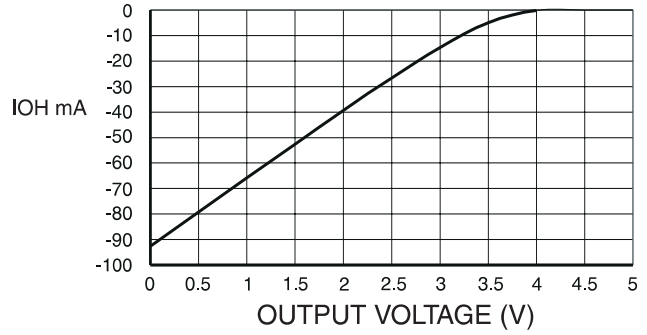
OUTPUT SOURCE CURRENT
VS. SUPPLY VOLTAGE (VOH = 2.4V, TA = 25°C)



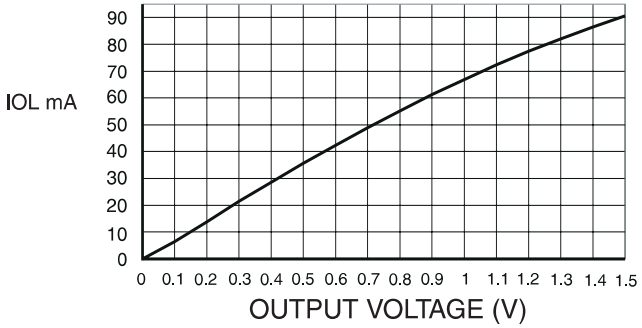
OUTPUT SINK CURRENT
VS. SUPPLY VOLTAGE (TA = 25°C, VOL = 0.45V)



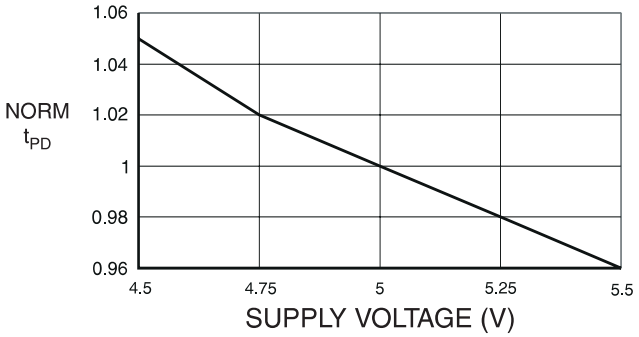
OUTPUT SOURCE CURRENT
VS. OUTPUT VOLTAGE (VOH = 2.4V, TA = 25°C)



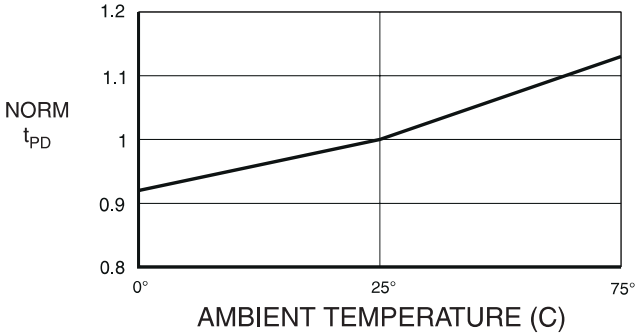
OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



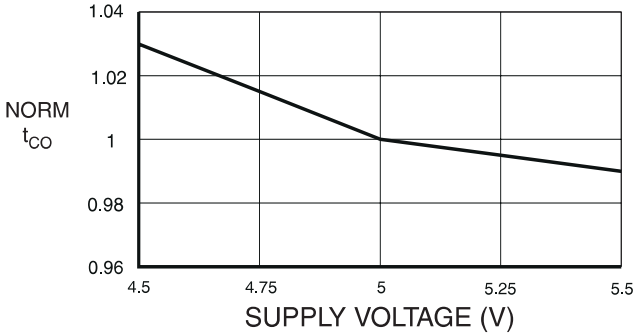
NORMALIZED t_{PD}
VS. SUPPLY VOLTAGE (TA = 25°C)



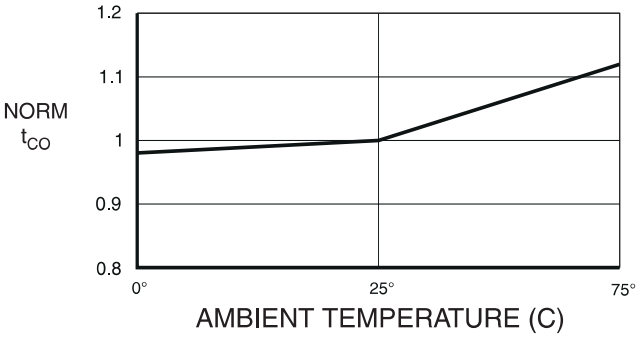
NORMALIZED t_{PD}
VS. AMBIENT TEMPERATURE (TA = 25°C)



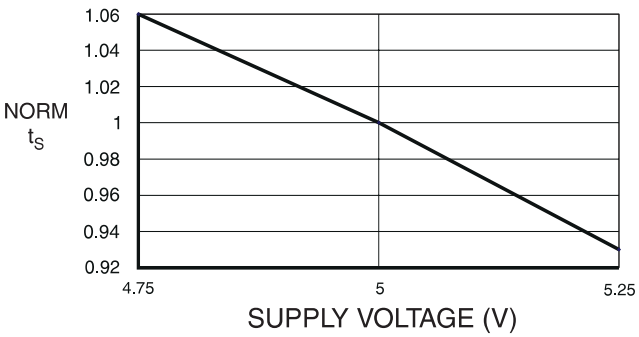
NORMALIZED t_{CO}
VS. SUPPLY VOLTAGE (TA = 25°C)



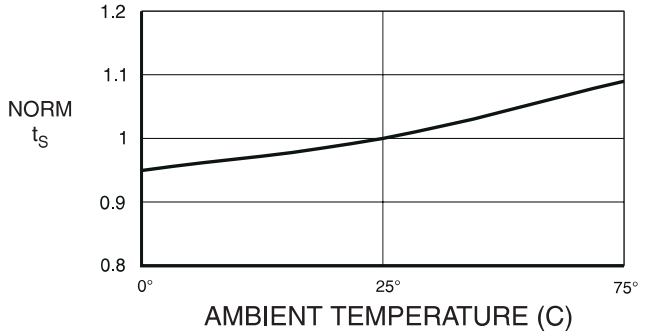
NORMALIZED t_{CO}
VS. AMBIENT TEMPERATURE (VCC = 5V)



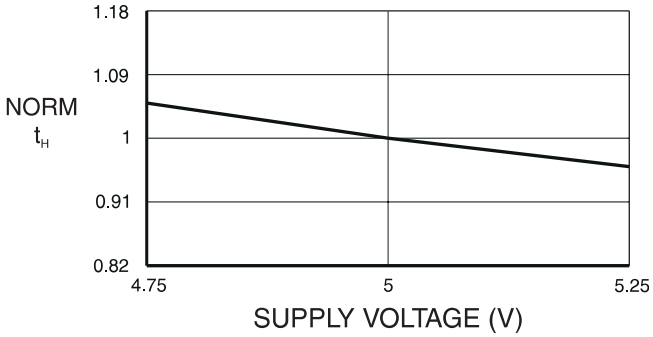
NORMALIZED t_S
VS. SUPPLY VOLTAGE (TA = 25C)



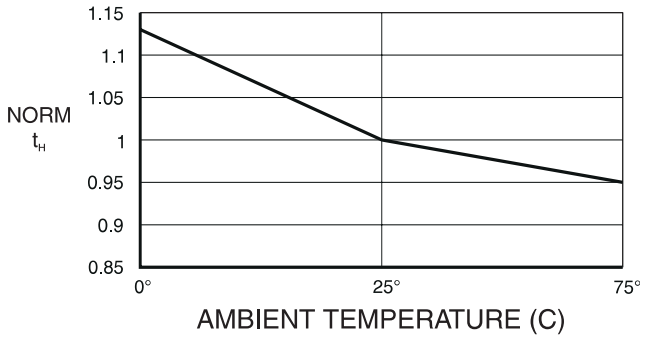
NORMALIZED t_S
VS. AMBIENT TEMPERATURE (TA = 25°C)



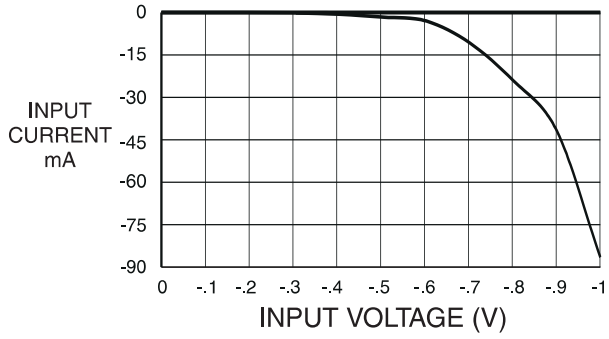
NORMALIZED t_H
VS. SUPPLY VOLTAGE (TA = 25°C)



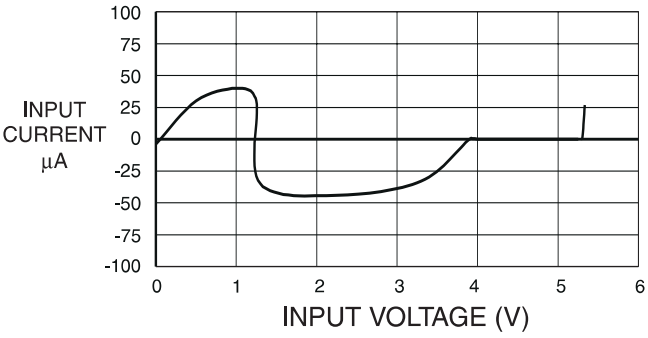
NORMALIZED t_H
VS. AMBIENT TEMPERATURE (VCC = 5V)



INPUT CLAMP CURRENT
VS. INPUT VOLTAGE (TA = 25°C, VCC = 5V)



INPUT CURRENT
VS. INPUT VOLTAGE (VCC = 5V, TA = 25°C)



10. Ordering Information

10.1 Standard Package Options

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
12	10	8	ATF16V8CZ-12JC ATF16V8CZ-12PC ATF16V8CZ-12SC ATF16V8CZ-12XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
15	12	10	ATF16V8CZ-15JC ATF16V8CZ-15PC ATF16V8CZ-15SC ATF16V8CZ-15XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
	12	10	ATF16V8CZ-15JI ATF16V8CZ-15PI ATF16V8CZ-15SI ATF16V8CZ-15XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)

Note: Shaded parts are being obsoleted in Q3-05 and being replaced by Green parts.

10.2 Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

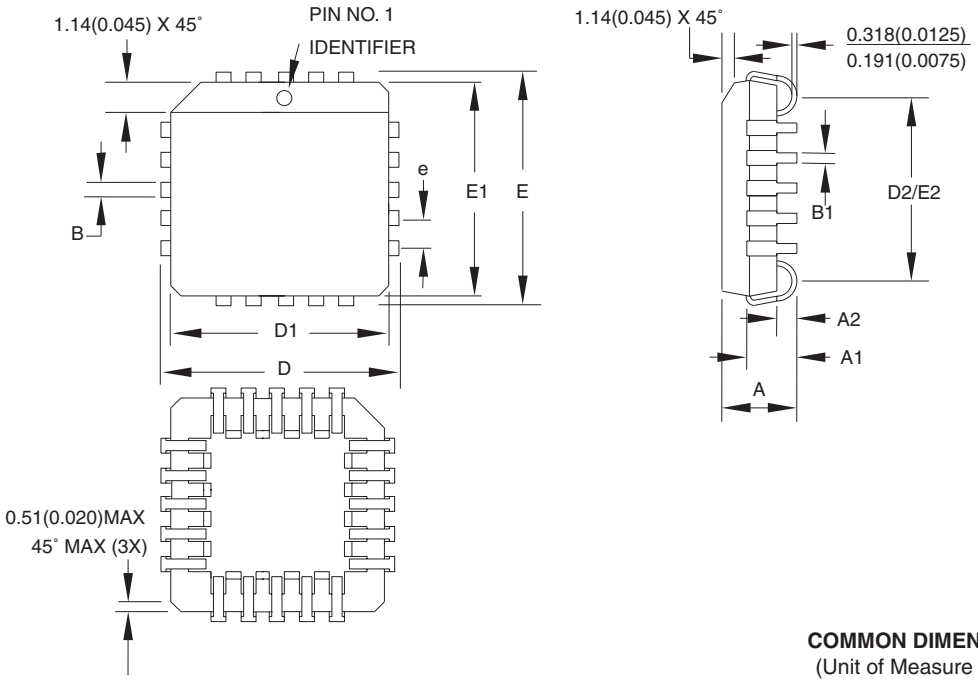
10.3 Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	12	10	ATF16V8CZ-15JU ATF16V8CZ-15PU ATF16V8CZ-15SU ATF16V8CZ-15XU	20J 20P3 20S 20X	Industrial (-40°C to 85°C)

Package Type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-wing Small Outline (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

11. Package Information

11.1 20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

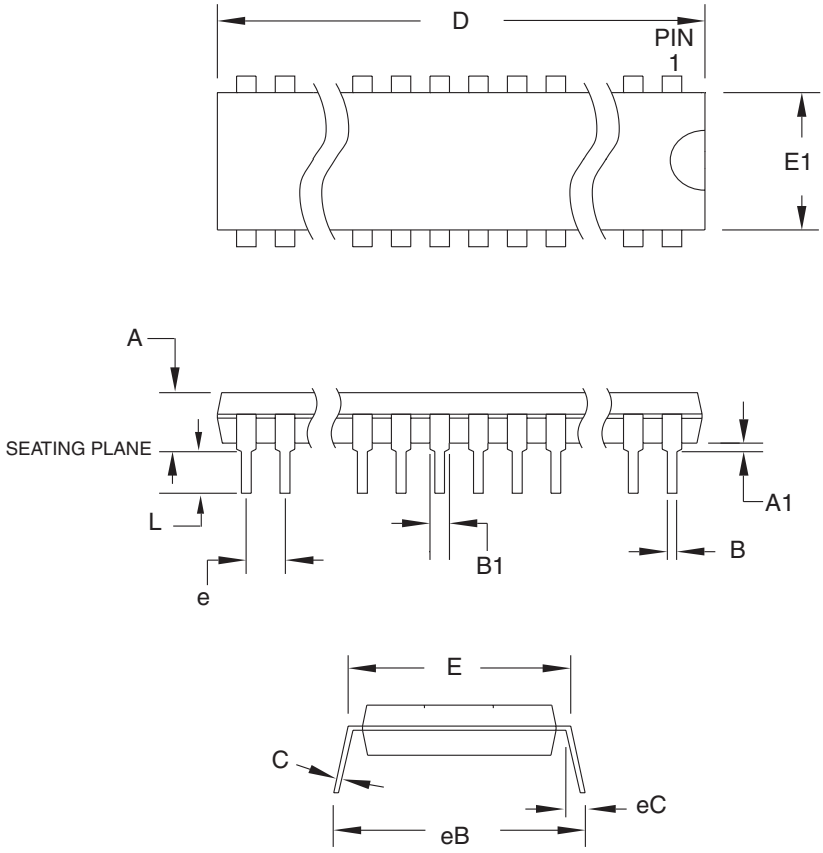
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

11.2 20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

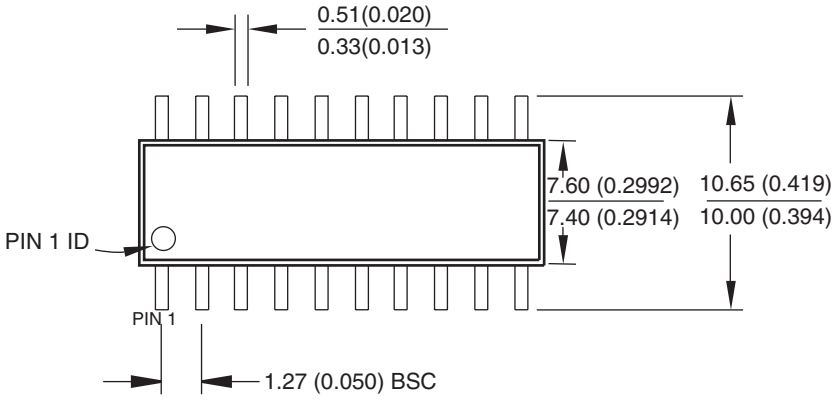
Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

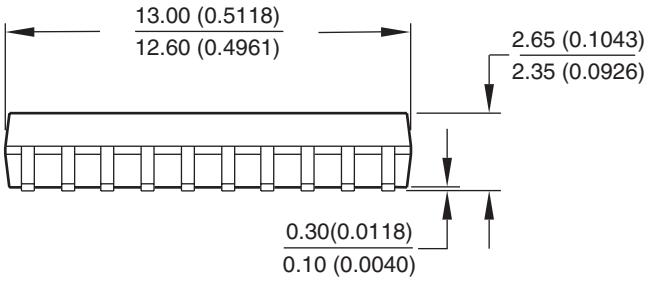
1/23/04

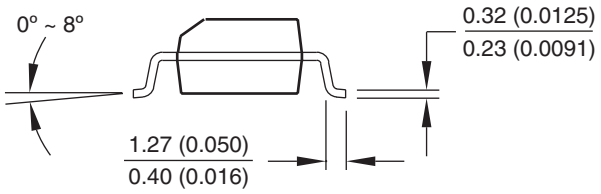
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

11.3 20S – SOIC

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
JEDEC Standard MS-013





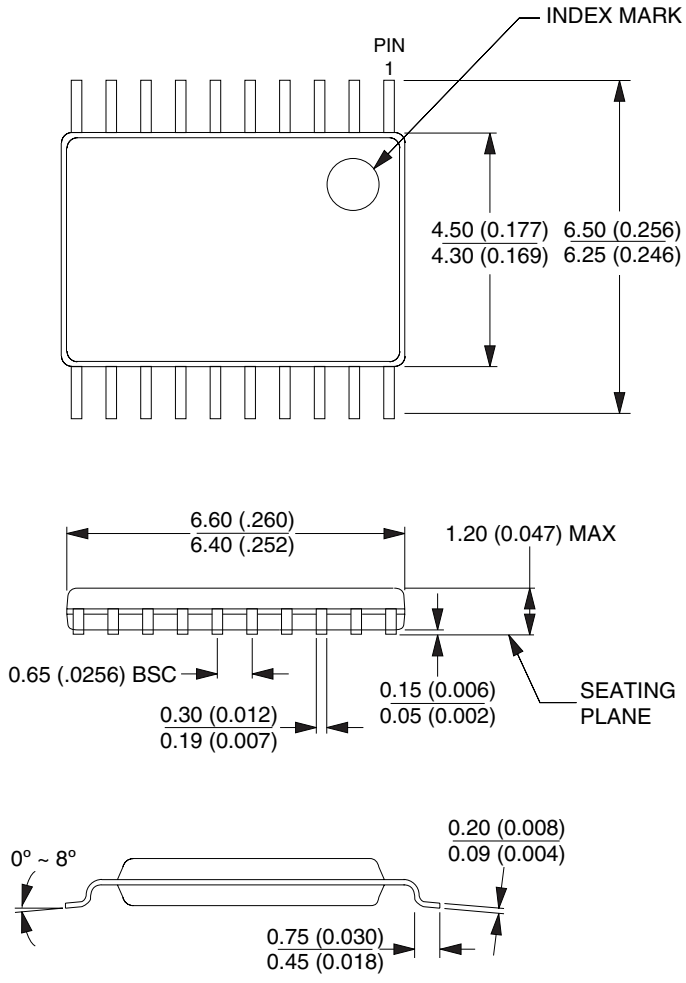


10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S**, 20-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC)	20S	B

11.4 20X – TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC



10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

12. Revision History

12.1 0453H

1. Green Package options added in 2005.

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