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#### Understanding Embedded - PLDs (Programmable Logic Devices)

Embedded - PLDs, or Programmable Logic Devices, are a type of digital electronic component used to build reconfigurable digital circuits. Unlike fixed-function logic devices, PLDs can be programmed to perform specific functions by the user. This flexibility allows designers to customize the logic to meet the exact needs of their applications, making PLDs a crucial component in modern embedded systems.

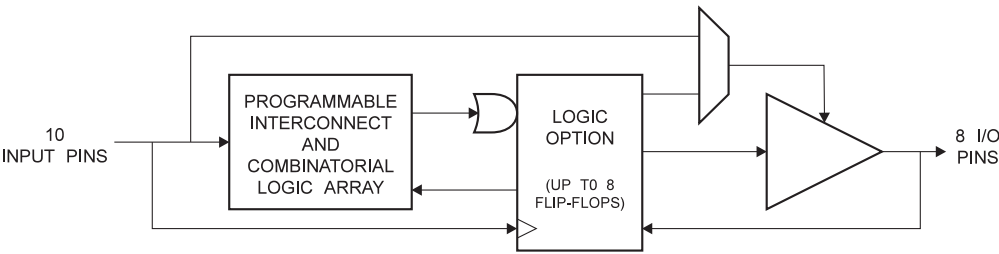
#### Applications of Embedded - PLDs (Programmable Logic Devices)

The versatility of PLDs makes them suitable for a wide range of applications. In consumer electronics, PLDs are used to enhance the functionality and performance of

#### Details

|                         |   |
|-------------------------|---|
| Product Status          | Obsolete  |
| Programmable Type       | EE PLD  |
| Number of Macrocells    | 8   |
| Voltage - Input         | 5V  |
| Speed                   | 15 ns   |
| Mounting Type           | Surface Mount   |
| Package / Case          | 20-TSSOP (0.173", 4.40mm Width)   |
| Supplier Device Package | 20-TSSOP  |
| Purchase URL            | <a href="https://www.e-xfl.com/product-detail/atmel/atf16v8cz-15xc">https://www.e-xfl.com/product-detail/atmel/atf16v8cz-15xc</a> |

**Figure 1-1.** Block Diagram

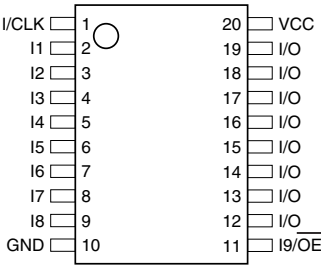


## 2. Pin Configuration and Pinouts

**Table 2-1.** Pinouts - All Pinouts Top View

| Pin Name        | Function               |
|-----------------|------------------------|
| CLK             | Clock                  |
| I               | Logic Inputs           |
| I/O             | Bi-directional Buffers |
| $\overline{OE}$ | Output Enable          |
| VCC             | +5V Supply             |

**Figure 2-1.** TSSOP



**Figure 2-2.** DIP/SOIC

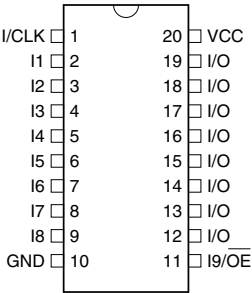
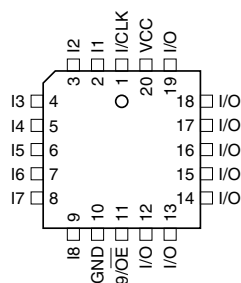


Figure 2-3. PLCC



### 3. Absolute Maximum Ratings\*

|  |                                |
|--|--------------------------------|
| Temperature Under Bias.....  | -40°C to +85°C                 |
| Storage Temperature .....  | -65°C to +150°C                |
| Voltage on Any Pin with<br>Respect to Ground .....                         | -2.0V to +7.0V <sup>(1)</sup>  |
| Voltage on Input Pins<br>with Respect to Ground<br>During Programming..... | -2.0V to +14.0V <sup>(1)</sup> |
| Programming Voltage with<br>Respect to Ground .....                        | -2.0V to +14.0V <sup>(1)</sup> |

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note:** 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20 ns.

### 4. DC and AC Operating Conditions

|                                 | Commercial   | Industrial    |
|---------------------------------|--------------|---------------|
| Operating Temperature (Ambient) | 0°C - 70°C   | -40°C - 85°C  |
| $V_{CC}$ Power Supply           | 5V $\pm 5\%$ | 5V $\pm 10\%$ |

#### 4.1 DC Characteristics

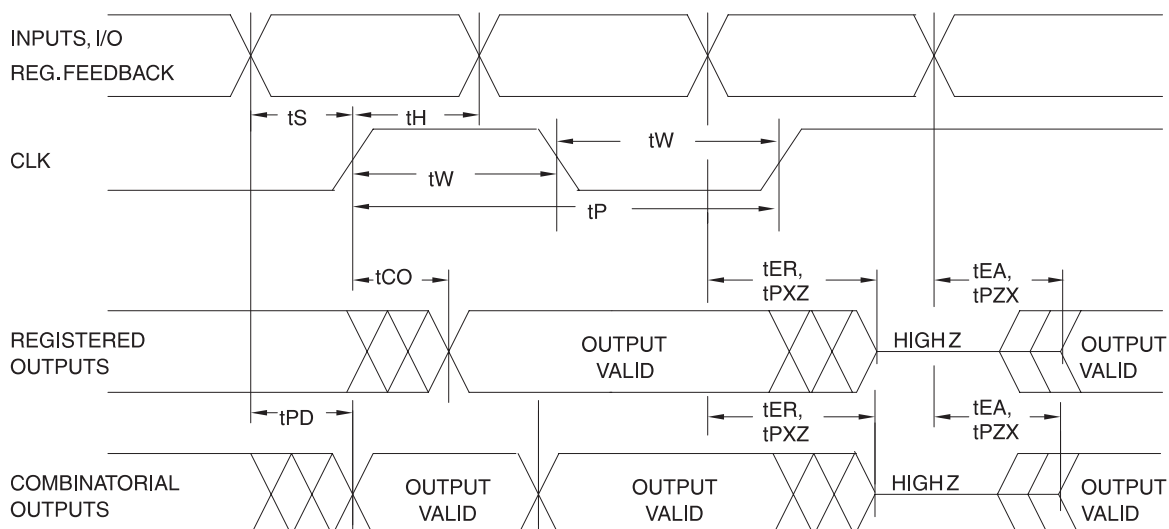
| Symbol         | Parameter                             | Condition   | Min  | Typ | Max        | Units   |
|----------------|---------------------------------------|---|------|-----|------------|---------|
| $I_{IL}$       | Input or I/O Low Leakage Current      | $0 \leq V_{IN} \leq V_{IL}(\text{Max})$                                   |      |     | -10        | $\mu A$ |
| $I_{IH}$       | Input or I/O High Leakage Current     | $3.5 \leq V_{IN} \leq V_{CC}$   |      |     | 10         | $\mu A$ |
| $I_{CC1}$      | Power Supply Current                  | 15 MHz, $V_{CC} = \text{Max}$ ,<br>$V_{IN} = 0$ , $V_{CC}$ , Outputs Open | Com  |     | 95         | mA      |
|                |                                       |   | Ind. |     | 105        | mA      |
| $I_{CC}^{(1)}$ | Power Supply Current,<br>Standby Mode | 0 MHz, $V_{CC} = \text{Max}$ ,<br>$V_{IN} = 0$ , $V_{CC}$ , Outputs Open  | Com. | 5   |            | $\mu A$ |
|                |                                       |   | Ind  | 5   |            | $\mu A$ |
| $I_{OS}$       | Output Short Circuit Current          | $V_{OUT} = 0.5V$ ;<br>$V_{CC} = 5V$ ; $T_A = 25^\circ C$                  |      |     | -150       | mA      |
| $V_{IL}$       | Input Low Voltage                     | $\text{Min} < V_{CC} < \text{Max}$  | -0.5 |     | 0.8        | V       |
| $V_{IH}$       | Input High Voltage                    |   | 2.0  |     | $V_{CC}+1$ | V       |
| $V_{OL}$       | Output Low Voltage                    | $V_{CC} = \text{Min}$ , All Outputs<br>$I_{OL} = -16 \text{ mA}$          |      |     | 0.5        | V       |

## 4.1 DC Characteristics

| Symbol   | Parameter           | Condition   |            | Min | Typ | Max | Units |
|----------|---------------------|---|------------|-----|-----|-----|-------|
| $V_{OH}$ | Output High Voltage | $V_{CC} = \text{Min}$<br>$I_{OL} = -3.2 \text{ mA}$ |            | 2.4 |     |     | V     |
| $I_{OL}$ | Output Low Current  | $V_{CC} = \text{Min}$                               | Com.       | 24  |     |     | mA    |
|          |                     |   | Ind.       | 12  |     |     |       |
| $I_{OH}$ | Output High Current | $V_{CC} = \text{Min}$                               | Com., Ind. | 4   |     |     | mA    |

Note: 1. All  $I_{CC}$  parameters measured with outputs open. Data is based on Atmel test patterns. Reading may vary with pattern.

## 4.2 AC Waveforms<sup>(1)</sup>



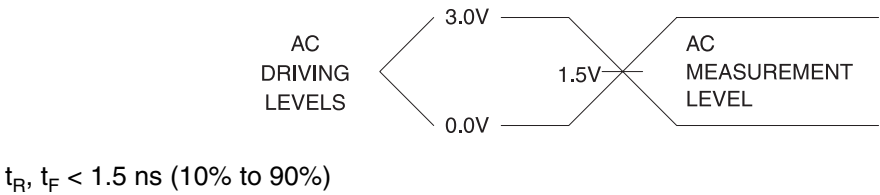
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

## 4.3 AC Characteristics

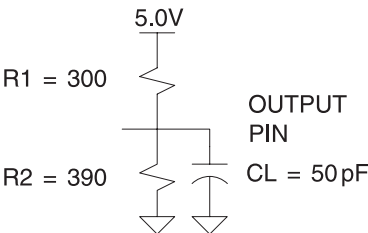
| Symbol    | Parameter                                  | -12 |     | -15 |     | Units |
|-----------|--|-----|-----|-----|-----|-------|
|           |  | Min | Max | Min | Max |       |
| $t_{PD}$  | Input or Feedback to Non-registered Output | 3   | 12  | 3   | 15  | ns    |
| $t_{CF}$  | Clock to Feedback                          |     | 6   |     | 8   | ns    |
| $t_{CO}$  | Clock to Output                            | 2   | 8   | 2   | 10  | ns    |
| $t_S$     | Input or Feedback Setup Time               | 10  |     | 12  |     | ns    |
| $t_H$     | Input Hold Time                            | 0   |     | 0   |     | ns    |
| $t_P$     | Clock Period                               | 12  |     | 16  |     | ns    |
| $t_W$     | Clock Width                                | 6   |     | 8   |     | ns    |
| $f_{MAX}$ | External Feedback $1/(t_S + t_{CO})$       |     | 55  |     | 45  | MHz   |
|           | Internal Feedback $1/(t_S + t_{CF})$       |     | 62  |     | 50  | MHz   |
|           | No Feedback $1/(t_P)$                      |     | 83  |     | 62  | MHz   |
| $t_{EA}$  | Input to Output Enable – Product Term      | 3   | 12  | 3   | 15  | ns    |
| $t_{ER}$  | Input to Output Disable – Product Term     | 2   | 15  | 2   | 15  | ns    |
| $t_{PZX}$ | $\overline{OE}$ pin to Output Enable       | 2   | 12  | 2   | 15  | ns    |
| $t_{PXZ}$ | $\overline{OE}$ pin to Output Disable      | 1.5 | 12  | 1.5 | 15  | ns    |

## 4.4 Input Test Waveforms

### 4.4.1 Input Test Waveforms and Measurement Levels



### 4.4.2 Output Test Loads



Note: Similar devices are tested with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible devices.

### 4.4.3 Pin Capacitance

**Table 4-1.** Pin Capacitance ( $f = 1 \text{ MHz}$ ,  $T = 25^\circ\text{C}^{(1)}$ )

|           | Typ | Max | Units | Conditions     |
|-----------|-----|-----|-------|----------------|
| $C_{IN}$  | 5   | 8   | pF    | $V_{IN} = 0V$  |
| $C_{OUT}$ | 6   | 8   | pF    | $V_{OUT} = 0V$ |

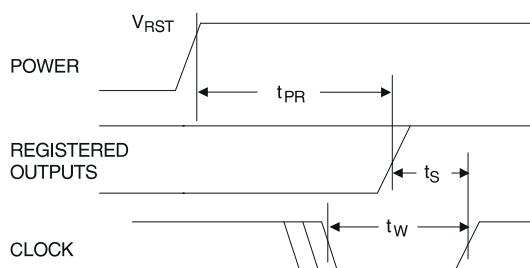
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## 4.5 Power-up Reset

The ATF16V8CZ's registers are designed to reset during power-up. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

1. The  $V_{CC}$  rise must be monotonic, from below 0.7V,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during  $t_{PR}$ .



| Parameter | Description            | Typ | Max   | Units |
|-----------|------------------------|-----|-------|-------|
| $t_{PR}$  | Power-up Reset Time    | 600 | 1,000 | ns    |
| $V_{RST}$ | Power-up Reset Voltage | 3.8 | 4.5   | V     |

## 4.6 Preload of Registered Outputs

The ATF16V8CZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by approved programmers.

## 5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8CZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

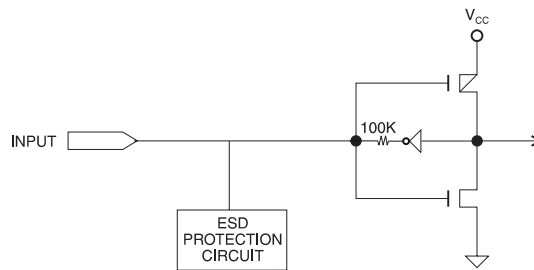
The security fuse should be programmed last, as its effect is immediate.

## 6. Input and I/O Pin-keeper Circuits

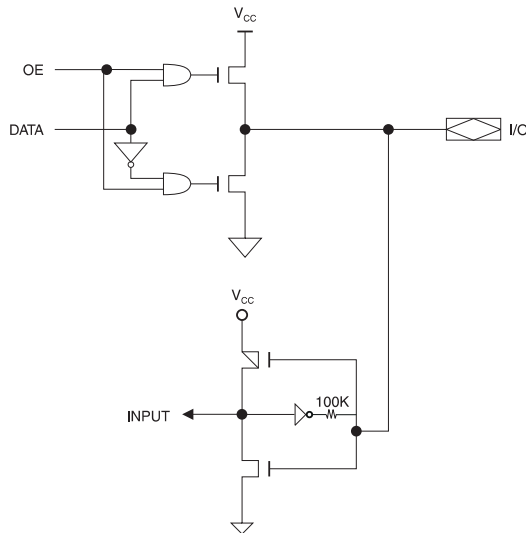
The ATF16V8CZ contains internal input and I/O pin-keeper circuits. These circuits allow each ATF16V8CZ pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40  $\mu$ A.

**Figure 6-1.** Input Diagram



**Figure 6-2.** I/O Diagram





## 7. Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8CZ architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8CZ can be configured in one of three different modes. Each mode makes the ATF16V8CZ look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8CZ universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8CZ can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the content of the ATF16V8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the security fuse.

**Table 7-1.** Compiler Mode Selection

|                         | Registered               | Complex                   | Simple                    | Auto Select |
|-------------------------|--------------------------|---------------------------|---------------------------|-------------|
| <b>ABEL, Atmel-ABEL</b> | P16C8R                   | P16V8C                    | P16V8AS                   | P16V8       |
| <b>CUPL</b>             | G16V8MS                  | G16V8MA                   | G16V8AS                   | G16V8A      |
| <b>LOG/iC</b>           | GAL16V8_R <sup>(1)</sup> | GAL16V8_C7 <sup>(1)</sup> | GAL16V8_C8 <sup>(1)</sup> | GAL16V8     |
| <b>OrCAD-PLD</b>        | “Registered”             | “Complex”                 | “Simple”                  | GAL16V8A    |
| <b>PLDesigner</b>       | P16V8R                   | P16V8C                    | P16V8C                    | P16V8A      |
| <b>Tango-PLD</b>        | G16V8R                   | G16V8C                    | G16V8AS                   | G16V8       |

Notes: 1. Only applicable for version 3.4 or lower.

## 8. Macrocell Configuration

Software compilers support the three different OMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable ( $\overline{OE}$ ) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with  $\overline{OE}$  controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without  $\overline{OE}$  control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

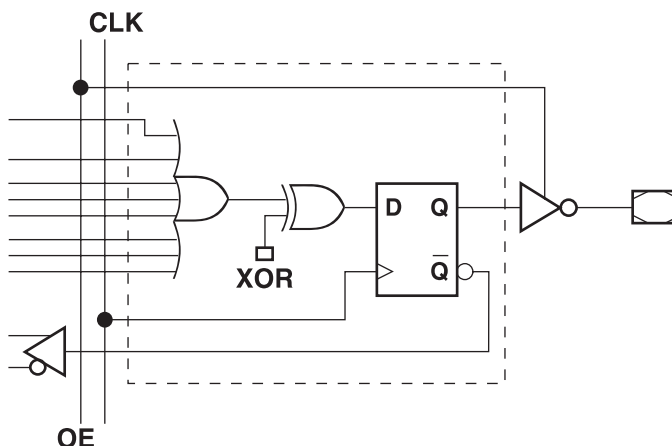
### 8.1 ATF16V8CZ Registered Mode

**PAL Device Emulation/PAL Replacement.** The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the  $\overline{OE}$  pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

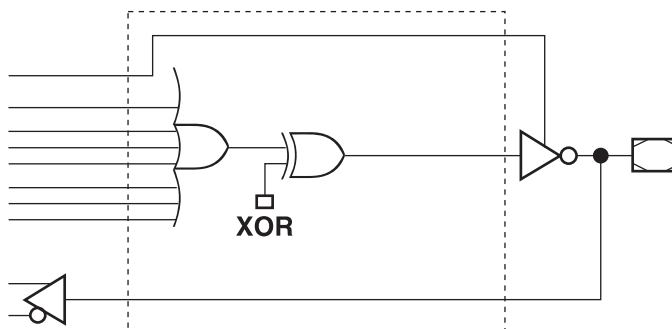
|      |       |
|------|-------|
| 16R8 | 16RP8 |
| 16R6 | 16RP6 |
| 16R4 | 16RP4 |

**Figure 8-1.** Registered Configuration for Registered Mode<sup>(1)(2)</sup>



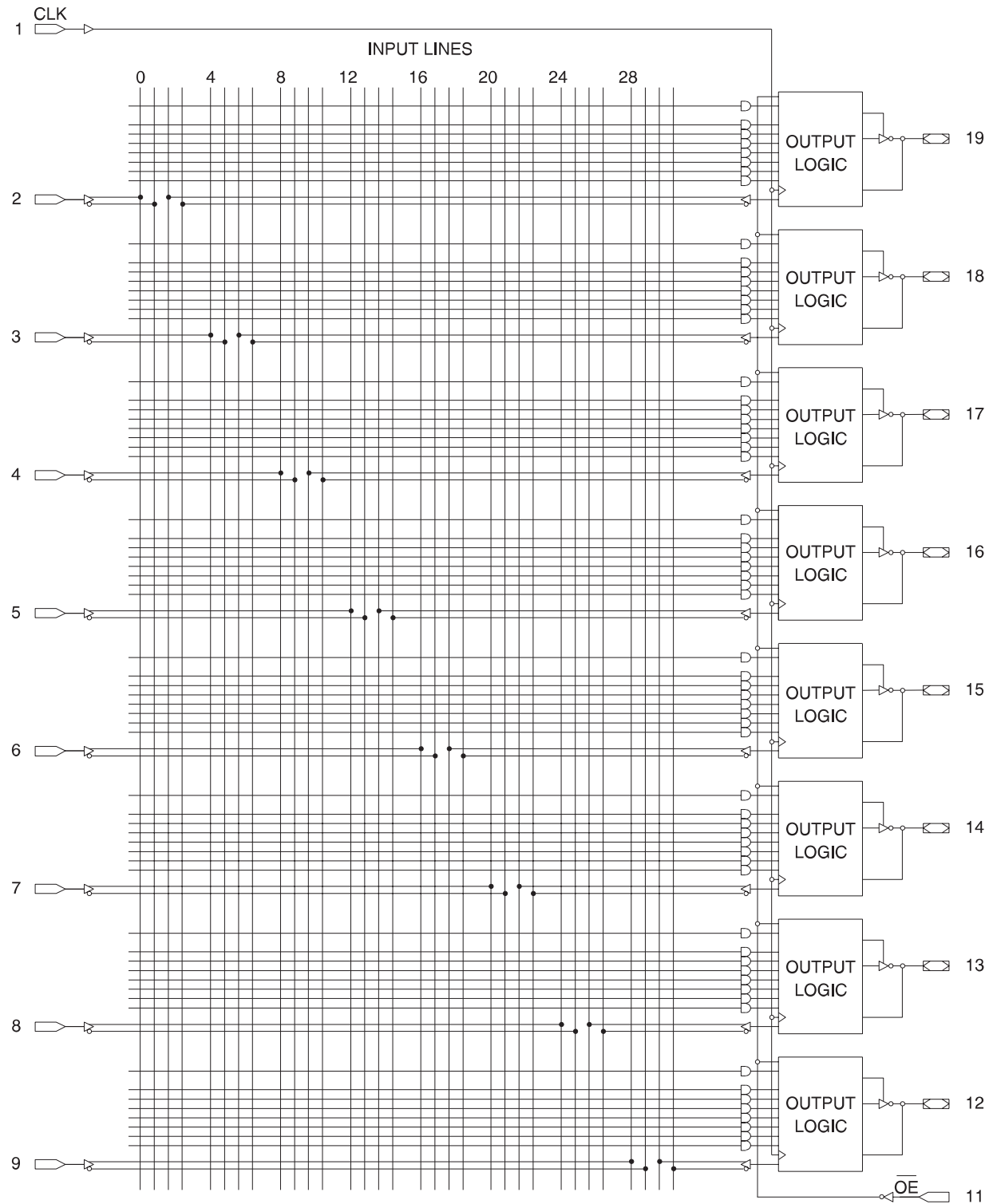
- Notes:
1. Pin 1 controls common CLK for the registered outputs.  
Pin 11 controls common  $\overline{OE}$  for the registered outputs.  
Pin 1 and Pin 11 are permanently configured as CLK and  $\overline{OE}$ .
  2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

**Figure 8-2.** Combinatorial Configuration for Registered Mode<sup>(1)(2)</sup>

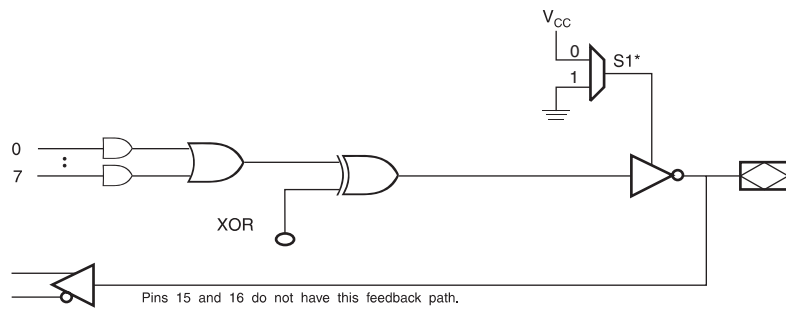


- Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and  $\overline{OE}$ .
  2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

**Figure 8-3.** Registered Mode Logic Diagram

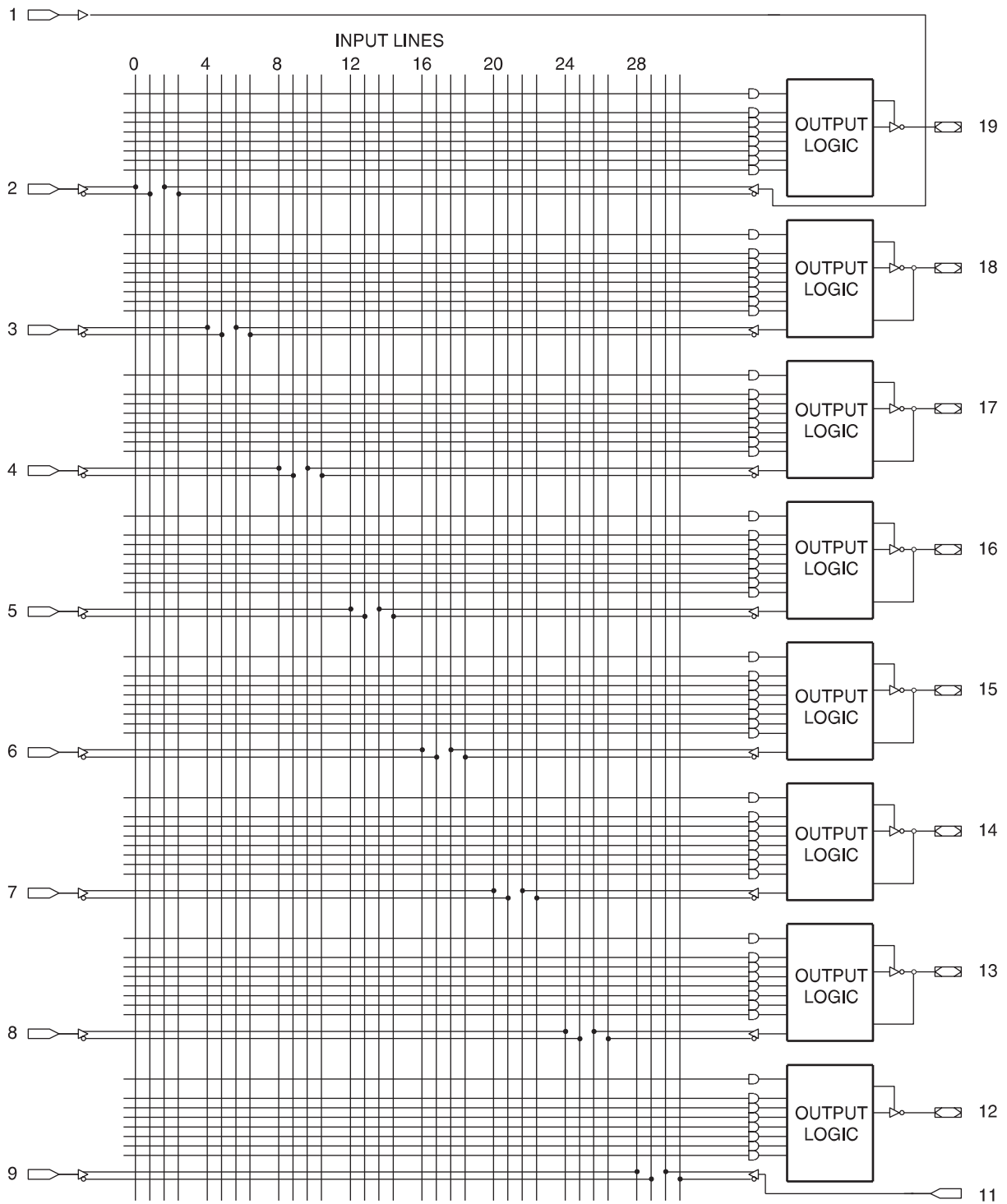


**Figure 9-1.** Simple Mode Option

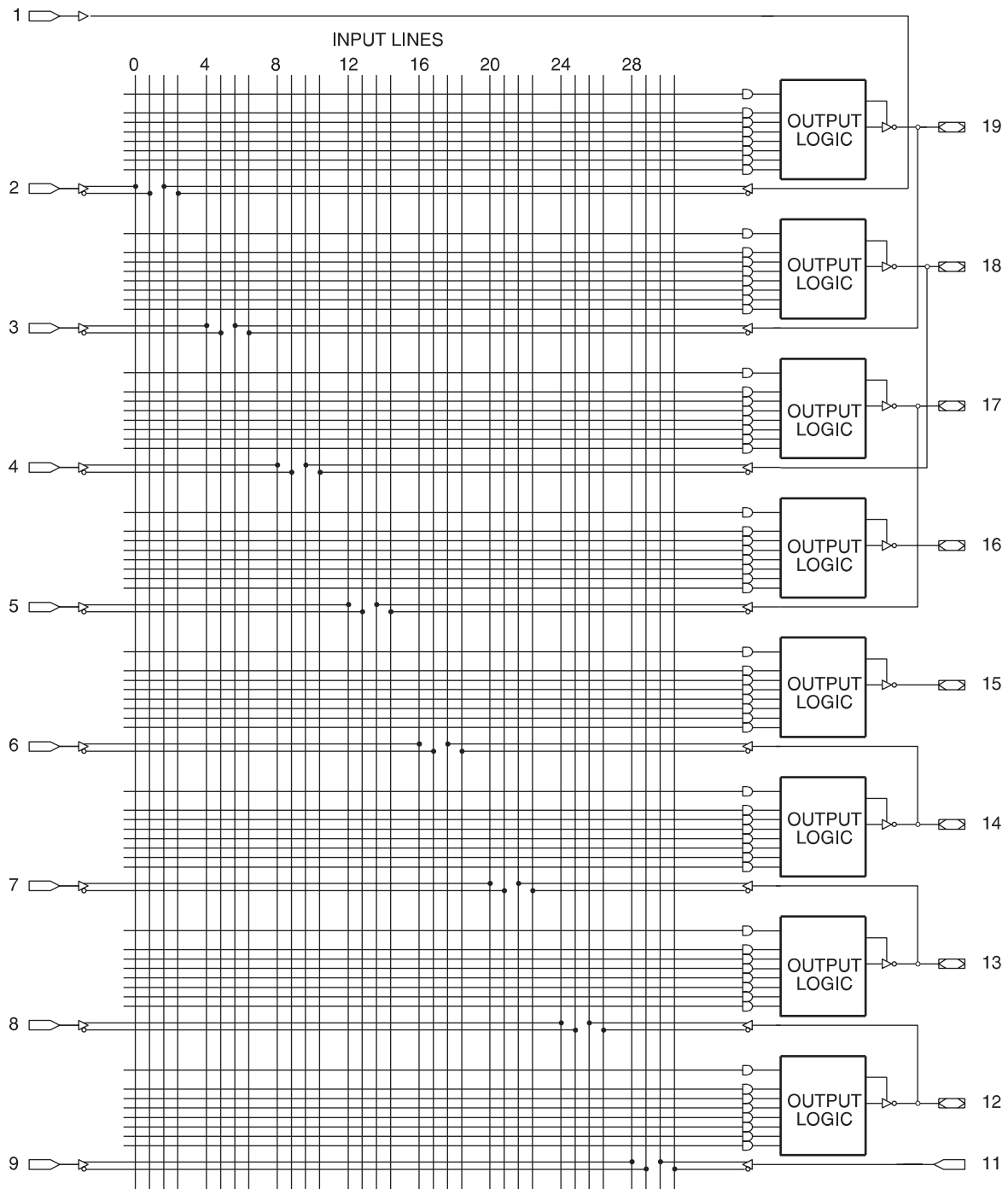


\* - Pins 15 and 16 are always enabled.

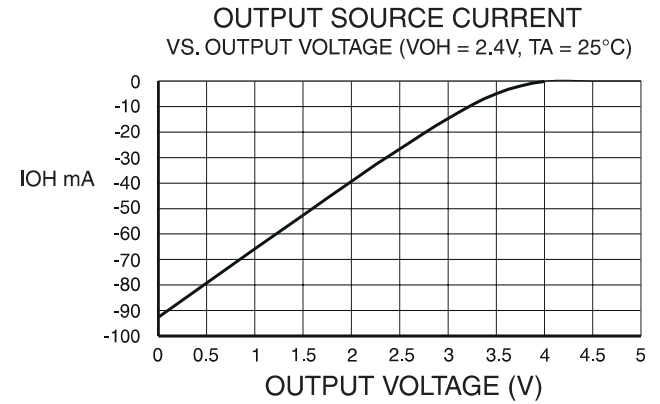
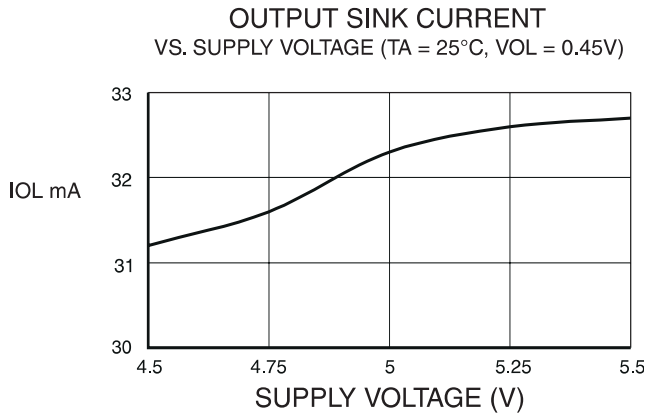
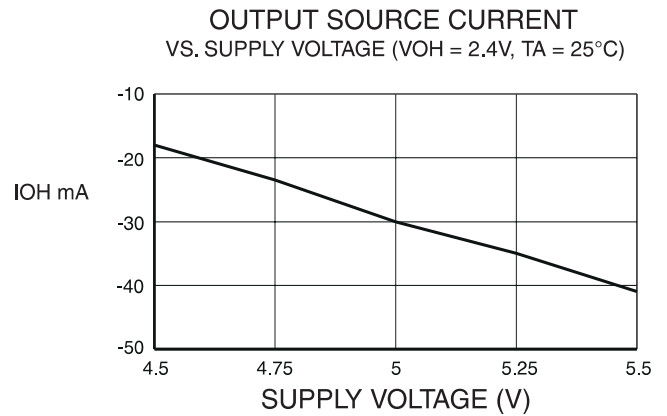
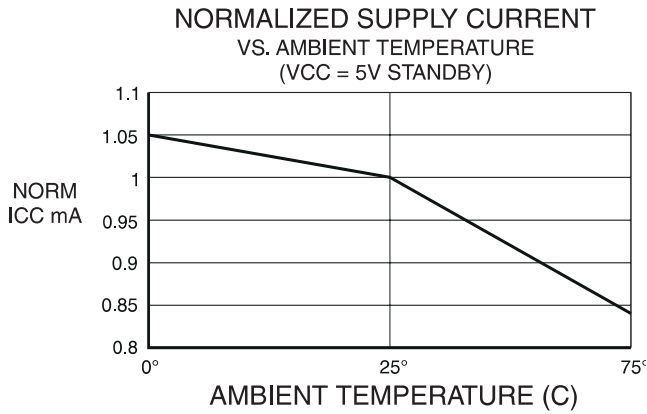
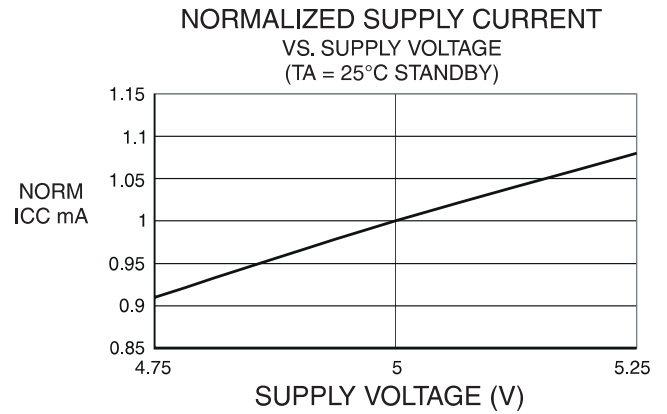
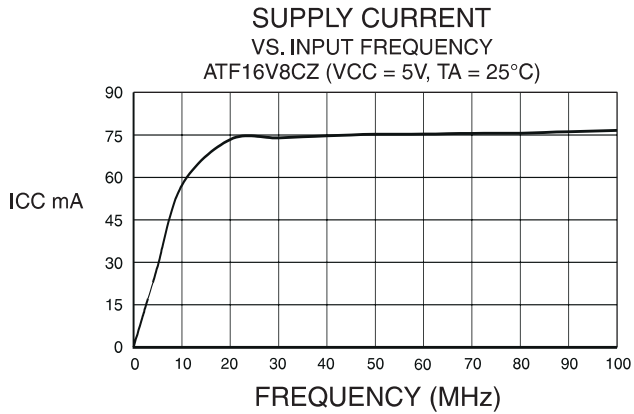
Figure 9-2. Complex Mode Logic Diagram



**Figure 9-3.** Simple Mode Logic Diagram

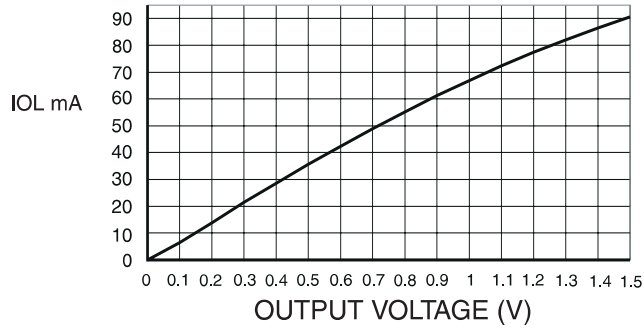


## 9.1 Test Characterization Data

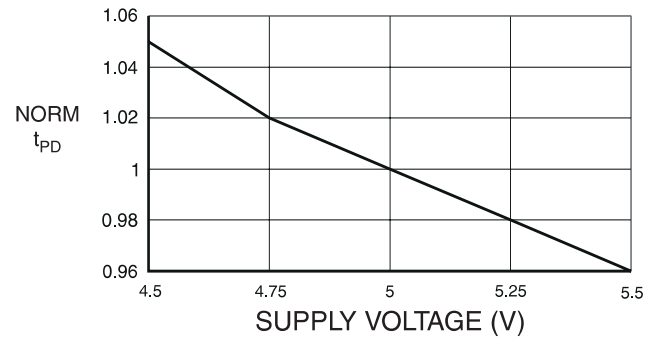




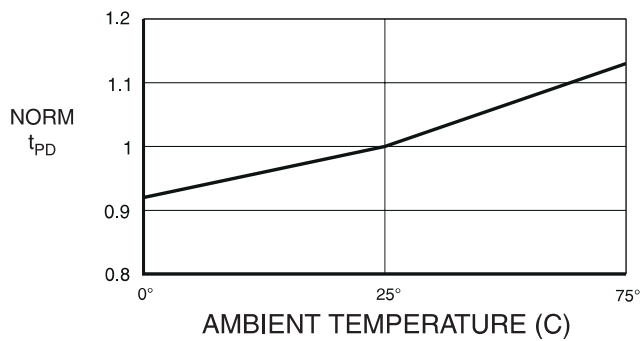
OUTPUT SINK CURRENT  
VS. OUTPUT VOLTAGE (VCC = 5V, TA = 25°C)



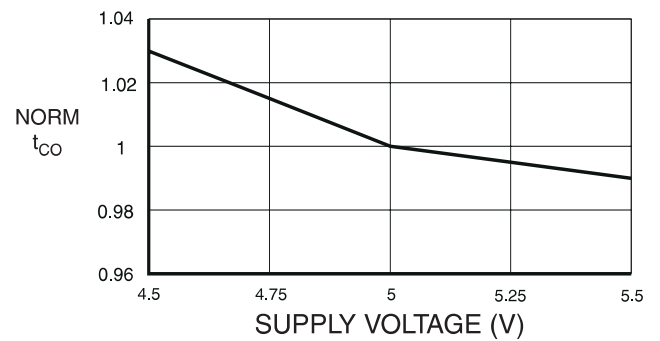
NORMALIZED  $t_{PD}$   
VS. SUPPLY VOLTAGE (TA = 25°C)



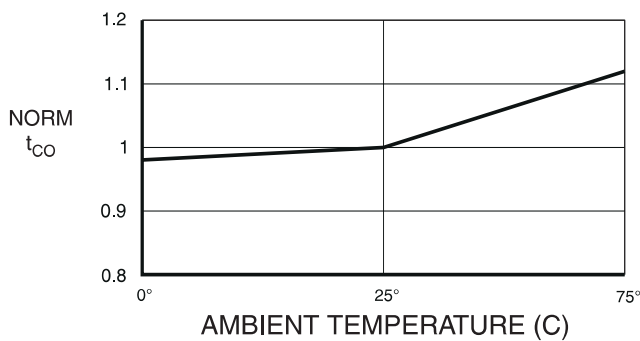
NORMALIZED  $t_{PD}$   
VS. AMBIENT TEMPERATURE (TA = 25°C)



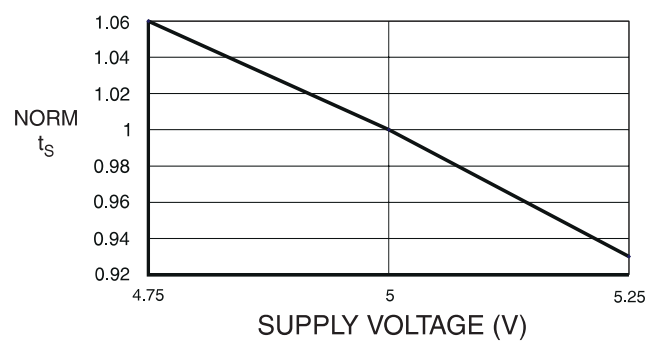
NORMALIZED  $t_{CO}$   
VS. SUPPLY VOLTAGE (TA = 25°C)

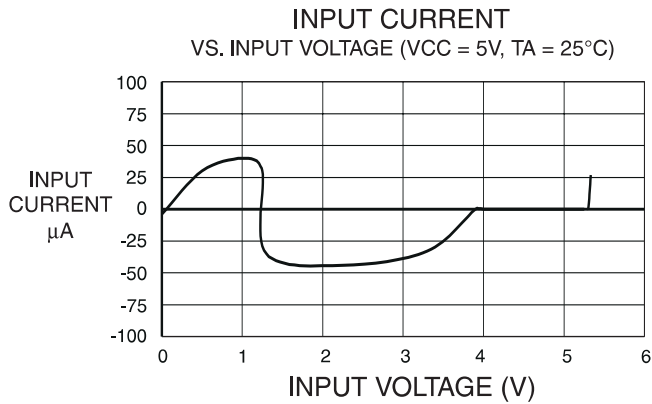
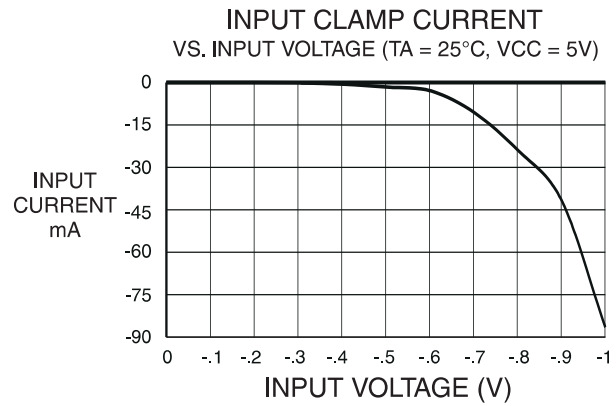
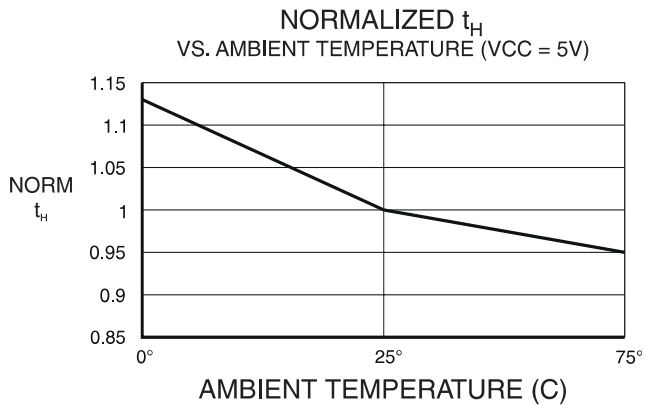
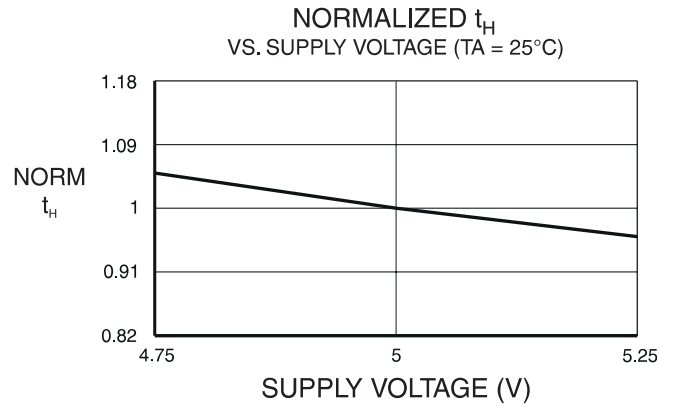
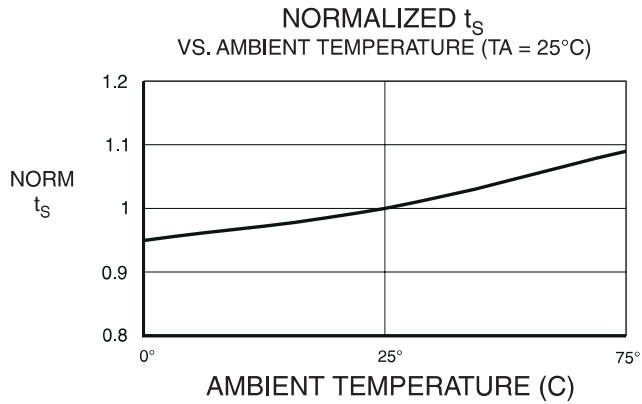


NORMALIZED  $t_{CO}$   
VS. AMBIENT TEMPERATURE (VCC = 5V)



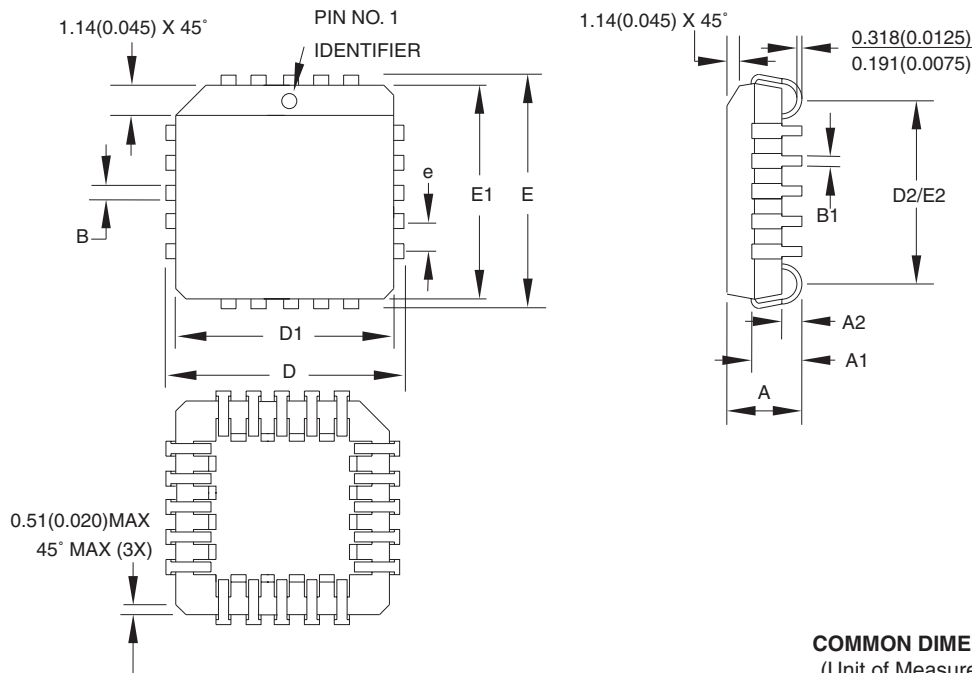
NORMALIZED  $t_S$   
VS. SUPPLY VOLTAGE (TA = 25°C)





## 11. Package Information

### 11.1 20J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | —   | 4.572  |        |
| A1     | 2.286     | —   | 3.048  |        |
| A2     | 0.508     | —   | —      |        |
| D      | 9.779     | —   | 10.033 |        |
| D1     | 8.890     | —   | 9.042  | Note 2 |
| E      | 9.779     | —   | 10.033 |        |
| E1     | 8.890     | —   | 9.042  | Note 2 |
| D2/E2  | 7.366     | —   | 8.382  |        |
| B      | 0.660     | —   | 0.813  |        |
| B1     | 0.330     | —   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

#### TITLE

**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)

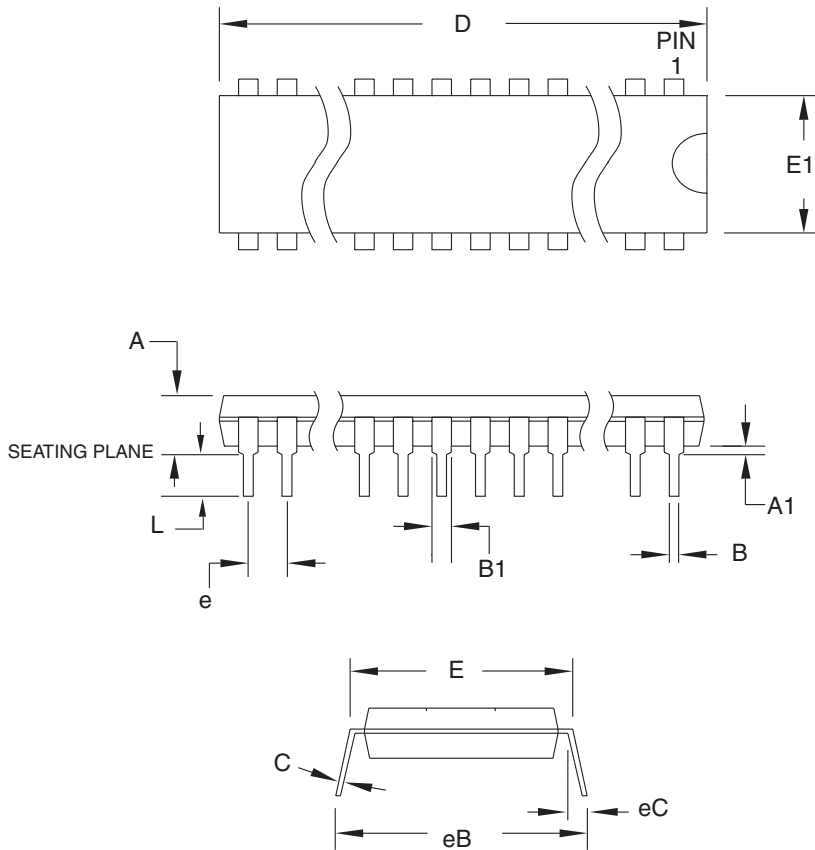
#### DRAWING NO.

20J

#### REV.

B

## 11.2 20P3 – PDIP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | –         | –   | 5.334  |        |
| A1     | 0.381     | –   | –      |        |
| D      | 24.892    | –   | 26.924 | Note 2 |
| E      | 7.620     | –   | 8.255  |        |
| E1     | 6.096     | –   | 7.112  | Note 2 |
| B      | 0.356     | –   | 0.559  |        |
| B1     | 1.270     | –   | 1.551  |        |
| L      | 2.921     | –   | 3.810  |        |
| C      | 0.203     | –   | 0.356  |        |
| eB     | –         | –   | 10.922 |        |
| eC     | 0.000     | –   | 1.524  |        |
| e      | 2.540 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-001, Variation AD.
  2. Dimensions D and E1 do not include mold Flash or Protrusion.  
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/23/04



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual  
Inline Package (PDIP)

### DRAWING NO.

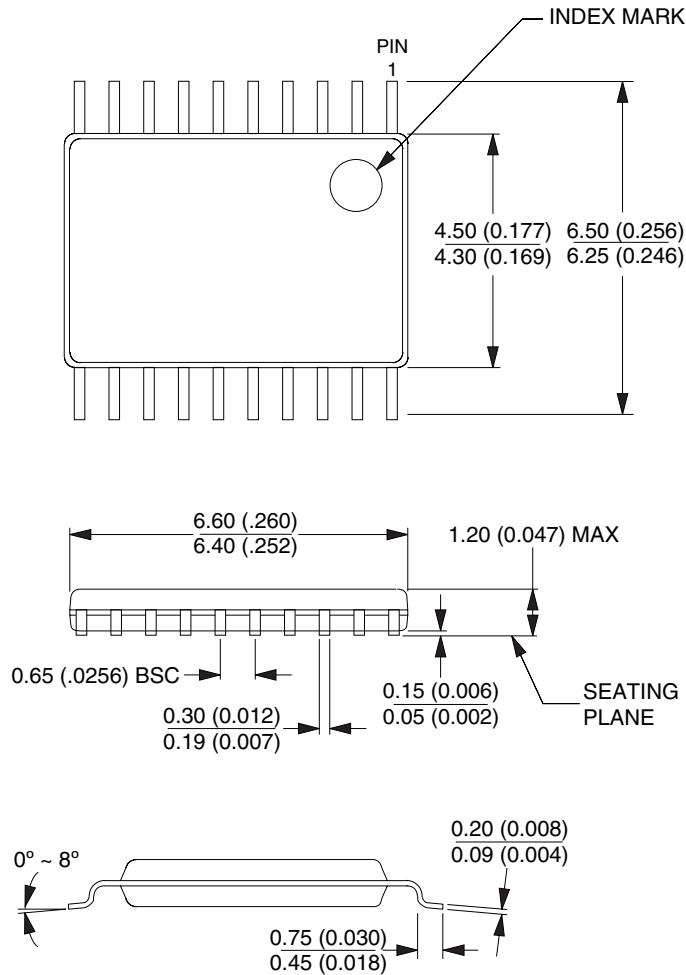
20P3

### REV.

D

## 11.4 20X – TSSOP

Dimensions in Millimeters and (Inches).  
Controlling dimension: Millimeters.  
JEDEC Standard MO-153 AC



10/23/03



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width,  
Plastic Thin Shrink Small Outline Package (TSSOP)

### DRAWING NO.

20X

### REV.

C