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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART, USB
Peripherals	PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-30°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-SQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f1a32auwa-2h

■SIO
- SIO0: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 512/3 tCYC
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO4: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  3) Automatic continuous data transmission (1 to 2048 bytes, specifiable in 1 byte units, suspension and resumption of data transmission possible in 1 byte or 2 bytes units)
  4) Auto-start-on-falling-edge function
  5) Clock polarity selectable
  6) CRC16 calculator circuit built in

■Full Duplex UART
  1) Data length: 7/8/9 bits selectable
  2) Stop bits: 1 bit (2 bits in continuous transmission mode)
  3) Baud rate: 16/3 to 8192/3 tCYC

■AD Converter: 12 bits × 12 channels
- 12-/8-bit resolution selectable AD converter
- Reference-voltage automatic generation control

■PWM: Multifrequency 12-bit PWM × 2 channels

■Infrared Remote Controller Receiver Circuit
  1) Noise rejection function (noise filter time constant: Approx. 120μs when the 32.768kHz crystal oscillator is selected as the reference voltage source)
  2) Supports data encoding systems such as PPM (Pulse Position Modulation) and Manchester encoding
  3) X'tal HOLD mode release function

■USB Interface (function controller)
- Compliant with USB 2.0 Full-Speed
- Supports a maximum of 4 user-defined endpoints.

Endpoint		EP0	EP1	EP2	EP3	EP4
Transfer Type	Control	○	-	-	-	-
	Bulk	-	○	○	○	○
	Interrupt	-	○	○	○	○
	Isochronous	-	○	○	○	○
Max. payload		64	64	64	64	64

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function
  1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
  2) Able to output oscillation clock of sub clock.

LC87F1A32A

■Interrupts
- 28 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/USB bus active/Remote control receive
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/USB bus reset/USB suspend/UART1 receive
8	0003BH	H or L	SIO1/USB endpoint/USB-SOF/SIO4/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/PWM0/PWM1

- Priority Level: X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 1024 levels (the stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits   (5 tCYC execution time)
- 24 bits × 16 bits   (12 tCYC execution time)
- 16 bits ÷ 8 bits   (8 tCYC execution time)
- 24 bits ÷ 16 bits   (12 tCYC execution time)
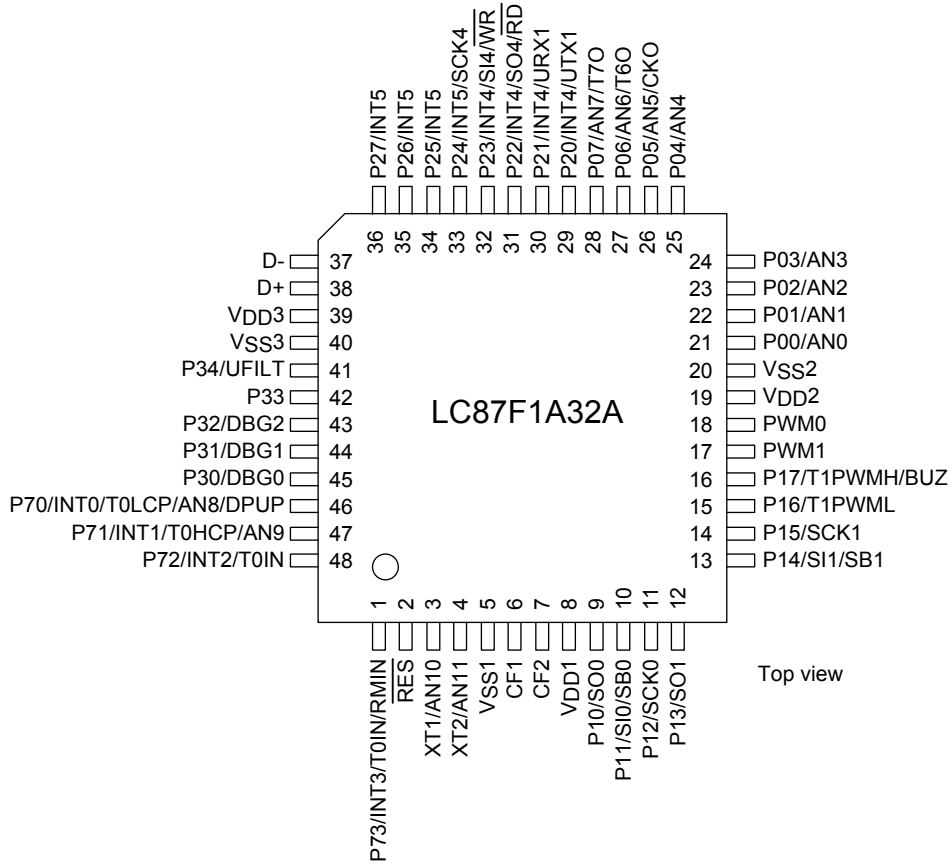
■Oscillation Circuits
- RC oscillation circuit (internal):   For system clock
- CF oscillation circuit: For system clock
- Crystal oscillation circuit: For system clock, time-of-day clock
- PLL circuit (internal):   For USB interface (see Fig.5)

■Standby Function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The PLL base clock generator , CF, RC and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an bus active interrupt source established in the USB interface circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except for reception of a remote control signal.
  1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are six ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit
     (5) Having an bus active interrupt source established in the USB interface circuit
     (6) Having an interrupt source established in the infrared remote controller receiver circuit

LC87F1A32A

Pin Assignment

SQFP48(7×7) "Lead-free Type"

SQFP48	NAME	SQFP48	NAME
1	P73/INT3/T0IN/RMIN	25	P04/AN4
2	$\overline{RES}$	26	P05/AN5/CKO
3	XT1/AN10	27	P06/AN6/T6O
4	XT2/AN11	28	P07/AN7/T7O
5	V$_{SS}$1	29	P20/INT4/UTX1
6	CF1	30	P21/INT4/URX1
7	CF2	31	P22/INT4/SO4/$\overline{RD}$
8	V$_{DD}$1	32	P23/INT4/SI4/$\overline{WR}$
9	P10/SO0	33	P24/INT5/SCK4
10	P11/SI0/SB0	34	P25/INT5
11	P12/SCK0	35	P26/INT5
12	P13/SO1	36	P27/INT5
13	P14/SI1/SB1	37	D-
14	P15/SCK1	38	D+
15	P16/T1PWML	39	V$_{DD}$3
16	P17/T1PWMH/BUZ	40	V$_{SS}$3
17	PWM1	41	P34/UFILT
18	PWM0	42	P33
19	V$_{DD}$2	43	P32/DBGP2
20	V$_{SS}$2	44	P31/ DBGP1
21	P00/AN0	45	P30/ DBGP0
22	P01/AN1	46	P70/INT0/T0LCP/AN8/DPUP
23	P02/AN2	47	P71/INT1/T0HCP/AN9
24	P03/AN3	48	P72/INT2/T0IN

Pin Description

Pin Name	I/O	Description	Option
V$_{SS}$1, V$_{SS}$2, V$_{SS}$3	-	- power supply pin	No
V$_{DD}$1, V$_{DD}$2	-	+ power supply pin	No
V$_{DD}$3	-	USB reference voltage pin	Yes

Port 0
P00 to P07
	I/O	• 8-bit I/O port
		• I/O specifiable in 4-bit units
		• Pull-up resistors can be turned on and off in 4-bit units.
		• HOLD reset input
		• Port 0 interrupt input
		• Pins functions
		  AD converter input port: AN0 to AN7 (P00 to P07)
		  P05: System Clock Output
		  P06: Timer 6 toggle outputs
		  P07: Timer 7 toggle outputs
			Yes

Port 1
P10 to P17
	I/O	• 8-bit I/O port
		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1-bit units.
		• Pin functions
		  P10: SIO0 data output
		  P11: SIO0 data input/bus I/O
		  P12: SIO0 clock I/O
		  P13: SIO1 data output
		  P14: SIO1 data input/bus I/O
		  P15: SIO1 clock I/O
		  P16: Timer 1 PWML output
		  P17: Timer 1 PWMH output/beeper output
			Yes

Port 2
P20 to P27
	I/O	• 8-bit I/O port
		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1-bit units.
		• Pin functions
		  P20 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/
		        timer 0H capture input
		  P24 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/
		        timer 0H capture input
		  P20: UART1 transmit
		  P21: UART1 receive
		  P22: SIO4 date I/O/parallel interface $\overline{RD}$ output
		  P23: SIO4 date I/O/parallel interface $\overline{WR}$ output
		  P24: SIO4 clock I/O
		  Interrupt acknowledge type
			Yes

	Rising	Falling	Rising & Falling	H level	L level
INT4	enable	enable	enable	disable	disable
INT5	enable	enable	enable	disable	disable

LC87F1A32A

Pin Name	I/O	Description	Option

Port 3
 	
P30 to P34
	I/O	• 5-bit I/O port
		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1-bit units.
		• Pin functions
		  P34: USB interface PLL filter pin (see Fig.5)
		  Onchip debugger pin: DBGP0 to DBGP2 (P30 to P32)
			Yes

Port 7
 	
P70 to P73
	I/O	• 4-bit I/O port
		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1-bit units.
		• Pin functions
		  P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output/
		     D+ 1.5kΩ pull-up resistor connect pin
		  P71: INT1 input/HOLD reset input/timer 0H capture input
		  P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/
		     High speed clock counter input
		  P73: INT3 input (input with a noise filter)/timer 0 event input/ timer 0H capture input/
		     infrared remote controller receiver input
		  AD converter input port: AN8(P70), AN9(P71)
		Interrupt acknowledge type
		
		<table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising & Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>
			No

PWM0 PWM1	I/O	• PWM0 and PWM1 output port • General-purpose input port	No
D-	I/O	• USB data I/O pin D- • General-purpose I/O port	No
D+	I/O	• USB data I/O pin D+ • General-purpose I/O port	No
$\overline{\text{RES}}$	Input	Reset pin	No

XT1	Input	• 32.768kHz crystal oscillator input pin
		• Pin functions
		  General-purpose input port
		  AD converter input port: AN10
		Must be connected to $V_{DD}1$ if not to be used.
			No

XT2	I/O	32.768kHz crystal oscillator output pin
		• Pin functions
		  General-purpose I/O port
		  AD converter input port: AN11
		Must be set for oscillation and kept open if not to be used.
			No

CF1	Input	Ceramic resonator input pin	No
CF2	Output	Ceramic resonator output pin	No

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

| Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
P20 to P27		2	Nch-open drain	Programmable
P30 to P34				
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
PWM0, PWM1	-	No	CMOS	No
D+, D-	-	No	CMOS	No
XT1	-	No	Input only	No
XT2	-	No	32.768kHz crystal oscillator output (Nch-open drain when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

Power Pin Treatment

Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.

Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ pins.

Example 1: When the microcontroller is in the backup state in the HOLD mode, the power to sustain the high level of output ports is supplied by their backup capacitors.
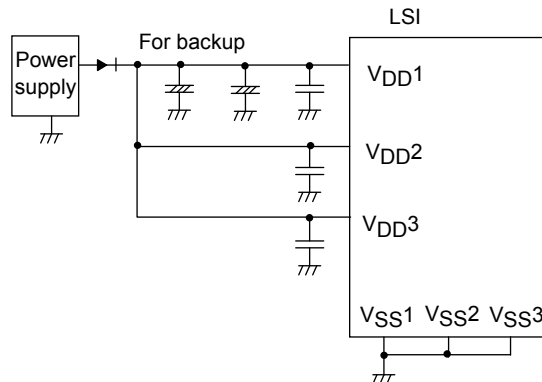
Example 2: The high level output at ports is not sustained and unstable in the HOLD backup mode.
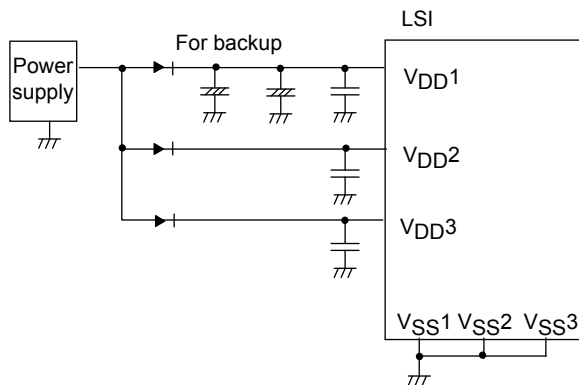
USB Reference Power Option

When a voltage 4.4 to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of reference voltage circuit can be switched by the option select. The procedure for marking the option selection is described below.

		(1)	(2)	(3)	(4)
Option select	USB Regulator	USE	USE	USE	NONUSE
	USB Regulator at HOLD mode	USE	NONUSE	NONUSE	NONUSE
	USB Regulator at HALT mode	USE	NONUSE	USE	NONUSE
Reference voltage circuit state	Normal state	active	active	active	inactive
	HOLD mode	active	inactive	inactive	inactive
	HALT mode	active	inactive	active	inactive

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for USB port output is equal to $V_{DD}1$.
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increase by approximately 100μA compared with when the reference voltage circuit is inactive.
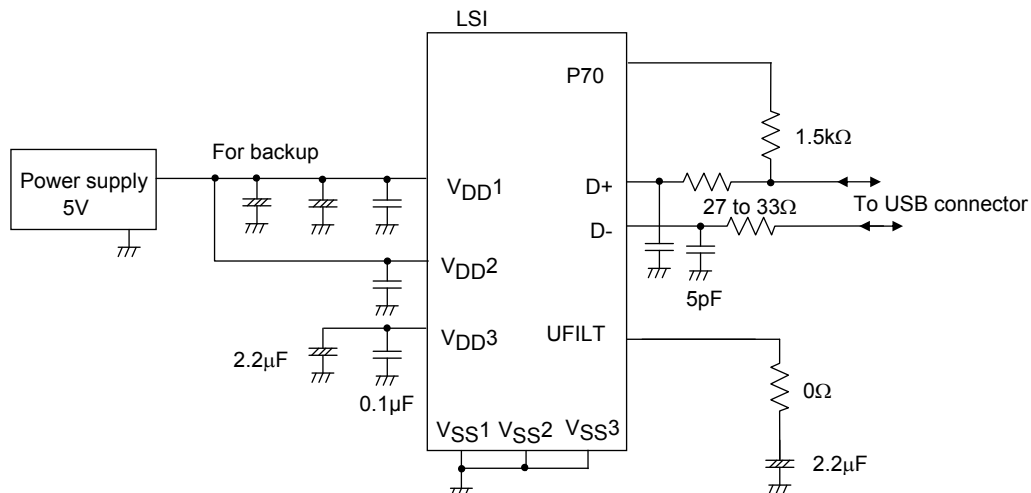
Example 1: $V_{DD}1=V_{DD}2=3.3V$
- Inactivating the reference voltage circuit (selection (4)).
- Connecting $V_{DD}3$ to $V_{DD}1$ and $V_{DD}2$.
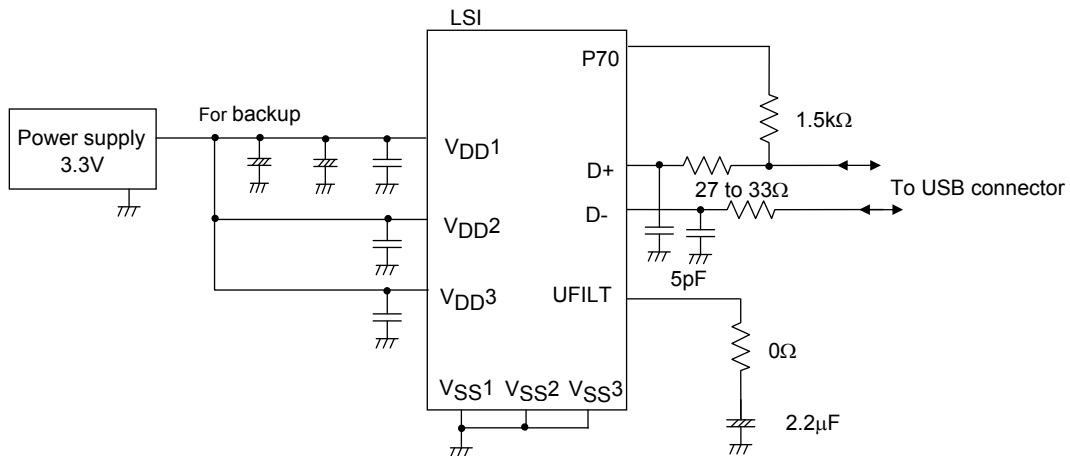
Example 2: $V_{DD}1=V_{DD}2=5.0V$
- Activating the reference voltage circuit (selection (1)).
- Isolating $V_{DD}3$ from $V_{DD}1$ and $V_{DD}2$, and connecting capacitor between $V_{DD}3$ and V_{SS}.

Absolute Maximum Ratings at $Ta = 25°C$, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		−0.3		+6.5	V
Input voltage		V_I(1)	XT1, CF1			−0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2, 3, 7 PWM0, PWM1, XT2			−0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		−10			mA
		IOPH(2)	PWM0, PWM1	Per 1 applicable pin		−20			
		IOPH(3)	Ports 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		−5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		−7.5			
		IOMH(2)	PWM0, PWM1	Per 1 applicable pin		−15			
		IOMH(3)	Ports 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		−3			
	Total output current	ΣIOAH(1)	Ports 0, 2	Total of all applicable pins		−25			
		ΣIOAH(2)	Port 1 PWM0, PWM1	Total of all applicable pins		−25			
		ΣIOAH(3)	Ports 0, 1, 2 PWM0, PWM1	Total of all applicable pins		−45			
		ΣIOAH(4)	Ports 3 P71 to P73	Total of all applicable pins		−10			
		ΣIOAH(5)	D+, D−	Total of all applicable pins		−25			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Ports 3, 7, XT2	Per 1 applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Ports 3, 7, XT2	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Ports 0, 2	Total of all applicable pins				45	
		ΣIOAL(2)	Port 1 PWM0, PWM1	Total of all applicable pins				45	
		ΣIOAL(3)	Ports 0, 1, 2 PWM0, PWM1	Total of all applicable pins				80	
		ΣIOAL(4)	Ports 3, 7, XT2	Total of all applicable pins				15	
		ΣIOAL(5)	D+, D−	Total of all applicable pins				25	
Allowable power Dissipation		Pd max	SQFP48(7×7)	Ta=-30to+70°C				190	mW
Operating ambient Temperature		Topr				−30		+70	°C
Storage ambient temperature		Tstg				−55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

LC87F1A32A

Electrical Characteristics at Ta = −30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1 D+, D−	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.7 to 5.5			1	μA
	$I_{IH}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{DD}$	2.7 to 5.5			1	
	$I_{IH}(3)$	CF1	$V_{IN}=V_{DD}$	2.7 to 5.5			15	
Low level input current	$IIL(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1 D+, D−	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.7 to 5.5	−1			
	$I_{IL}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{SS}$	2.7 to 5.5	−1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	2.7 to 5.5	−15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3 P71 to P73	$I_{OH}=−1mA$	4.5 to 5.5	$V_{DD}−1$			
	$V_{OH}(2)$		$I_{OH}=−0.4mA$	3.0 to 5.5	$V_{DD}−0.4$			
	$V_{OH}(3)$		$I_{OH}=−0.2mA$	2.7 to 5.5	$V_{DD}−0.4$			
	$V_{OH}(4)$	PWM0, PWM1 P05 (CK0 when using system clock output function)	$I_{OH}=−10mA$	4.5 to 5.5	$V_{DD}−1.5$			
	$V_{OH}(5)$		$I_{OH}=−1.6mA$	3.0 to 5.5	$V_{DD}−0.4$			
	$V_{OH}(6)$		$I_{OH}=−1mA$	2.7 to 5.5	$V_{DD}−0.4$			
Low level output voltage	$V_{OL}(1)$	P00, P01	$I_{OL}=30mA$	4.5 to 5.5			1.5	V
	$V_{OL}(2)$		$I_{OL}=5mA$	3.0 to 5.5			0.4	
	$V_{OL}(3)$		$I_{OL}=2.5mA$	2.7 to 5.5			0.4	
	$V_{OL}(4)$	Ports 0, 1, 2 PWM0, PWM1 XT2	$I_{OL}=10mA$	4.5 to 5.5			1.5	
	$V_{OL}(5)$		$I_{OL}=1.6mA$	3.0 to 5.5			0.4	
	$V_{OL}(6)$		$I_{OL}=1mA$	2.7 to 5.5			0.4	
	$V_{OL}(7)$	Ports 3, 7	$I_{OL}=1.6mA$	3.0 to 5.5			0.4	
	$V_{OL}(8)$		$I_{OL}=1mA$	2.7 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.7 to 5.5	18	50	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Ports 1, 2, 3, 7		2.7 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.7 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Serial I/O Characteristics at Ta = −30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig.9.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transmission/ reception mode • USB nor SIO4 are not in use simultaneous. • See Fig.8. • (Note 4-1-2)		4			
			tSCKHA(1b)		• Continuous data transmission/reception mode • USB is in use simultaneous. • SIO4 is not in use simultaneous. • See Fig.8. • (Note 4-1-2)		7			
			tSCKHA(1c)		• Continuous data transmission/ reception mode • USB and SIO4 are in use simultaneous. • See Fig.8. • (Note 4-1-2)		9			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig.8.	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)					1/2		
		High level pulse width	tSCKH(2)					1/2		
			tSCKHA(2a)		• Continuous data transmission/ reception mode • USB nor SIO4 are not in use simultaneous. • CMOS output selected • See Fig.8.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
			tSCKHA(2b)		• Continuous data transmission/ reception mode • USB is in use simultaneous. • SIO4 is not in use simultaneous. • CMOS output selected • See Fig.8.		tSCKH(2) +2tCYC		tSCKH(2) +(19/3) tCYC	
			tSCKHA(2c)		• Continuous data transmission/ reception mode • USB and SIO4 are in use simultaneous. • CMOS output selected • See Fig.8.		tSCKH(2) +2tCYC		tSCKH(2) +(25/3) tCYC	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Continued from preceding page.

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Serial input	Data setup time	tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig.8.	2.7 to 5.5	0.03			μs
	Data hold time	thDI(1)			2.7 to 5.5	0.03			
Serial output	Input clock — Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	
		tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.7 to 5.5			1tCYC +0.05	
	Output clock	tdD0(3)		(Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig.8.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig.8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig.8.	2.7 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)					1/2		
		High level pulse width	tSCKH(4)					1/2		
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig.8.	2.7 to 5.5	0.03			μs
	Data hold time		thDI(2)			2.7 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig.8.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

3. SIO4 Serial I/O Characteristics (Note 4-3-1)

Parameter			Symbol	Pin/ Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(5)	SCK4(P24)	See Fig.8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(5)				1			
		High level pulse width	tSCKH(5)				1			
			tSCKHA(5a)		• USB nor continuous data Transmission/reception mode Of SIO0 are not in use simultaneous. • See Fig.8. • (Note 4-3-2)		4			
			tSCKHA(5b)		• USB is in use simultaneous. • Do not use SIO0 continuous data transmission mode at the same time. • See Fig.8. • (Note 4-3-2)		7			
			tSCKHA(5c)		• USB and continuous data transmission/ reception mode of SIO0 are in use simultaneous. • See Fig.8. • (Note 4-3-2)		10			
	Output clock	Frequency	tSCK(6)	SCK4(P24)	• CMOS output selected • See Fig.8	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(6)					1/2		
		High level pulse width	tSCKH(6)					1/2		
			tSCKHA(6a)		• USB, AIF nor continuous data transmission/reception mode of SIO0 are not in use simultaneous. • CMOS output selected • See Fig.8.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(10/3) tCYC	tCYC
			tSCKHA(6b)		• USB is in use simultaneous. • Do not use SIO0 continuous data transmission mode at the same time. • CMOS output selected • See Fig8.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(19/3) tCYC	
			tSCKHA(6c)		• USB and continuous data transmission/reception mode of SIO0 are in use simultaneous. • CMOS output selected • See Fig.8.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(28/3) tCYC	
Serial input		Data setup time	tsDI(3)	SO4(P22), SI4(P23)	• Must be specified with respect to rising edge of SIOCLK. • See Fig.8.	2.7 to 5.5	0.03			μs
		Data hold time	thDI(3)			2.7 to 5.5	0.03			

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input in continuous trans/rec mode, a time from SI4RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Continued from preceding page.

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V$_{DD}$[V]	min	typ	max	unit
Serial output	Output delay time	tdD0(5)	SO4(P22), SI4(P23)	• Must be specified with respect to rising edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig.8.	2.7 to 5.5			(1/3)tCYC +0.05	μs

Pulse Input Conditions at Ta = −30°C to +70°C, V$_{SS}$1 = V$_{SS}$2 = V$_{SS}$3 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V$_{DD}$[V]	min	typ	max	unit
High/low level pulse width	tP1H(1) tP1L(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	256			
	tPIL(5)	RMIN(P73)	Recognized by the infrared remote controller receiver circuit as a signal.	2.7 to 5.5	4			RMCK (Note 5-1)
	tPIL(6)	$\overline{RES}$	Resetting is enabled.	2.7 to 5.5	200			μs

Note5-1: Represents the period of the reference clock (1 tCYC to 128 tCYC or the source frequency of the subclock) for the infrared remote controller receiver circuit.

LC87F1A32A

AD Converter Characteristics at Ta= −30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12-bits AD Converter Mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	μs
				3.0 to 5.5	64		115	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	−1			

<8-bits AD Converter Mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		90	μs
				3.0 to 5.5	40		90	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	−1			

Conversion time calculation formulas:

12-bits AD Converter Mode: TCAD (Conversion time) = $((52/(\text{AD division ratio}))+2) \times (1/3) \times t_{CYC}$

8-bits AD Converter Mode: TCAD (Conversion time) = $((32/(\text{AD division ratio}))+2) \times (1/3) \times t_{CYC}$

<Recommended Operating Conditions>

External oscillator FmCF[MHz]	Supply Voltage Range V_{DD}[V]	System Clock Division (SYSDIV)	Cycle Time tCYC [ns]	AD Frequency Division Ratio (ADDIV)	Conversion Time (TCAD)[μs]	
					12-bit AD	8-bit AD
12	4.0 to 5.5	1/1	250	1/8	34.8	21.5
	3.0 to 5.5	1/1	250	1/16	69.5	42.8

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:
- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = −30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				$V_{DD}[V]$	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ $=V_{DD}2$ $=V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration	4.4 to 5.5		9.8	24	
	IDDOP(2)			3.0 to 3.6		5.6	14	
	IDDOP(3)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit operation mode • 1/1 frequency division ration	4.4 to 5.5		14	34	
	IDDOP(4)			3.0 to 3.6		7.7	19	mA
	IDDOP(5)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/2 frequency division ration	4.4 to 5.5		6.1	14	
	IDDOP(6)			3.0 to 3.6		3.7	8.5	
	IDDOP(7)			2.7 to 3.0		3.0	6.7	
	IDDOP(8)		• FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ration	4.4 to 5.5		0.63	3.0	
	IDDOP(9)			3.0 to 3.6		0.35	1.6	
	IDDOP(10)			2.7 to 3.0		0.30	1.3	
	IDDOP(11)		• FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ration	4.4 to 5.5		39	150	
	IDDOP(12)			3.0 to 3.6		17	58	μA
	IDDOP(13)			2.7 to 3.0		14	43	
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ $=V_{DD}2$ $=V_{DD}3$	• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ration	4.4 to 5.5		4.9	12	
	IDDHALT(2)			3.0 to 3.6		2.6	6.3	
	IDDHALT(3)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation mode • Internal RC oscillation stopped • USB circuit operation mode • 1/1 frequency division ration	4.4 to 5.5		8.9	23	
	IDDHALT(4)			3.0 to 3.6		4.6	12	mA
	IDDHALT(5)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/2 frequency division ration	4.4 to 5.5		3.0	7.2	
	IDDHALT(6)			3.0 to 3.6		1.6	3.8	
	IDDHALT(7)			2.7 to 3.0		1.3	2.9	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V$_{DD}$[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(8)	V$_{DD}$1 =V$_{DD}$2 =V$_{DD}$3	• HALT mode • FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ration	4.4 to 5.5		0.37	1.8	mA
	IDDHALT(9)			3.0 to 3.6		0.18	0.83	
	IDDHALT(10)			2.7 to 3.0		0.15	0.62	
	IDDHALT(11)		• HALT mode • FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ration	4.4 to 5.5		24	93	
	IDDHALT(12)			3.0 to 3.6		7.9	33	
	IDDHALT(13)			2.7 to 3.0		5.8	22	
HOLD mode consumption current	IDDHOLD(1)	V$_{DD}$1	HOLD mode • CF1=V$_{DD}$ or open (External clock mode)	4.4 to 5.5		0.08	24	μA
	IDDHOLD(2)			3.0 to 3.6		0.03	11	
	IDDHOLD(3)			2.7 to 3.0		0.02	9.6	
Timer HOLD mode consumption current	IDDHOLD(4)	V$_{DD}$1	Timer HOLD mode • CF1=V$_{DD}$ or open (External clock mode) • FsX'tal=32.768kHz crystal oscillation mode	4.4 to 5.5		19	77	
	IDDHOLD(5)			3.0 to 3.6		5.1	23	
	IDDHOLD(6)			2.7 to 3.0		3.3	14	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

USB Characteristics and Timing at Ta = 0°C to +70°C, V$_{SS}$1 = V$_{SS}$2 = V$_{SS}$3 = 0V

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
High level output	V$_{OH(USB)}$	• 15kΩ±5% to GND	2.8		3.6	V
Low level output	V$_{OL(USB)}$	• 1.5kΩ±5% to 3.6 V	0.0		0.3	V
Output signal crossover voltage	V$_{CRS}$		1.3		2.0	V
Differential input sensitivity	V$_{DI}$	• |(D+)–(D−)|	0.2			V
Differential input common mode range	V$_{CM}$		0.8		2.5	V
High level input	V$_{IH(USB)}$		2.0			V
Low level input	V$_{IL(USB)}$				0.8	V
USB data rise time	t$_R$	• R$_S$=27 to 33Ω, CL=50pF • V$_{DD}$3=3.0 to 3.6V	4		20	ns
USB data fall time	t$_F$	• R$_S$=27 to 33Ω, CL=50pF • V$_{DD}$3=3.0 to 3.6V	4		20	ns

F-ROM Programming Characteristics at Ta = +10°C to +55°C, V$_{SS}$1 = V$_{SS}$2= V$_{SS}$3 =0V

Parameter	Symbol	Pin	Conditions	Specification				
				V$_{DD}$[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	V$_{DD}$1	• Excluding power dissipation in the microcontroller block	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		• Erase operation	3.0 to 5.5		20	30	ms
	tFW(2)		• Write operation			40	60	μs

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator
　　　　at Ta = 0°C to +70°C

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
6MHz	MURATA	CSTCR6M00G15L**-R0	(39)	(39)	680	2.7 to 5.5	0.05	0.50	Built-in C1, C2
8MHz	MURATA	CSTCE8M00G15L**-R0	(33)	(33)	220	3.0 to 5.5	0.05	0.50	
10MHz	MURATA	CSTCE10M0G15L**-R0	(33)	(33)	220	3.0 to 5.5	0.05	0.50	
12MHz	MURATA	CSTCE12M0G15L**-R0	(33)	(33)	330	3.0 to 5.5	0.05	0.50	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a CF Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	OPEN	560k	2.7 to 5.5	1.1	3.0	Applicable CL value=12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.
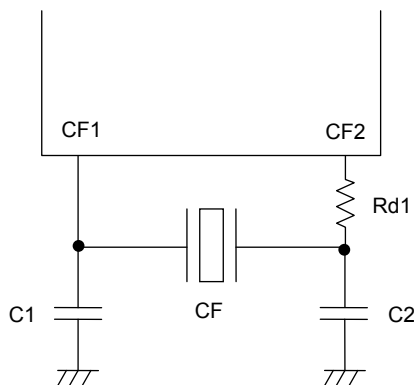
Figure 1 CF Oscillator Circuit　　　　Figure 2 XT Oscillator Circuit
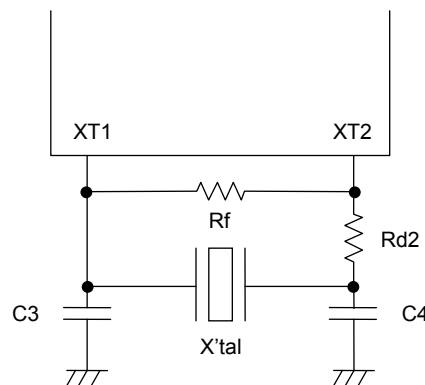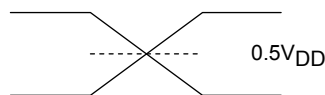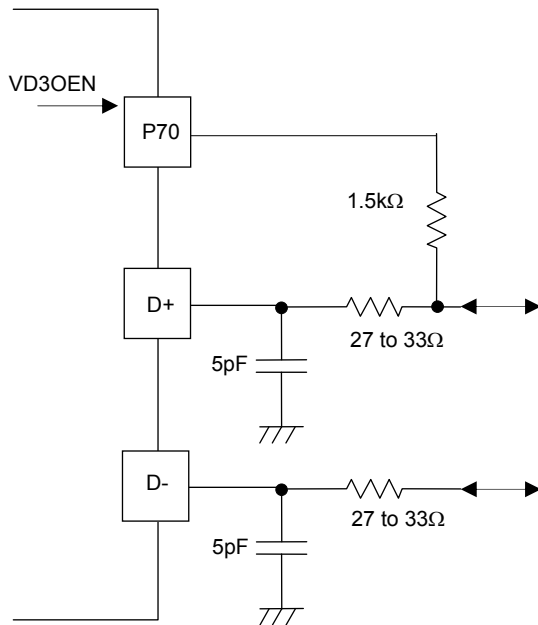


Figure 3 AC Timing Measurement Point
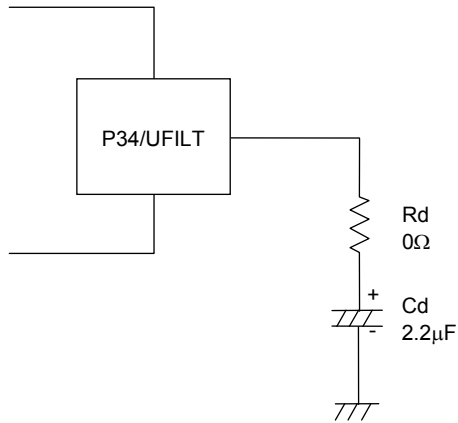
When using the internal PLL circuit to generate the 48 MHz clock for USB , it is necessary to connect a filter circuit such as that shown to the left to the P34/UFILT pin.

Figure 5 External Filter Circuit for the Internal USB-dedicated PLL Circuit

Note:
It's necessary to adjust the Circuit Constant of the USB Port Peripheral Circuit each mounting board. Make the D+ Pull-up resistors available to control on/off according to the Vbus.

Figure 6 USB Port Peripheral Circuit
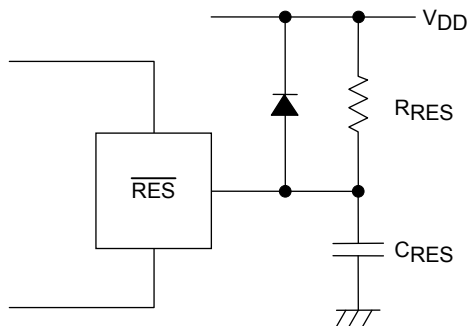
Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 7 Reset Circuit
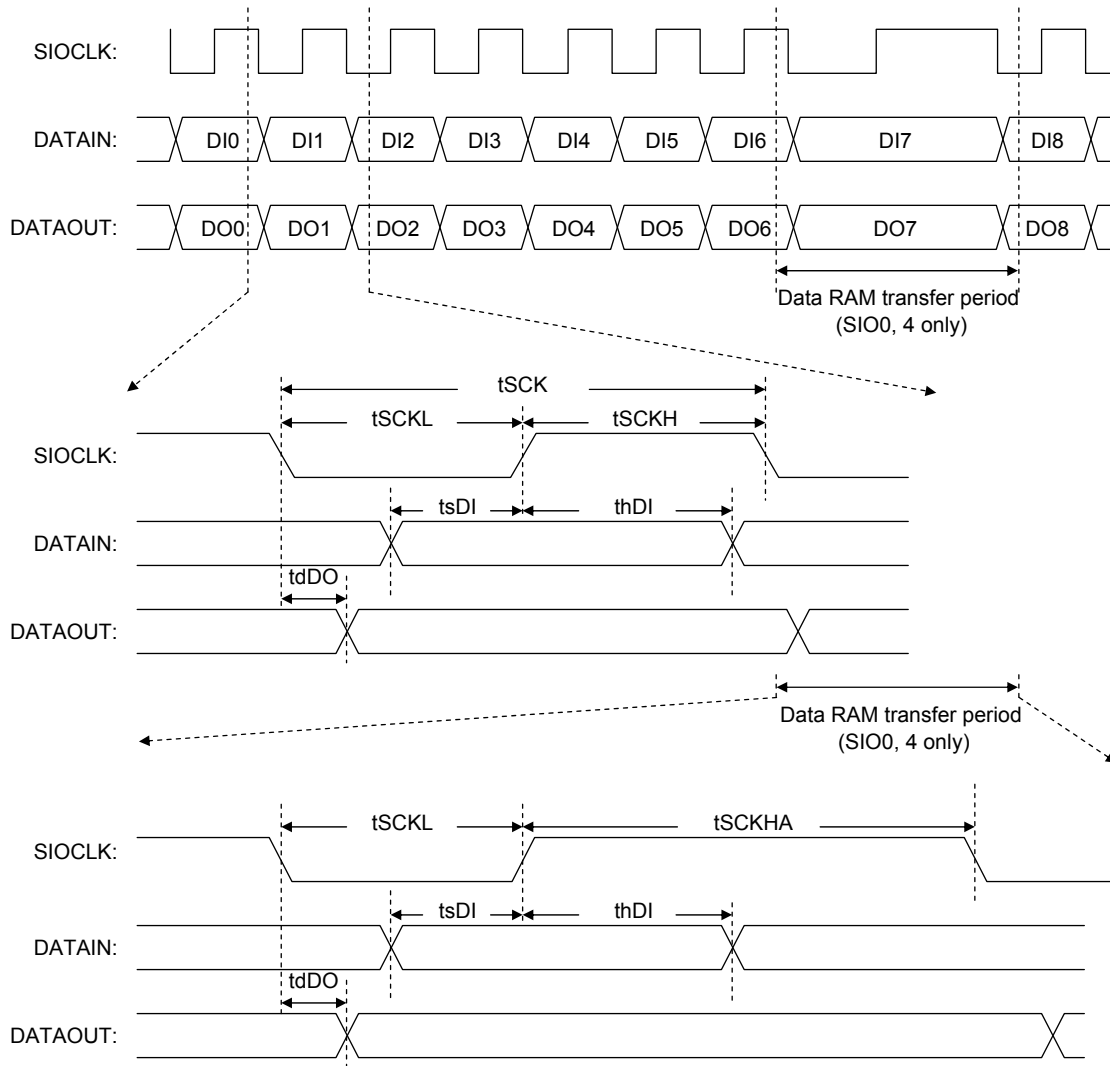
Figure 8 Serial I/O Waveforms
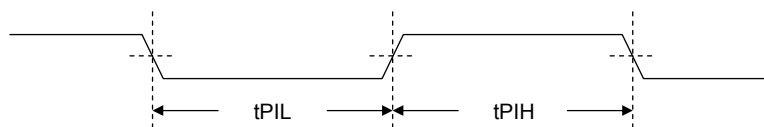
Figure 9 Pulse Input Timing Signal Waveform
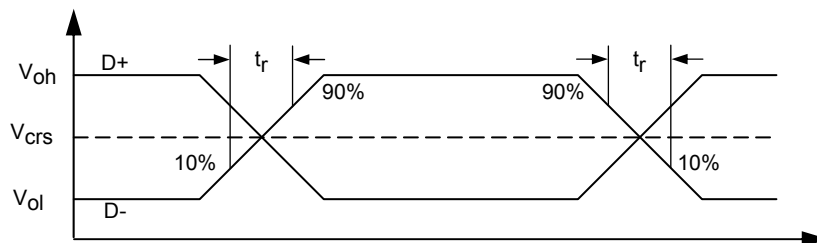
Figure 10 USB Data Signal Timing and Voltage Level

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F1A32AUWA-2H	SPQFP-48 / SQFP-48 (Pb-Free / Halogen Free)	2500 / Tray JEDEC