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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	Host Interface, PS/2, SMBus, UART/USART
Peripherals	PWM, WDT
Number of I/O	104
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w83l951dg

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP72 MPS2_CLK	46	I/O16tsh	General Purpose I/O Function Mouse PS2 Clock Signal
GP71 KPS2_DAT	47	I/O16tsh	General Purpose I/O Function Keyboard PS2 Data Signal
GP70 KPS2_CLK	48	I/O16tsh	General Purpose I/O Function Keyboard PS2 Clock Signal
VCC1	49	Ivdd	Normal Power Input, +3.3V
RESET#	50	I_{ts}	System Reset.
LCLK	51	Its	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	Its	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	Its	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O24ts	Serial IRQ input/Output.
GND	55	Ivss	Normal GND
LAD0	56	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LPWRSTS	60	Its	Power status. Indicates current power status of LPC interface.
GP47	61	I/O16tsh	General Purpose I/O Function
GP46 CLKRUN#	62	I/O16tsh	General Purpose I/O Function Advance LPC function: It is used to request starting the clock
GP45 GATE_A20	63	I/O16tsh	General Purpose I/O Function Gate A20 output
GP44 KBRST#	64	I/O16tsh	General Purpose I/O Function CPU reset output

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP43 TXD	65	I/O16tsh	General Purpose I/O Function UART TX output
GP42 RXD	66	I/O16tsh	General Purpose I/O Function UART RX Input
GP41 FAN_TACH1	67	I/O16tsh	General Purpose I/O Function Fan tachometer 1
GP40 FAN_TACH0	68	I/O16tsh	General Purpose I/O Function Fan tachometer 0
SYMBOL	PIN	I/O	FUNCTION
GND	69	Ivss	Normal GND
GP27 PWM3	70	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP26 PWM2	71	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP25 PWM1	72	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP24 PWM0	73	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP23 KC19	74	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP22 KC18	75	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP21 KC17	76	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP20 KC16	77	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
VCC1	78	Ivdd	Normal Power Input, +3.3V
GP17 KC15 FA15	79	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP51	120	I/O16tsh	General Purpose I/O Function
GP50	121	I/O16tsh	General Purpose I/O Function
XOUT	122	Oc	24MHz/12MHz System Clock Output
XIN	123	Ic	24MHz/12MHz System Clock Input
TEST#	124	I_{ts}	Test pin to provide different operation.
XCOUT	125	Oc	32.768 KHz Clock Output
XCIN	126	Ic	32.768 KHz Clock Input
GPC7 EXTINT37	127	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC6 EXTINT36	128	I/O16tsh	General Purpose I/O Function External Interrupt Input

5.2 RESET# & TEST# Part

Table 5-3 RESET# & TEST# pin configuration table

SYMBOL	PIN	I/O	FUNCTION
RESET#	50	I_{ts}	System Reset.
TEST#	124	I_{ts}	Test pin to provide different operation.

In W83L951DG/FG, RESET# Pin and TEST# Pin decide the status of W83L951DG/FG to provide 4 operations.

TEST#	RESET#	CHIP CURRENT STATUS
0	0	Internal Flash Access Interface Enable
0	1	Reserved
1	0	Normal Reset
1	1	Normal Operation

5.3 LPC Interface Part

LPC Interface is formed by LAD0~LAD3, SERIRQ, LRESET#, LFRAME#, LCLK and VCC2. These pins are defined by LPC interface Spec except VCC2. Below are descriptions about all LPC pins:

Table 5-4 LPC interface pin configuration table

SYMBOL	PIN	I/O	FUNCTION
LCLK	51	I_{ts}	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	I_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	I_{ts}	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O_{24ts}	Serial IRQ input/Output.
LAD0	56	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.

Note: Other pins about LPC interface, CLKRUN#: Please see “GP4” part.VCC2: Please see “power & clock” part.

5.4 GPIO0 Part

This part contains:

General Purpose I/O Function

Default is General Purpose I/O. Change the value of GPIO0 and GPIOD0 register to determine 8 input/output.

Keyboard Matrix Column Output

Use Chipctrl2 register bit 3 to enable {GP0, GP1, GP20~23} keyboard scan and GP3 key wakeup interrupt function.

Internal Flash Access Interface

When TEST# and RESET# are both low, Internal Flash Access Interface is enabled and other functions are disabled.

6. FUNCTIONAL DESCRIPTION

In W83L951DG/FG, memory organization and data type are based on Turbo 51 core controller. Register sets of various function blocks are finished by accessing Special Function Register (SFR).

According to the difference of accessing approaches, SFR are divided into Address Mapping and External RAM Address Mapping.

Internal RAM Address Mapping:

It means to use direct addressing to access 128 bytes from internal RAM address 80H to 0FFH. Function blocks that use Internal RAM Address Mapping are listed below:

Table 6-1 Reset Source Table

NAME	RESET SOURCE
8051 Core	System Reset.
Internal Interrupt Controller	System Reset
PS2 Device Interface	System Reset + PS2 Reset
Low Pin Count Interface Controller	System Reset + LPC Power Fail + LPC Reset
SMBus 1	System Reset + SMBUS1 Reset
SMBus 2	System Reset + SMBUS2Reset
GPIO Controller	System Reset.

Table 6-2 Internal RAM Address Mapping Table

Base on 00h	Index							
Offset	0	1	2	3	4		6	7
80	+GP0	SP	DPL1	DPH1	DPL2	DPH2	ID	VERSION
88	+GP1	CHIPCTRL1	CHIPCTRL2	CHIPCTRL3	DPSEL	INTEN	MMEN	
90	+GP2	KBCCON	LPCCON	DBB0STS	DBB0	DBB0ADDH	DBB0ADDL	SIRQ0
98	+GP3	DBB1STS	DBB1	DBB1ADDH	DBB1ADDL	SIRQ1		
A0	+GP4	KPS2DATA	KPS2CON	KPS2STS	MPS2DATA	MPS2CON	MPS2STS	PS2HSEN
A8	+GP5	APS2DATA	APS2CON	APS2STS				
B0	+GP6	S1CR	S1IREQ	S1IE	S1FIFOCON	S1MFIFO	S1MCON	S1MSTS
B8	+GP7	S1MFIFOSTS	S1SFIFO	S1SCON	S1SSTS	S1SFIFOSTS		
C0	+GP8	S2CR	S2IREQ	S2IE	S2FIFOCON	S2MFIFO	S2MCON	S2MSTS
C8	+GP9	S2MFIFOSTS	S2SFIFO	S2SCON	S2SSTS	S2SFIFOSTS		
D0	+PSW	GPD0	GPD1	GPD2	GPD3	GPD4	GPD5	GPD6
D8	+GPA	GPD7	GPD8	GPD9	GPDA	GPDB	GPDC	
E0	+ACC	IE1	IE2	IE3	IE4			
E8	+GPB	IREQ1	IREQ2	IREQ3	IREQ4			
F0	+B	IP1	IP2	IP3	IP4			
F8	+GPC	FCON	FADDH	FADDL	FDATA			
Index + 8	8	9	A	B	C		E	F

Read Only Reserved + a bit addressable register

6.1.1.18 External Wake-up 2 Register (EXTWKP2) (Default Value: 0000_0000)

Bit7~5: Reserved

Bit4: Enable RTC Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Bit3: Enable LPC Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Bit2: Enable APS2 Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Auxiliary PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

Bit1: Enable MPS2 Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Mouse PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

Bit0: Enable KPS2 Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Keyboard PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

6.3 Personal System 2 Block

The Winbond Keyboard controller has three independent PS/2 serial ports implemented in hardware, which are directly controlled by the on chip 8051. Each of the three PS/2 serial channels uses a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has two signal lines: Clock and Data. Both signal lines are bi-directional and employ open drain. The PS2DATA, PS2CON and PS2STS is defined individually for each PS/2 channel. PS2HSEN is only one register for controlling all PS/2 device handshake action.

Table 6-8 Personal System 2(PS2) Register Define

KEYBOARD & MOUSE & AUXILIARY PS2 BLOCK(9)									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A1	KPS2DATA	KPS2 Data register [7:0]							
A2	KPS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	KPS2T/R
A3	KPS2STS	KPS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY
A4	MPS2DATA	MPS2 Data register [7:0]							
A5	MPS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	MPS2T/R
A6	MPS2STS	MPS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY
A7	PS2HSEN	Reserved							HSEN
A9	APS2DATA	APS2 Data register [7:0]							
AA	APS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	APS2T/R
AB	APS2STS	APS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY

Gray: Only with System Reset to initial.

6.3.1 Register Description

6.3.1.1 PS/2 Handshake Enable Register (PS2HSEN) (Default Value:: 0000_0000)

Bit 7~1: Reserved (always return 'LOW')

Bit 0: Handshake Mode Enable (HSEN)

0: The handshake mode of PS2 disables.

1: The handshake mode of PS2 enables.

When the handshake mode of PS2 is enabling, the TR bit (BIT 0) of PSCON is automatically set high when the START_DEC bit (bit 6) of PS2STS of the other channel is set.

Note:

The priority of three PS2 interface is KPS2 > MPS2 > APS2.

Whether the handshake mode of PS2 is enabled or not, the TR bit (BIT 0) of PSCON is automatically set high when the RDATA_RDY bit (bit 0) of PS2STS of this channel is set.

6.3.1.3 PS/2 Control Registers (PS2CON) (Default Value:: 0000_0000)

Bit 7: NOISE FILTER ENABLE (NFEN)

0: Disable noise filter for clock line

1: Enable noise filter for clock line

Bit 6: Inhibit bit

The low to high transition of the inhibit bit will hold the clock line low for 100us(Input clock=24MHz) or 200us(Input clock=12MHz).

Bit 5-4: STOP

Bits [5:4] of the Control Register are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits [5:4] =

00: Receiver expects an active high stop bit.

01: Receiver expects an active low stop bit.

10: Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit).

11: Reserved.

Bit 3-2: PARITY

Bits [3:2] of the Control Register are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits [3:2] =

00: Receiver expects Odd Parity (Default Value:).

01: Receiver expects Even Parity.

10: Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit).

11: Reserved.

Bit 1: PS2_EN PS2 Channel Enable

When PS2_EN=1 the PS/2 State machine is enabled allowing the channel to perform automatic reception or transmission depending on the bit value of PS2_T/R. When PS2_EN = 0, the channel's automatic PS/2 state machine is disabled.

Note:

If the PS2_EN bit is cleared prior to the rising edge of the 10th (parity bit) clock edge the receive data is discarded (RDATA_RDY remains low).

If the PS2_EN bit is cleared following the rising edge of the 10th clock signal then the receive data is saved in the Receive Register (RDATA_RDY goes high) assuming no parity error.

In the foregoing two situations, ps2 device can't differentiate host receive data success or fail, and therefore we don't recommend to use this function. It shall set to high before you start any operation of PS2.

Bit 0: PS2_T/R PS/2 Channel Transmit/Receive

This bit is only valid when PS2_EN=1 and sets the PS2 logic for automatic transmission or reception when PS2_T/R equals HIGH or LOW respectively (This bit may be modified, after unsetting PS2_EN).

When set the PS/2 channel is enabled to transmit data. To properly initiate a transmit operation this bit must be set prior to writing to the Transmit Register; writes are blocked to the Transmit Register when this bit is not set.

Upon setting the PS2_T/R bit the channel will drive its CLK line low and then float the DATA line and hold this state until a write occurs to the Transmit Register or until the PS2_T/R bit is cleared. Writing to the Transmit Register initiates the transmit operation. KB controller drives the data line low and, within 100us, floats the clock line (externally pulled high by the pull-up resistor) to signal to the external PS/2 device that data is now available.

The PS2_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Timeout error condition occurs.

Note: If the PS2_T/R bit is set while the channel is actively receiving data prior to the rising edge of the 10th (parity bit) clock edge the receive data is discarded. If this bit is not set prior to the 10th clock signal then the receive data is saved in the Receive Register.

When the PS2_T/R bit is cleared the PS/2 channel is enabled to receive data. Upon clearing this bit, whether RDATA_RDY=0 or no, the channel's CLK and DATA will float waiting for the external PS/2 device to signal the start of a transmission for receiving data. But if RDATA_RDY=1, the hardware won't generate interrupt to indicate finished receive data.

If the PS2_T/R bit is set while RDATA_RDY=1 then the channel's DATA line will float but its CLK line will be held low, holding off the peripheral, until the Receive Register is read.

6.3.1.4 PS/2 Status Registers (PS2STS) (Default Value:: 0000_0000)

Bit 7: Receiver Busy (RX_BUSY)

This bit is indicators for each of the three PS/2 Channels. When a RX_BUSY bit is set the associated channel is actively receiving PS/2 data; when a RX_BUSY bit is clear the channel is idle.

Bit 6: Start Bit Detect (START_DEC)

This bit is set on detecting start bit of receive conditions. Writing high will clear this bit.

Bit 5: Transmitter Timeout (XMIT_TIMEOUT)

This bit is set on one of 3 transmit conditions, and in addition the channel's CLK line is automatically pulled low and held for a period of 300us(Input clock=24MHz) or 600us(Input clock=12MHz) following assertion of the XMIT_TIMEOUT bit during which time the PS2_T/R is also held low:

When the transmitter bit time (time between falling edges) exceeds 300us(Input clock=24MHz) or 600us(Input clock=12MHz).

When the transmitter start bit is not received within 25ms(Input clock=24MHz) or 50ms(Input clock=12MHz) from signaling a transmit start event.

If the time from the 1st (start, falling edge) bit to the 11th (stop, falling edge) bit exceeds 2ms.

Writing high will clear this bit.

6.6.1.3 GPIO 2 Input/Output Register (GPIO2) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.4 GPIO 3 Input/Output Register (GPIO3) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.5 GPIO 4 Input/Output Register (GPIO4) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.6 GPIO 5 Input/Output Register (GPIO5) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.7 GPIO 6 Input/Output Register (GPIO6) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

Bit 4~0: Clock Prescale Number

Input clock=24MHz : Count frequency is 1MHz / 2(Clock Prescale Number +1).

Input clock=12MHz : Count frequency is 1MHz / 4(Clock Prescale Number +1).

6.7.1.2 Watch Dog Status Register (WDTSTS) (Default Value: 0000_0000)

Reset with Power Reset.

Bit 7~1: Reserved

Bit 0: WDT Reset Finished

1: Finished, 0: No Happened.

6.8.1.7 Timer X Register (TX) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer X Reload.

Read: Current Timer X Counter Value

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in first prescale period width.

6.8.1.8 Clock Prescale Number of Timer Y (PREY) (Default Value: 1111_1111)

Bit 7~0: Clock Prescale Number

Write: Prescale Counter Reload.

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in first prescale period width.

Read: Current Prescale Counter Value

6.8.1.9 Timer Y Register (TY) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer Y Reload.

Read: Current Timer X Counter Value

6.9.1.3 PWM 2 Period Register (PWM2P) (Default Value: 0000_0000)

Use the 8-bit register to control width of a full period output.

6.9.1.4 PWM 3 Period Register (PWM3PH, PWM3PL) (Default Value: 0000h)

Use the 16-bit register to control width of a full period output.

6.9.1.5 PWM 4 Period Register (PWM4PH, PWM4PL) (Default Value: 0000h)

Use the 16-bit register to control width of a full period output.

6.9.1.6 PWM 1 High Level Register (PWM1H) (Default Value: 0000_0000)

PWM1H is defined as high signal width for PWM1 output. It is an 8-bit register.

6.9.1.7 PWM 2 High Level Register (PWM2H) (Default Value: 0000_0000)

PWM2H is defined as high signal width for PWM2 output. It is an 8-bit register.

6.9.1.8 PWM 3 High Level Register (PWM3HH, PWM3HL) (Default Value: 0000_0000)

(PWM3HH, PWM3HL) is defined as high signal width for PWM3 output. It is a 16-bit register.

6.9.1.9 PWM 4 High Level Register (PWM4HH, PWM4HL) (Default Value: 0000_0000)

(PWM4HH, PWM4HL) is defined as high signal width for PWM4 output. It is a 16-bit register.

6.10 UART Block

W83L951DG/FG supports one Universal asynchronous serial I/O mode (UART) .Eight serial data transfer formats can be selected, for vary selection of Stop bit, Parity, Parity check, Data length, and the transfer formats used by a transmitter and receiver must be identical.

The transmitter and receiver shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register. The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a byte while the next byte is being received.

Table 6-18.UART Register Define

UART Block(5)									
ExtAddr	Name	7	6	5	4	3	2	1	0
30	UARTCON	TxEn	TS	RxEn	PARE	PARS	STPS	CHAS	Reserved
31	UARTSTS	ParErr	FrameErr	OverErr	Reserved			RxBFull	TxBFull
32	BRGH	Baud Rate Generator High Byte[7:0]							
33	BRGL	Baud Rate Generator Low Byte[7:0]							
34	UARTBUF	UART Transmit / Receive Buffer[7:0]							

Gray: Only with System Reset to initial.

6.10.1 Register Description

6.10.1.1 UART Control Register (UARTCON) (Default Value: 0000_0000)

Bit 7: Transmit enable bit (TE)

0: Transmit disabled. 1: Transmit enable.

Bit 6: Transmit Speed up bit (TS) (Reserved)

0: Disable.

1: Enable.

Bit 5: Receive enable bit (RE)

0: Receive disable. 1: Receive enable.

Bit 4: Parity enable bit (PARE).

0: Parity Bit disable. 1: Parity Bit enable.

Bit 3: Parity selection bit (PARS).

0: Odd parity. 1: Even parity.

Bit 2: Stop bit length selection bit (STPS)

0: 1 stop bit. 1: 2 stop bits.

Bit 1: Character length selection bit (CHAS) .

0: 8 bits 1: 7 bits.

Bit 0: User Define Register

6.10.1.2 UART Status Register (UARTSTS) (Default Value: 0000_0000)

Bit 7: Parity Error Status for Packet at Receive Buffer (PE)

Read: 0 - No error, 1 - Parity error

Bit 6: Framing Error Status for Packet at Receive Buffer (FE)

Read: 0 - No error, 1 - Framing error

Bit 5: Overrun Error Interrupt (OE)

For UART Rx Interrupt, users need to write this bit to clear.

Read:

0 - No error

1 - Overrun error

Write:

0 - No Chang

1 - Clear

Bit 4~2: No use (return 'L' when read)

Bit 1: Receive Buffer Full Status Flag (RBF)

Receive Buffer Full generates the interrupt. Read buffer can clear the flag.

0: Buffer empty

1: Buffer full

Bit 0: Transmit Buffer Full Status Flag (TBF)

Transmit Buffer Empty generates the interrupt. Write buffer can clear the flag. And next byte is allowed to write into the buffer.

0: Buffer empty

1: Buffer full

Write:

0 - No Change

1 - Clear

Bit 6: Start Frame Error Status Flag (Write 'HIGH' to Clear)

When Start Frame Error flag occurs, CIR Interrupt is generated. Write the bit can clear Start Frame Error Flag.

Read:

0 - No error

1 – Start Frame Error

Write:

0 - No Change

1 - Clear

Bit 5: Repeat Status Flag (Write 'HIGH' to Clear)

When Repeat Flag occurs, CIR Interrupt is generated. Write the bit can clear Repeat Flag.

Read:

0 - No happened

1 – Repeat Packet Received.

Write:

0 - No Change

1 - Clear

Bit 4: Finish Status Flag (Write 'HIGH' to Clear)

When Finish Flag occurs, CIR Interrupt is generated. Write the bit can clear Finish Flag.

Read:

0 - No happened

1 – Packet Received is finish.

Write:

0 - No Chang

1 - Clear

Bit 3: Data Frame Error Interrupt Mask Enable

0 – Enable.

1 – Disable.

Bit 2: Start Frame Error Interrupt Mask Enable

0 – Enable.

1 – Disable.

6.17 Flash Memory

The W83L951DG/FG has a 64KByte, 3.3-volt only CMOS flash memory. The byte-wide (× 8) data appears on DQ7–DQ0. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is not required. The unique cell architecture of the Flash results in fast program/erase operations with extremely low current consumption (compared to other comparable 3.3-volt flash memory products). The device can also be programmed and erased by using standard EPROM programmers.

6.17.1 External Programming Mode

The context of flash in Winbond Keyboard controller is empty by default. At the first use, you must program the flash by external writer device. For programming the flash by external device, the Winbond Keyboard controller must enter the flash-programming mode by TEST# Pin is connected to GND. RESET# Pin is connected to GND. FA [7:0] and FD [7:0] port is combined to GP07 to GP00. FA [7:0] is latched by the ALE (GP34).

In External Programming Mode, W83L951DG/FG protects Internal Flash data, so W83L951DG/FG will close “Read Command”. Under this condition, users must run “Erase Command” to use “Read Command”.

6.17.2 Internal Programming Mode

In W83L951DG/FG, in addition to access internal flash by outside, it provides to access SFR by Microprocessor. When Enable Memory Bit of Memory Mapping Control Register is high, and PC is F800~FFFFh, Microprocessor can access Internal Flash by SFR.

Table 6-26.Internal Programming Flash Register Define

INTERNAL PROGRAMMING FLASH									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F9	FCON	CEB	OEB	WEB	Reserved				EXCHANG_GP
FA	FADDH	A[15:8]							
FB	FADDL	A[7:0]							
FC	FDATA	DQ[7:0]							

6.17.2.1 Flash Control Register (FCON) (Default Value: 0000_0000)

6.17.2.2 Bit7: Flash Chip Select Enable (CEB)

Like CE# Pin. Refer to next section for further details.

Bit6: Flash Output Enable (OEB)

Like OE# Pin. Refer to next section for further details.

Bit5: Flash Write Enable (WEB)

Like WE# Pin. Refer to next section for further details.

Bit4~Bit1: Reserved

Bit0: Exchange GPIOA/B/C to GPIO1/0/3 Function (Reserved)

6.17.7 Embedded Algorithm

6.17.7.1 Embedded Programming Algorithm

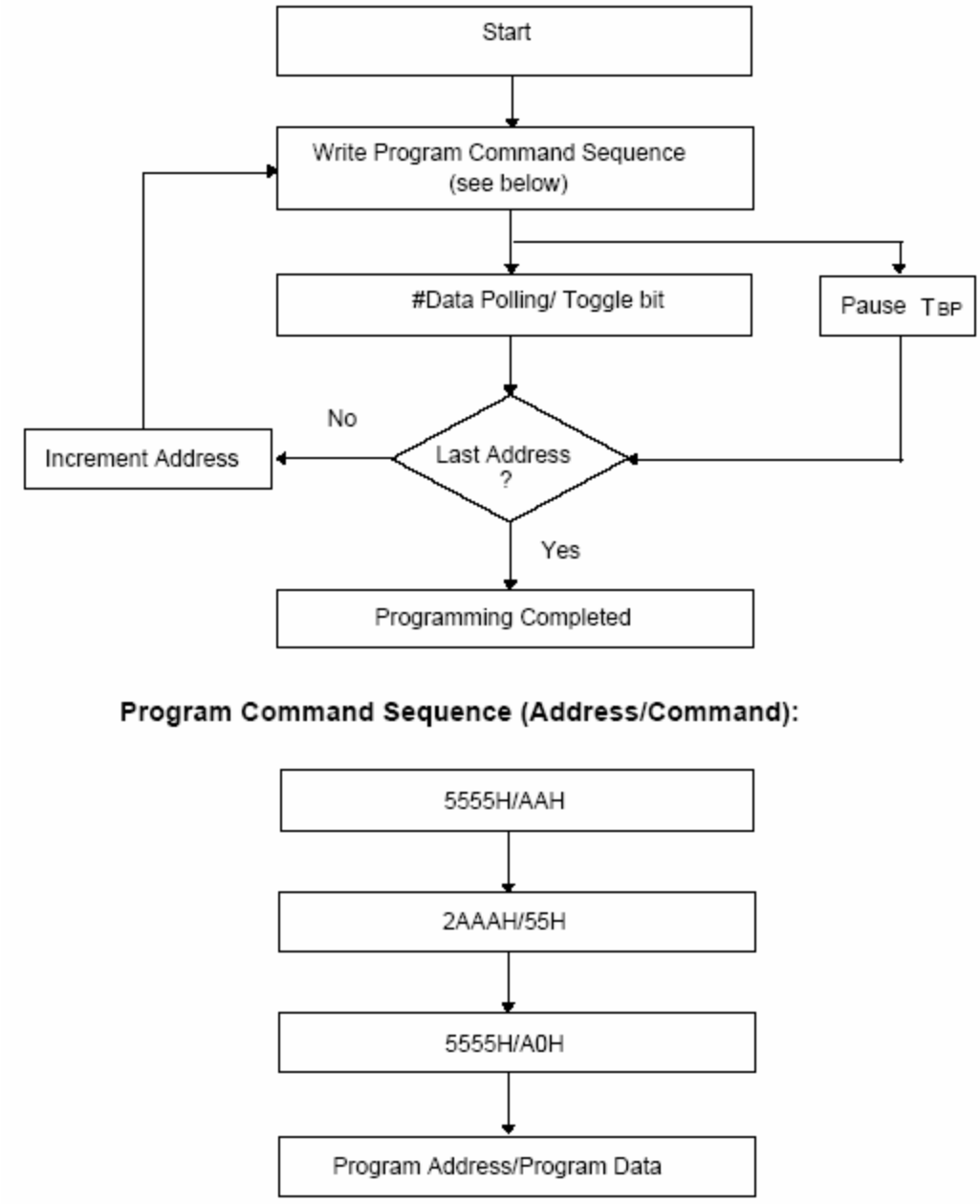

Figure 6-3.Embedded Programming Algorithm State Diagram

6.17.8 Timing Parameters

Table 6-29.Read Cycle Timing Parameters Table

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	TRC	90	-	ns
Chip Enable Access Time	TCE	-	90	ns
Address Access Time	TAA	-	90	ns
Output Enable Access Time	TOE	-	45	ns
#CE Low to Active Output	TCLZ	0	-	ns
#OE Low to Active Output	TOLZ	0	-	ns
#CE High to High-Z Output	TCHZ	-	25	ns
#OE High to High-Z Output	TOHZ	-	25	ns
Output Hold from Address Change	TOH	0	-	ns

Note: (VDD = 3.3V ±0.3V, VSS = 0V, TA = 0 to 70° C or -40 to 85° C)

Table 6-30.Write Cycle Timing Parameters Table

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	40	-	-	nS
#WE and #CE Setup Time	TCS	0	-	-	nS
#WE and #CE Hold Time	TCH	0	-	-	nS
#OE High Setup Time	TOES	0	-	-	nS
#OE High Hold Time	TOEH	0	-	-	nS
#CE Pulse Width	TCP	100	-	-	nS
#WE Pulse Width	TWP	100	-	-	nS
#WE High Width	TWPH	100	-	-	nS
Data Setup Time	TDS	40	-	-	nS
Data Hold Time	TDH	10	-	-	nS
Byte Programming Time	TBP	-	35	50	μS
Chip Erase Cycle Time	TEC	-	50	100	mS
Sector/Page Erase Cycle Time	TEP	-	12.5	25	mS

11. DEMO CIRCUITS