Renesas Electronics America Inc - R8A77450HA01BG#UA Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	-
Speed	1GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77450ha01bg-ua

1. Overview

1.1 Introduction

The RZ/G1E is that features the basic functions for Rich Graphics Applications.

The RZ/G1E includes:

- Two 1.0-GHz ARM Cortex®-A7 MPCore® cores,
- Memory controller for DDR3-SDRAM (DDR3-1333) with 32 bits × 1 channel,
- Three-dimensional graphics engines,
- Video processing unit,
- 2 channels Display Output,
- 2 channels Video Input,
- Sound processing unit,
- SD card host interface,
- USB2.0 interfaces, and
- CAN interface.

Also, a full implementation of the extremely expandable and Internal AXI bus has been adopted for the RZ/G1E.

This bus structure is optimized for maximum system performance, leading to the realization of high-performance and cost-effective premium in-vehicle infotainment systems.

Notes: 1. ARM is a registered trademark and Cortex is a trademark of ARM Limited. All other brands or product names are the property of their respective holders.

1.3 List of Specifications

1.3.1 ARM Core

Item	Description
System CPU Cortex-A7	• ARM Cortex-A7 Dual MPCore 1.0 GHz • L1 I/D cache 32/32 KBytes, L2 cache 512 KBytes • NEON™/VFPv4 supported • Security extension supported
ARM debugger (CoreSight™)	• CoreSight system compliant • JTAG/SWD I/F supported • CoreSight ETR 16 KBytes for program flow trace • CoreSight ETR 4 KBytes for system trace

Item	Description	
Serial sound interface unit (SSIU)	Overall specification	• Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats — Supports TDM format (six modules of ten modules can be used for this function) • Max. 4 independent stereo sound sources in a TDM format can be distributed to each course. Moreover Max. 4 independent stereo sound source can be combined output in TDM format.
	Serial sound interface (SSI)	• Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-/32-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
Audio clock generator (ADG)	• Selection or division of audio clock signals	

Item	Description
Clock-synchronized serial interface with FIFO (MSIOF)	• 3 channels • Max. speed: 26 Mbps • Internal 64-Byte transmit FIFOs/internal 256-Byte receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
Quad-SPI (QSPI)	• Single/Dual/Quad-SPI: serial slave transfer enabled • Supports master mode • SPCLK clock rate: 1…4080 in master mode; Max. 78 MHz
High-speed serial communication interface with FIFO (HSCIF)	• 3 channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS and HCTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM timer (PWM)	• 7 channels • High-level width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1024 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
Boot Function (BOOT)	• System startup with selectable boot mode at power-on reset • Program downloaded to internal memory (LRAM) • Autorun function for the downloaded program

2. Area Map

See section 2, Area Map in the RZ/G Series User's Manual: Hardware.

LBSC, SCIFB, PWM, TPU, SCIFA, MSIOF, IIC, HSCIF, RCAN, QSPI and GPIO (No.177 to 196): Up to 8-Function Multiplexed and Mode Pin assigned (No.177, 180, 182, 186, 188, 191 and 192)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.
When MD[3:1]=000, the LBSC will execute area 0 booting; MD[3:1]≠000, the QSPI will execute QSPI booting.

Function	1	2	3	4	5	6	7	GPIO	
MD[3:1]	=000							≠000	
No.									During POR
Pin No.									V(power)/|IOH|
Mode Pin									Pull-up
177	LBSC	SCIFB0	-	-	-	-	-		I(Mode Pin)
H4	A4	SCIFB0_TXD	-	-	-	-	-	GP0_20	3.3V(VCCQ)/8mA
MD1	O(L)	O	-	-	-	-	-	IO(I)	Off
178	LBSC	SCIFB0	PWM4	TPU	-	-	-		I(GPIO)
F2	A5	SCIFB0_RXD	PWM4_B	TPUTO3_C	-	-	-	GP0_21	3.3V(VCCQ)/8mA
	O(L)	I	O	O	-	-	-	IO(I)	On
179	LBSC	SCIFB0	SCIFA4	TPU	-	-	-		I(GPIO)
G5	A6	SCIFB0_CTS#	SCIFA4_RXD_B	TPUTO2_C	-	-	-	GP0_22	3.3V(VCCQ)/8mA
	O(L)	I	I	O	-	-	-	IO(I)	On
180	LBSC	SCIFB0	SCIFA4	-	-	-	-		I(Mode Pin)
F1	A7	SCIFB0_RTS#	SCIFA4_TXD_B	-	-	-	-	GP0_23	3.3V(VCCQ)/8mA
MD4	O(L)	O	O	-	-	-	-	IO(I)	Off
181	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(GPIO)
J5	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	GP0_24	3.3V(VCCQ)/8mA
	O(L)	I	I	-	-	-	-	IO(I)	On
182	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(Mode Pin)
G2	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	GP0_25	3.3V(VCCQ)/8mA
MD5	O(L)	O	O	-	-	-	-	IO(I)	Off
183	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
J4	A10	MSIOF1_SCK	IIC0_SCL_B	-	-	-	-	GP0_26	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
184	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
H3	A11	MSIOF1_SYNC	IIC0_SDA_B	-	-	-	-	GP0_27	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
185	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(GPIO)
G3	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	GP0_28	3.3V(VCCQ)/8mA
	O(L)	O	I	-	-	-	-	IO(I)	On
186	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(Mode Pin)
G1	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	GP0_29	3.3V(VCCQ)/8mA
MD6	O(L)	O	O	-	-	-	-	IO(I)	Off
187	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(GPIO)
K5	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1#	-	-	-	GP0_30	3.3V(VCCQ)/8mA
	O(L)	I	I	I	-	-	-	IO(I)	On
188	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(Mode Pin)
H1	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	GP0_31	3.3V(VCCQ)/8mA
MD7	O(L)	O	O	O	-	-	-	IO(I)	Off
189	LBSC	MSIOF2	HSCIF0	Reserved	Reserved	RCAN	TPU		I(GPIO)
J2	A16	MSIOF2_SCK	HSCIF0_HSCK_B	-	-	CAN_CLK_C	TPUTO2_B	GP1_0	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	I	O	IO(I)	On
190	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(GPIO)
K4	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	-	-	-	GP1_1	3.3V(VCCQ)/8mA
	O(L)	IO	I	I	-	-	-	IO(I)	On
191	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(Mode Pin)
H2	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	-	-	-	GP1_2	3.3V(VCCQ)/8mA
MDT0	O(L)	O	O	O	-	-	-	IO(I)	Off
192	LBSC	MSIOF2	PWM4	TPU	Reserved	-	-		I(Mode Pin)
K3	A19	MSIOF2_SS2	PWM4	TPUTO2	-	-	-	GP1_3	3.3V(VCCQ)/8mA
MD18	O(L)	O	O	O	-	-	-	IO(I)	Off
193	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K2	A20	SPCLK	-	-	-	-	-	GP1_4	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
194	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K1	A21	MOSI/IO0	-	-	-	-	-	GP1_5	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
195	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
L3	A22	MISO/IO1	-	ATADIR1#	-	-	-	GP1_6	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On
196	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
J3	A23	IO2	-	ATAWR1#	-	-	-	GP1_7	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On

VIN, I2C, SCIFA, EthernetAVB, ADG, EtherMAC, MSIOF, RCAN, SCIF, IIC, SSI, HSCIF and GPIO (No.257 to 277): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	GPIO	
No.									During POR
Pin No.									V(power)/|IOH|
									Pull-up
257	VIN0	I2C3	SCIFA5	Reserved	EthernetAVB	-	-		I(GPIO)
AA1	VI0_CLKENB	I2C3_SCL	SCIFA5_RXD_C	-	AVB_RXD7	-	-	GP3_9	3.3V(VCCQ)/4mA
	I	IO	I	-	I	-	-	IO(I)	On
258	VIN0	I2C3	SCIFA5	Reserved	EthernetAVB	-	-		I(GPIO)
W2	VI0_FIELD	I2C3_SDA	SCIFA5_TXD_C	-	AVB_RX_ER	-	-	GP3_10	3.3V(VCCQ)/4mA
	I	IO	O	-	I	-	-	IO(I)	On
259	VIN0	SCIF0	I2C0	Reserved	EthernetAVB	-	-		I(GPIO)
Y1	VI0_HSYNC#	SCIF0_RXD_B	I2C0_SCL_C	-	AVB_COL	-	-	GP3_11	3.3V(VCCQ)/4mA
	I	I	IO	-	I	-	-	IO(I)	On
260	VIN0	SCIF0	I2C0	ADG	EthernetAVB	-	-		I(GPIO)
W1	VI0_VSYNC#	SCIF0_TXD_B	I2C0_SDA_C	AUDIO_CLKOUT_B	AVB_TX_EN	-	-	GP3_12	3.3V(VCCQ)/8mA
	I	O	IO	O	O	-	-	IO(I)	On
261	EtherMAC	VIN0	MSIOF2	I2C5	EthernetAVB	Reserved	Reserved		I(GPIO)
T5	ETH_MDIO	VI0_G0	MSIOF2_RXD_B	I2C5_SCL_D	AVB_TX_CLK	-	-	GP3_13	3.3V(VCCQ)/4mA
	IO	I	I	IO	I	-	-	IO(I)	On
262	EtherMAC	VIN0	MSIOF2	I2C5	EthernetAVB	Reserved	Reserved		I(GPIO)
V4	ETH_CRS_DV	VI0_G1	MSIOF2_TXD_B	I2C5_SDA_D	AVB_TXD0	-	-	GP3_14	3.3V(VCCQ)/8mA
	I	I	O	IO	O	-	-	IO(I)	On
263	EtherMAC	VIN0	MSIOF2	RCAN0	EthernetAVB	Reserved	Reserved		I(GPIO)
U5	ETH_RX_ER	VI0_G2	MSIOF2_SCK_B	CAN0_RX_B	AVB_TXD1	-	-	GP3_15	3.3V(VCCQ)/8mA
	I	I	IO	I	O	-	-	IO(I)	On
264	EtherMAC	VIN0	MSIOF2	RCAN0	EthernetAVB	Reserved	Reserved		I(GPIO)
V3	ETH_RXD0	VI0_G3	MSIOF2_SYNC_B	CAN0_TX_B	AVB_TXD2	-	-	GP3_16	3.3V(VCCQ)/8mA
	I	I	IO	O	O	-	-	IO(I)	On
265	EtherMAC	VIN0	MSIOF2	SCIF4	EthernetAVB	Reserved	-		I(GPIO)
U4	ETH_RXD1	VI0_G4	MSIOF2_SS1_B	SCIF4_RXD_D	AVB_TXD3	-	-	GP3_17	3.3V(VCCQ)/8mA
	I	I	O	I	O	-	-	IO(I)	On
266	EtherMAC	VIN0	MSIOF2	SCIF4	EthernetAVB	Reserved	-		I(GPIO)
V5	ETH_LINK	VI0_G5	MSIOF2_SS2_B	SCIF4_TXD_D	AVB_TXD4	-	-	GP3_18	3.3V(VCCQ)/8mA
	I	I	O	O	O	-	-	IO(I)	On
267	EtherMAC	VIN0	SCIF2	EthernetAVB	SSI	-	-		I(GPIO)
V1	ETH_REF_CLK	VI0_G6	SCIF2_SCK_C	AVB_TXD5	SSI_SCK5_B	-	-	GP3_19	3.3V(VCCQ)/8mA
	I	I	IO	O	IO	-	-	IO(I)	On
268	EtherMAC	VIN0	SCIF2	IIC0 (I2C6)	EthernetAVB	SSI	-		I(GPIO)
V2	ETH_TXD1	VI0_G7	SCIF2_RXD_C	IIC0_SCL_D	AVB_TXD6	SSI_WS5_B	-	GP3_20	3.3V(VCCQ)/8mA
	O	I	I	IO	O	IO	-	IO(I)	On
269	EtherMAC	VIN0	SCIF2	IIC0 (I2C6)	EthernetAVB	SSI	-		I(GPIO)
U3	ETH_TX_EN	VI0_R0	SCIF2_TXD_C	IIC0_SDA_D	AVB_TXD7	SSI_SDATA5_B	-	GP3_21	3.3V(VCCQ)/8mA
	O	I	O	IO	O	IO	-	IO(I)	On
270	EtherMAC	VIN0	SCIF3	EthernetAVB	SSI	-	-		I(GPIO)
W4	ETH_MAGIC	VI0_R1	SCIF3_SCK_B	AVB_TX_ER	SSI_SCK6_B	-	-	GP3_22	3.3V(VCCQ)/8mA
	O	I	IO	O	IO	-	-	IO(I)	On
271	EtherMAC	VIN0	SCIF3	I2C4	EthernetAVB	SSI	-		I(GPIO)
U2	ETH_TXD0	VI0_R2	SCIF3_RXD_B	I2C4_SCL_E	AVB_GTX_CLK	SSI_WS6_B	-	GP3_23	3.3V(VCCQ)/8mA
	O	I	I	IO	O	IO	-	IO(I)	On
272	EtherMAC	VIN0	SCIF3	I2C4	EthernetAVB	SSI	-		I(GPIO)
W5	ETH_MDC	VI0_R3	SCIF3_TXD_B	I2C4_SDA_E	AVB_MDC	SSI_SDATA6_B	-	GP3_24	3.3V(VCCQ)/8mA
	O	I	O	IO	O	IO	-	IO(I)	On
273	HSCIF0	VIN0	I2C1	ADG	EthernetAVB	SSI	-		I(GPIO)
U1	HSCIF0_HRX	VI0_R4	I2C1_SCL_C	AUDIO_CLKA_B	AVB_MDIO	SSI_SCK78_B	-	GP3_25	3.3V(VCCQ)/8mA
	I	I	IO	I	IO	IO	-	IO(I)	On
274	HSCIF0	VIN0	I2C1	ADG	EthernetAVB	SSI	-		I(GPIO)
T4	HSCIF0_HTX	VI0_R5	I2C1_SDA_C	AUDIO_CLKB_B	AVB_LINK	SSI_WS78_B	-	GP3_26	3.3V(VCCQ)/8mA
	O	I	IO	I	I	IO	-	IO(I)	On
275	HSCIF0	VIN0	SCIF0	I2C0	EthernetAVB	SSI	-		I(GPIO)
T3	HSCIF0_HCTS#	VI0_R6	SCIF0_RXD_D	I2C0_SCL_E	AVB_MAGIC	SSI_SDATA7_B	-	GP3_27	3.3V(VCCQ)/8mA
	IO	I	I	IO	O	IO	-	IO(I)	On
276	HSCIF0	VIN0	SCIF0	I2C0	EthernetAVB	SSI	-		I(GPIO)
T2	HSCIF0_HRTS#	VI0_R7	SCIF0_TXD_D	I2C0_SDA_E	AVB_PHY_INT	SSI_SDATA8_B	-	GP3_28	3.3V(VCCQ)/8mA
	IO	I	O	IO	I	IO	-	IO(I)	On
277	HSCIF0	SCIF	EthernetAVB	ADG	-	-	-		I(GPIO)
T1	HSCIF0_HSCK	SCIF_CLK_B	AVB_CRS	AUDIO_CLKC_B	-	-	-	GP3_29	3.3V(VCCQ)/8mA
	IO	I	I	I	-	-	-	IO(I)	On

SSI, SCIF, PWM, INTC, LBSC, EtherMAC, IIC, VIN, RCAN, HSCIF, SCIFA, I2C and GPIO (No.319 to 334): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset except for No.322 to 324. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	GPIO	
No.										During POR
Pin No.										V(power)/|IOH|
										Pull-up
319	SSI	Reserved	Reserved	Reserved	-	-	-	-		I(GIPIO)
AD22	SSI_SCK4	-	-	-	-	-	-	-	GP5_7	3.3V(VCCQ)/16mA
	IO	-	-	-	-	-	-	-	IO(I)	-
320	SSI	Reserved	Reserved	Reserved	-	-	-	-		I(GIPIO)
AB21	SSI_WS4	-	-	-	-	-	-	-	GP5_8	3.3V(VCCQ)/16mA
	IO	-	-	-	-	-	-	-	IO(I)	-
321	SSI	Reserved	Reserved	Reserved	-	-	-	-		I(GIPIO)
Y21	SSI_SDATA4	-	-	-	-	-	-	-	GP5_9	3.3V(VCCQ)/16mA
	IO	-	-	-	-	-	-	-	IO(I)	-
322	Reserved	-	-	-	-	-	-	-	-	IO(MLB)
AD24	-	-	-	-	-	-	-	-	-	3.3V(VCCQ)/16mA
	-	-	-	-	-	-	-	-	-	-
323	-	-	-	-	-	-	-	-	-	P
W20	VSS_MLBPLL	-	-	-	-	-	-	-	-	GND(VDD_MLBPLL)/-
	P	-	-	-	-	-	-	-	-	-
324	-	-	-	-	-	-	-	-	-	P
V21	VDD_MLBPLL	-	-	-	-	-	-	-	-	1.8V(VDD_MLBPLL)/-
	P	-	-	-	-	-	-	-	-	-
325	SSI	SCIF1	PWM1	INTC	Reserved	LBSC	EtherMAC	-		I(GPIO)
AC6	SSI_SDATA8	SCIF1_SCK_B	PWM1_B	IRQ9	-	DACK2	ETH_MDIO_B	-	GP5_10	3.3V(VCCQ)/8mA
	IO	IO	O	I	-	O	IO	-	IO(I)	On
326	SSI	SCIF1	IIC0(I2C6)	VIN1	RCAN0	Reserved	EtherMAC	-		I(GPIO)
AE6	SSI_SCK1	SCIF1_RXD_B	IIC0_SCL_C	VI1_CLK	CAN0_RX_D	-	ETH_CRS_DV_B	-	GP5_11	3.3V(VCCQ)/8mA
	IO	I	IO	I	I	-	I	-	IO	On
327	SSI	SCIF1	IIC0(I2C6)	VIN1	RCAN0	Reserved	EtherMAC	-		I(GPIO)
AB5	SSI_WS1	SCIF1_TXD_B	IIC0_SDA_C	VI1_DATA0	CAN0_TX_D	-	ETH_RX_ER_B	-	GP5_12	3.3V(VCCQ)/8mA
	IO	O	IO	I	O	-	I	-	IO	On
328	SSI	HSCIF1	VIN1	Reserved	LBSC	EtherMAC	-	-		I(GPIO)
AC5	SSI_SDATA1	HSCIF1_HRX_B	VI1_DATA1	-	ATAWR0#	ETH_RXD0_B	-	-	GP5_13	3.3V(VCCQ)/8mA
	IO	I	I	-	O	I	-	-	IO	On
329	SSI	HSCIF1	VIN1	Reserved	LBSC	EtherMAC	-	-		I(GPIO)
AE4	SSI_SCK2	HSCIF1_HTX_B	VI1_DATA2	-	ATAG0#	ETH_RXD1_B	-	-	GP5_14	3.3V(VCCQ)/8mA
	IO	O	I	-	O	I	-	-	IO	On
330	SSI	HSCIF1	SCIFA0	VIN1	Reserved	LBSC	EtherMAC	-		I(GPIO)
AD4	SSI_WS2	HSCIF1_HCTS#_B	SCIFA0_RXD_D	VI1_DATA3	-	ATACS00#	ETH_LINK_B	-	GP5_15	3.3V(VCCQ)/8mA
	IO	IO	I	I	-	O	I	-	IO	On
331	SSI	HSCIF1	SCIFA0	VIN1	Reserved	LBSC	EtherMAC	-		I(GPIO)
AC4	SSI_SDATA2	HSCIF1_HRTS#_B	SCIFA0_TXD_D	VI1_DATA4	-	ATACS10#	ETH_REF_CLK_B	-	GP5_16	3.3V(VCCQ)/8mA
	IO	IO	O	I	-	O	I	-	IO	On
332	SSI	SCIF2	PWM2	VIN1	Reserved	LBSC	EtherMAC	-		I(GPIO)
AE3	SSI_SCK9	SCIF2_SCK_B	PWM2_B	VI1_DATA5	-	EX_WAIT1	ETH_TXD1_B	-	GP5_17	3.3V(VCCQ)/8mA
	IO	IO	O	I	-	I	O	-	IO	On
333	SSI	SCIF2	I2C3	VIN1	LBSC	EtherMAC	-	-		I(GPIO)
AD3	SSI_WS9	SCIF2_RXD_B	I2C3_SCL_E	VI1_DATA6	ATARD0#	ETH_TX_EN_B	-	-	GP5_18	3.3V(VCCQ)/8mA
	IO	I	IO	I	O	O	-	-	IO	On
334	SSI	SCIF2	I2C3	VIN1	LBSC	EtherMAC	-	-		I(GPIO)
AD2	SSI_SDATA9	SCIF2_TXD_B	I2C3_SDA_E	VI1_DATA7	ATADIR0#	ETH_MAGIC_B	-	-	GP5_19	3.3V(VCCQ)/8mA
	IO	O	IO	I	O	O	-	-	IO	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
49	C21	M0DM0	O	Z	M0DM0	Z	-
50	F16	VDDQ_M0DPLL0	-	P	-	P	-
51	F15	VSSQ_M0DPLL0	-	P	-	P	-
52	C14	M0VREFDQ0	-	P	-	P	-
53	B17	M0DQ8	IO	Z	M0DQ8	Z	-
54	D17	M0DQ9	IO	Z	M0DQ9	Z	-
55	B19	M0DQ10	IO	Z	M0DQ10	Z	-
56	B20	M0DQ11	IO	Z	M0DQ11	Z	-
57	D19	M0DQ12	IO	Z	M0DQ12	Z	-
58	E19	M0DQ13	IO	Z	M0DQ13	Z	-
59	B18	M0DQ14	IO	Z	M0DQ14	Z	-
60	E18	M0DQ15	IO	Z	M0DQ15	Z	-
61	A18	M0DQS1	IO	Z(*1)	M0DQS1	Z(*1)	-
62	A17	M0DQS1#	IO	Z(*1)	M0DQS1#	Z(*1)	-
63	D18	M0DM1	O	Z	M0DM1	Z	-
64	E16	VDDQ_M0DPLL1	-	P	-	P	-
65	E15	VSSQ_M0DPLL1	-	P	-	P	-
66	G24	M0DQ16	IO	Z	M0DQ16	Z	-
67	E22	M0DQ17	IO	Z	M0DQ17	Z	-
68	E24	M0DQ18	IO	Z	M0DQ18	Z	-
69	C25	M0DQ19	IO	Z	M0DQ19	Z	-
70	F24	M0DQ20	IO	Z	M0DQ20	Z	-
71	D24	M0DQ21	IO	Z	M0DQ21	Z	-
72	B25	M0DQ22	IO	Z	M0DQ22	Z	-
73	C24	M0DQ23	IO	Z	M0DQ23	Z	-
74	F25	M0DQS2	IO	Z(*1)	M0DQS2	Z(*1)	-
75	E25	M0DQS2#	IO	Z(*1)	M0DQS2#	Z(*1)	-
76	F22	M0DM2	O	Z	M0DM2	Z	-
77	J21	VDDQ_M0DPLL2	-	P	-	P	-
78	H21	VSSQ_M0DPLL2	-	P	-	P	-
79	G23	M0VREFDQ1	-	P	-	P	-
80	J23	M0DQ24	IO	Z	M0DQ24	Z	-
81	K22	M0DQ25	IO	Z	M0DQ25	Z	-
82	H22	M0DQ26	IO	Z	M0DQ26	Z	-
83	L22	M0DQ27	IO	Z	M0DQ27	Z	-
84	J24	M0DQ28	IO	Z	M0DQ28	Z	-
85	L24	M0DQ29	IO	Z	M0DQ29	Z	-
86	K24	M0DQ30	IO	Z	M0DQ30	Z	-
87	L25	M0DQ31	IO	Z	M0DQ31	Z	-
88	H25	M0DQS3	IO	Z(*1)	M0DQS3	Z(*1)	-
89	J25	M0DQS3#	IO	Z(*1)	M0DQS3#	Z(*1)	-
90	J22	M0DM3	O	Z	M0DM3	Z	-
91	J20	VDDQ_M0DPLL3	-	P	-	P	-
92	H20	VSSQ_M0DPLL3	-	P	-	P	-
93	C7	VDDQ_M0BKUP	-	P	-	P	-
94	V25	EXTAL	I	I	EXTAL	I	-
95	V24	XTAL	O	O	XTAL	O	-
96	E8	VDD_CPGPLL0	-	P	-	P	-
97	E9	VSS_CPGPLL0	-	P	-	P	-
98	K15/L15	VDD_CPGPLL1	-	P	-	P	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
199	B1	CLKOUT	O	O	CLKOUT	O	-
200	E2	CS0#	O	I	CS0#/GP1_10(*4)	H/I	On
201	M5	CS1#/A26	O	I	[CS1#/A26]/GP1_11	[H/L] (*5)/I	On
202	E1	EX_CS0#	O	I	GP1_12	I	On
203	E3	EX_CS1#	O	I	GP1_13	I	On
204	D1	EX_CS2#	O	I	GP1_14	I	On
205	D2	EX_CS3#	O	I	GP1_15	I	On
206	C1	EX_CS4#	O	I	GP1_16	I	On
207	B2	EX_CS5#	O	I	GP1_17	I	On
208	M4	BS#	O	I(MD8)	BS#/GP1_18(*4)	H/I	Off
209	M3	RD#	O	I(MD14)	RD#GP1_19(*4)	H/I	Off
210	M1	RD/WR#	O	I(MD9)	GP1_20	I	Off
211	L1	WE0#	O	I(MD19)	WE0#/ GP1_21(*4)	H/I	Off
212	L4	WE1#	O	I(MD20)	WE1#/ GP1_22(*4)	H/I	Off
213	C2	EX_WAIT0	I	I	EX_WAIT0/ GP1_23(*4)	I/I	On
214	L5	DREQ0#	I	I	GP1_24	I	On
215	M2	DACK0	O	I(MD21)	GP1_25	I	Off
216	AA18	DU0_DR0	O	I	GP2_0	I	On
217	AB18	DU0_DR1	O	I	GP2_1	I	On
218	AE19	DU0_DR2	O	I	GP2_2	I	On
219	AC18	DU0_DR3	O	I	GP2_3	I	On
220	AD19	DU0_DR4	O	I	GP2_4	I	On
221	AD17	DU0_DR5	O	I	GP2_5	I	On
222	AC17	DU0_DR6	O	I	GP2_6	I	On
223	AC19	DU0_DR7	O	I	GP2_7	I	On
224	AA17	DU0_DG0	O	I	GP2_8	I	On
225	AB16	DU0_DG1	O	I	GP2_9	I	On
226	AD18	DU0_DG2	O	I	GP2_10	I	On
227	AD16	DU0_DG3	O	I	GP2_11	I	On
228	AB17	DU0_DG4	O	I	GP2_12	I	On
229	AA16	DU0_DG5	O	I	GP2_13	I	On
230	AE16	DU0_DG6	O	I	GP2_14	I	On
231	AC16	DU0_DG7	O	I	GP2_15	I	On
232	AC14	DU0_DB0	O	I	GP2_16	I	On
233	AE17	DU0_DB1	O	I	GP2_17	I	On
234	AA15	DU0_DB2	O	I	GP2_18	I	On
235	AB15	DU0_DB3	O	I	GP2_19	I	On
236	AD14	DU0_DB4	O	I	GP2_20	I	On
237	AD15	DU0_DB5	O	I	GP2_21	I	On
238	AA14	DU0_DB6	O	I	GP2_22	I	On
239	AC15	DU0_DB7	O	I	GP2_23	I	On
240	AE15	DU0_DOTCLKIN	I	I	GP2_24	I	On
241	AE14	DU0_DOTCLKOUT0	O	I	GP2_25	I	On
242	AE13	DU0_DOTCLKOUT1	O	I	GP2_26	I	On
243	AD13	DU0_EXHSYNC/DU0_HSYNC	IO	I(MD11)	GP2_27	I	Off
244	AB14	DU0_EXVSYNC/DU0_VSYNC	IO	I(MD12)	GP2_28	I	Off
245	AC13	DU0_EXODDF/DU0_ODDF/DISP/CDE	IO	I	GP2_29	I	On
246	AE18	DU0_DISP	O	I(MD10)	GP2_30	I	Off
247	AB13	DU0_CDE	O	I(MD13)	GP2_31	I	Off
248	AB1	VI0_CLK	I	I	GP3_0	I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
299	AA22	SCIF3_SCK	IO	I	GP4_19	I	On
300	AC22	SCIF3_RXD	I	I	GP4_20	I	On
301	AC21	SCIF3_TXD	O	I	GP4_21	I	On
302	AD21	I2C2_SCL	IO	I	GP4_22	I	On
303	AC20	I2C2_SDA	IO	I	GP4_23	I	On
304	AE22	SSI_SCK5	IO	I	GP4_24	I	On
305	AB20	SSI_WS5	IO	I	GP4_25	I	On
306	AA20	SSI_SDATA5	IO	I	GP4_26	I	On
307	AE20	SSI_SCK6	IO	I	GP4_27	I	On
308	AD20	SSI_WS6	IO	I	GP4_28	I	On
309	AE21	SSI_SDATA6	IO	I	GP4_29	I	On
310	AB19	SSI_SCK78	IO	I	GP4_30	I	On
311	AA19	SSI_WS78	IO	I	GP4_31	I	On
312	AB7	SSI_SDATA7	IO	I	GP5_0	I	On
313	AE5	SSI_SCK0129	IO	I	GP5_1	I	On
314	AA7	SSI_WS0129	IO	I	GP5_2	I	On
315	AA6	SSI_SDATA0	IO	I	GP5_3	I	On
316	AD6	SSI_SCK34	IO	I	GP5_4	I	On
317	AB6	SSI_WS34	IO	I	GP5_5	I	On
318	AD5	SSI_SDATA3	IO	I	GP5_6	I	On
319	AD22	SSI_SCK4	IO	I	GP5_7	I	-
320	AB21	SSI_WS4	IO	I	GP5_8	I	-
321	Y21	SSI_SDATA4	IO	I	GP5_9	I	-
322	AD24	MLB_REF	IO	IO	Reserved	IO	-
323	W20	VSS_MLBPLL	-	P	-	P	-
324	V21	VDD_MLBPLL	-	P	-	P	-
325	AC6	SSI_SDATA8	IO	I	GP5_10	I	On
326	AE6	SSI_SCK1	IO	I	GP5_11	I	On
327	AB5	SSI_WS1	IO	I	GP5_12	I	On
328	AC5	SSI_SDATA1	IO	I	GP5_13	I	On
329	AE4	SSI_SCK2	IO	I	GP5_14	I	On
330	AD4	SSI_WS2	IO	I	GP5_15	I	On
331	AC4	SSI_SDATA2	IO	I	GP5_16	I	On
332	AE3	SSI_SCK9	IO	I	GP5_17	I	On
333	AD3	SSI_WS9	IO	I	GP5_18	I	On
334	AD2	SSI_SDATA9	IO	I	GP5_19	I	On
335	AD1	AUDIO_CLKA	I	I	GP5_20	I	On
336	AE2	AUDIO_CLKB	I	I	GP5_21	I	On
337	AC1	AUDIO_CLKC	I	I	GP5_22	I	On
338	AC2	AUDIO_CLKOUT	O	I	GP5_23	I	On
339	W21	IIC1_SCL	IO	Z	IIC1_SCL	Z	-
340	V22	IIC1_SDA	IO	Z	IIC1_SDA	Z	-

Notes: 1. No.47, 48, 61, 62, 74, 75, 88 and 89 (M0DQSx and M0DQSx#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx pin and high-level for the M0DQSx# pin respectively.

2. No.137 to 142 and 146 to 151 Default pin function and pin state:
Depends on MD[21:20], MD[12:10], and MDT[1:0] settings.
"I" is in function mode (GPIO); "Z" is in debug mode.

3. No.138 to 142 and 147 to 151 Default pull-up:
"-" is in debugging operation only; "Off" is in other than debugging operation.

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
245	AC13	DU0_EXODDF/DU0_ODDF/DISP/CDE	I	-	-	On	Open
246	AE18	DU0_DISP	I	MD10	-	Off	Pulled-up to VCCQ or pulled-down to VSS
247	AB13	DU0_CDE	I	MD13	-	Off	Pulled-up to VCCQ or pulled-down to VSS
248	AB1	VI0_CLK	I	-	-	On	Open
249	AA4	VI0_DATA0/VI0_B0	I	-	-	On	Open
250	AB3	VI0_DATA1/VI0_B1	I	-	-	On	Open
251	AA3	VI0_DATA2/VI0_B2	I	-	-	On	Open
252	AB2	VI0_DATA3/VI0_B3	I	-	-	On	Open
253	Y3	VI0_DATA4/VI0_B4	I	-	-	On	Open
254	W3	VI0_DATA5/VI0_B5	I	-	-	On	Open
255	Y2	VI0_DATA6/VI0_B6	I	-	-	On	Open
256	AA2	VI0_DATA7/VI0_B7	I	-	-	On	Open
257	AA1	VI0_CLKENB	I	-	-	On	Open
258	W2	VI0_FIELD	I	-	-	On	Open
259	Y1	VI0_HSYNC#	I	-	-	On	Open
260	W1	VI0_VSYNC#	I	-	-	On	Open
261	T5	ETH_MDIO	I	-	-	On	Open
262	V4	ETH_CRS_DV	I	-	-	On	Open
263	U5	ETH_RX_ER	I	-	-	On	Open
264	V3	ETH_RXD0	I	-	-	On	Open
265	U4	ETH_RXD1	I	-	-	On	Open
266	V5	ETH_LINK	I	-	-	On	Open
267	V1	ETH_REF_CLK	I	-	-	On	Open
268	V2	ETH_TXD1	I	-	-	On	Open
269	U3	ETH_TX_EN	I	-	-	On	Open
270	W4	ETH_MAGIC	I	-	-	On	Open
271	U2	ETH_TXD0	I	-	-	On	Open
272	W5	ETH_MDC	I	-	-	On	Open
273	U1	HSCIF0_HRX	I	-	-	On	Open
274	T4	HSCIF0_HTX	I	-	-	On	Open
275	T3	HSCIF0_HCTS#	I	-	-	On	Open
276	T2	HSCIF0_HRTS#	I	-	-	On	Open
277	T1	HSCIF0_HSCK	I	-	-	On	Open
278	Y5	I2C0_SCL	I	-	-	On	Open
279	Y4	I2C0_SDA	I	-	-	On	Open
280	Y24	I2C1_SCL	I	-	-	On	Open
281	Y25	I2C1_SDA	I	-	-	On	Open
282	W24	MSIOF0_RXD	I	-	-	On	Open
283	W23	MSIOF0_TXD	I	-	-	On	Open
284	AA25	MSIOF0_SCK	I	-	-	On	Open
285	AB25	MSIOF0_SYNC	I	-	-	On	Open
286	Y22	MSIOF0_SS1	I	-	-	On	Open
287	W22	MSIOF0_SS2	I	-	-	On	Open
288	AB23	HSCIF1_HRX	I	-	-	On	Open
289	AA23	HSCIF1_HTX	I	-	-	On	Open
290	AA24	HSCIF1_HSCK	I	-	-	On	Open
291	Y23	HSCIF1_HCTS#	I	-	-	On	Open
292	AB24	HSCIF1_HRTS#	I	-	-	On	Open
293	AC25	SCIF1_SCK	I	-	-	On	Open

5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMMR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PMMR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR6, peripheral function select registers IPSR0 to IPSR13, module select registers MOD_SEL, MOD_SEL2 and MOD_SEL3, IO cell control registers IOCTRL0 to IOCTRL3 and IOCTRL7.

5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0)

Function: GPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP0 [31]	GP0 [30]	GP0 [29]	GP0 [28]	GP0 [27]	GP0 [26]	GP0 [25]	GP0 [24]	GP0 [23]	GP0 [22]	GP0 [21]	GP0 [20]	GP0 [19]	GP0 [18]	GP0 [17]	GP0 [16]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP0 [15]	GP0 [14]	GP0 [13]	GP0 [12]	GP0 [11]	GP0 [10]	GP0 [9]	GP0 [8]	GP0 [7]	GP0 [6]	GP0 [5]	GP0 [4]	GP0 [3]	GP0 [2]	GP0 [1]	GP0 [0]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP0[31:0]	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP6[25]	GP-6-25	Peripheral function selected by IP0[21:20]
GP6[26]	-	-
GP6[27]	-	-
GP6[28]	-	-
GP6[29]	-	-
GP6[30]	-	-
GP6[31]	-	-

5.3.11 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP2 [31]	IP2 [30]	IP2 [29]	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP2[1:0]	A7	SCIFB0_RTS_N	SCIFA4_TXD_B	-	-	-	-	-	-
IP2[3:2]	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	-	-
IP2[5:4]	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	-	-
IP2[7:6]	A10	MSIOF1_SCK	IIC0_SCL_B (I2C6)	-	-	-	-	-	-
IP2[9:8]	A11	MSIOF1_SYNC	IIC0_SDA_B (I2C6)	-	-	-	-	-	-
IP2[11:10]	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	-	-
IP2[13:12]	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	-	-
IP2[15:14]	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1_N	-	-	-	-	-
IP2[17:16]	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	-	-
IP2[20:18]	A16	MSIOF2_SCK	HSCIF0_HSCK_B	Reserved	Reserved	CAN_CLK_C	TPUTO2_B	-	-
IP2[23:21]	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	Reserved	-	-	-	-
IP2[26:24]	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	Reserved	-	-	-	-
IP2[29:27]	A19	MSIOF2_SS2	PWM4	TPUTO2	Reserved	-	-	-	-
IP2[31:30]	A20	SPCLK	Reserved	-	-	-	-	-	-

Legend: - Setting prohibited

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP1[5]	A21	MOSI_IO0	Reserved	-	-	-	-	-	GP1[5]	IP3[1:0]
GP1[6]	A22	MISO_IO1	Reserved	ATADIR1_N	-	-	-	-	GP1[6]	IP3[3:2]
GP1[7]	A23	IO2	Reserved	ATAWR1_N	-	-	-	-	GP1[7]	IP3[5:4]
GP1[8]	A24	IO3	EX_WAIT2	-	-	-	-	-	GP1[8]	IP3[7:6]
GP1[9]	A25	SSL	ATARD1_N	-	-	-	-	-	GP1[9]	IP3[9:8]
GP1[10]	CS0_N	VI1_DATA8	-	-	-	-	-	-	GP1[10]	IP3[10]
GP1[11]	CS1_N_A26	VI1_DATA9	-	-	-	-	-	-	GP1[11]	IP3[11]
GP1[12]	EX_CS0_N	VI1_DATA10	-	-	-	-	-	-	GP1[12]	IP3[12]
GP1[13]	EX_CS1_N	TPUTO3_B	SCIFB2_RXD	VI1_DATA11	-	-	-	-	GP1[13]	IP3[14:13]
GP1[14]	EX_CS2_N	PWM0	SCIF4_RXD_C	Reserved	Reserved	TPUTO3	SCIFB2_TXD	Reserved	GP1[14]	IP3[17:15]
GP1[15]	EX_CS3_N	SCIFA2_SCK	SCIF4_TXD_C	Reserved	Reserved	Reserved	SCIFB2_SCK	Reserved	GP1[15]	IP3[20:18]
GP1[16]	EX_CS4_N	SCIFA2_RXD	I2C2_SCL_E	Reserved	Reserved	Reserved	SCIFB2_CTS_N	Reserved	GP1[16]	IP3[23:21]
GP1[17]	EX_CS5_N	SCIFA2_TXD	I2C2_SDA_E	Reserved	Reserved	Reserved	SCIFB2_RTS_N	Reserved	GP1[17]	IP3[26:24]
GP1[18]	BS_N	DRACK0	PWM1_C	TPUTO0_C	ATACS01_N	Reserved	-	-	GP1[18]	IP3[29:27]
GP1[19]	RD_N	ATACS11_N	-	-	-	-	-	-	GP1[19]	IP3[30]
GP1[20]	RD_WR_N	ATAG1_N	-	-	-	-	-	-	GP1[20]	IP3[31]
GP1[21]	WE0_N	-	-	-	-	-	-	-	GP1[21]	-
GP1[22]	WE1_N	-	-	-	-	-	-	-	GP1[22]	-
GP1[23]	EX_WAIT0	CAN_CLK_B	SCIF_CLK	Reserved	-	-	-	-	GP1[23]	IP4[1:0]
GP1[24]	DREQ0_N	SCIFB1_RXD	-	-	-	-	-	-	GP1[24]	IP7[31]
GP1[25]	DACK0	-	-	-	-	-	-	-	GP1[25]	-
GP2[0]	DU0_DR0	Reserved	SCIF5_RXD_C	I2C2_SCL_D	Reserved	-	-	-	GP2[0]	IP4[4:2]
GP2[1]	DU0_DR1	Reserved	SCIF5_TXD_C	I2C2_SDA_D	Reserved	-	-	-	GP2[1]	IP4[7:5]
GP2[2]	DU0_DR2	Reserved	Reserved	-	-	-	-	-	GP2[2]	IP4[9:8]
GP2[3]	DU0_DR3	Reserved	Reserved	-	-	-	-	-	GP2[3]	IP4[11:10]
GP2[4]	DU0_DR4	Reserved	Reserved	-	-	-	-	-	GP2[4]	IP4[13:12]
GP2[5]	DU0_DR5	Reserved	Reserved	-	-	-	-	-	GP2[5]	IP4[15:14]
GP2[6]	DU0_DR6	Reserved	Reserved	-	-	-	-	-	GP2[6]	IP4[17:16]
GP2[7]	DU0_DR7	Reserved	Reserved	-	-	-	-	-	GP2[7]	IP4[19:18]
GP2[8]	DU0_DG0	Reserved	SCIFA0_RXD_C	I2C3_SCL_D	Reserved	-	-	-	GP2[8]	IP4[22:20]
GP2[9]	DU0_DG1	Reserved	SCIFA0_TXD_C	I2C3_SDA_D	Reserved	-	-	-	GP2[9]	IP4[25:23]
GP2[10]	DU0_DG2	Reserved	Reserved	-	-	-	-	-	GP2[10]	IP4[27:26]
GP2[11]	DU0_DG3	Reserved	Reserved	-	-	-	-	-	GP2[11]	IP4[29:28]
GP2[12]	DU0_DG4	Reserved	Reserved	-	-	-	-	-	GP2[12]	IP4[31:30]
GP2[13]	DU0_DG5	Reserved	Reserved	-	-	-	-	-	GP2[13]	IP5[1:0]
GP2[14]	DU0_DG6	Reserved	Reserved	-	-	-	-	-	GP2[14]	IP5[3:2]
GP2[15]	DU0_DG7	Reserved	Reserved	-	-	-	-	-	GP2[15]	IP5[5:4]
GP2[16]	DU0_DB0	Reserved	SCIFA4_RXD_C	I2C4_SCL_D	CAN0_RX_C	Reserved	-	-	GP2[16]	IP5[8:6]
GP2[17]	DU0_DB1	Reserved	SCIFA4_TXD_C	I2C4_SDA_D	CAN0_TX_C	Reserved	-	-	GP2[17]	IP5[11:9]
GP2[18]	DU0_DB2	Reserved	Reserved	-	-	-	-	-	GP2[18]	IP5[13:12]
GP2[19]	DU0_DB3	Reserved	Reserved	-	-	-	-	-	GP2[19]	IP5[15:14]
GP2[20]	DU0_DB4	Reserved	Reserved	-	-	-	-	-	GP2[20]	IP5[17:16]

Bit Name	Set Value = 1
PUPR2[6]	DU0_DR6 is pull up
PUPR2[5]	DU0_DR5 is pull up
PUPR2[4]	DU0_DR4 is pull up
PUPR2[3]	DU0_DR3 is pull up
PUPR2[2]	DU0_DR2 is pull up
PUPR2[1]	DU0_DR1 is pull up
PUPR2[0]	DU0_DR0 is pull up

5.3.29 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR3 [31]	PUPR3 [30]	PUPR3 [29]	PUPR3 [28]	PUPR3 [27]	PUPR3 [26]	PUPR3 [25]	PUPR3 [24]	PUPR3 [23]	PUPR3 [22]	PUPR3 [21]	PUPR3 [20]	PUPR3 [19]	PUPR3 [18]	PUPR3 [17]	PUPR3 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR3 [15]	PUPR3 [14]	PUPR3 [13]	PUPR3 [12]	PUPR3 [11]	PUPR3 [10]	PUPR3 [9]	PUPR3 [8]	PUPR3 [7]	PUPR3 [6]	PUPR3 [5]	PUPR3 [4]	PUPR3 [3]	PUPR3 [2]	PUPR3 [1]	PUPR3 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR3[31:0]	H'FFFF FFFF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR3[31]	I2C1_SDA is pull up
PUPR3[30]	I2C1_SCL is pull up
PUPR3[29]	I2C0_SDA is pull up
PUPR3[28]	I2C0_SCL is pull up
PUPR3[27]	HSCIF0_HSCK is pull up
PUPR3[26]	HSCIF0_HRTS_N is pull up
PUPR3[25]	HSCIF0_HCTS_N is pull up
PUPR3[24]	HSCIF0_HTX is pull up
PUPR3[23]	HSCIF0_HRX is pull up
PUPR3[22]	ETH_MDC is pull up
PUPR3[21]	ETH_TXD0 is pull up
PUPR3[20]	ETH_MAGIC is pull up
PUPR3[19]	ETH_TX_EN is pull up
PUPR3[18]	ETH_TXD1 is pull up
PUPR3[17]	ETH_REF_CLK is pull up
PUPR3[16]	ETH_LINK is pull up
PUPR3[15]	ETH_RXD1 is pull up
PUPR3[14]	ETH_RXD0 is pull up
PUPR3[13]	ETH_RX_ER is pull up
PUPR3[12]	ETH_CRS_DV is pull up
PUPR3[11]	ETH_MDIO is pull up
PUPR3[10]	VI0_VSYNC_N is pull up
PUPR3[9]	VI0_HSYNC_N is pull up
PUPR3[8]	VI0_FIELD is pull up
PUPR3[7]	VI0_CLKENB is pull up

5.3.33 SD Control Register 0 (IOCTRL0)

Function: IOCTRL0 controls the driving abilities of pins in use for the MMC and SD0 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	drv2_mmcclk	drv1_mmcclk	drv2_mmccmd	drv1_mmccmd	drv2_mmcd0	drv1_mmcd0	drv2_mmcd1	drv1_mmcd1	drv2_mmcd2	drv1_mmcd2	drv2_mmcd3	drv1_mmcd3	drv2_mmcd4	drv1_mmcd4	drv2_mmcd5	drv1_mmcd5
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_mmcd6	drv1_mmcd6	drv2_mmcd7	drv1_mmcd7	drv2_sd0cd	drv1_sd0cd	drv2_sd0clk	drv1_sd0clk	drv2_sd0cmd	drv1_sd0cmd	drv2_sd0data0	drv1_sd0data0	drv2_sd0data1	drv1_sd0data1	drv2_sd0data2	drv1_sd0data2
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_mmcclk	1	R/W	MMC_CLK Setting.
30	drv1_mmcclk	1	R/W	The value of these bits must be 11.
29	drv2_mmccmd	1	R/W	MMC_CMD Setting.
28	drv1_mmccmd	1	R/W	The value of these bits must be 11.
27	drv2_mmcd0	1	R/W	MMC_CD0 Setting.
26	drv1_mmcd0	1	R/W	The value of these bits must be 11.
25	drv2_mmcd1	1	R/W	MMC_CD1 Setting.
24	drv1_mmcd1	1	R/W	The value of these bits must be 11.
23	drv2_mmcd2	1	R/W	MMC_CD2 Setting.
22	drv1_mmcd2	1	R/W	The value of these bits must be 11.
21	drv2_mmcd3	1	R/W	MMC_CD3 Setting.
20	drv1_mmcd3	1	R/W	The value of these bits must be 11.
19	drv2_mmcd4	1	R/W	MMC_CD4 Setting.
18	drv1_mmcd4	1	R/W	The value of these bits must be 11.
17	drv2_mmcd5	1	R/W	MMC_CD5 Setting.
16	drv1_mmcd5	1	R/W	The value of these bits must be 11.
15	drv2_mmcd6	1	R/W	MMC_CD6 Setting.
14	drv1_mmcd6	1	R/W	The value of these bits must be 11.
13	drv2_mmcd7	1	R/W	MMC_CD7 Setting.
12	drv1_mmcd7	1	R/W	The value of these bits must be 11.
11	drv2_sd0cd	1	R/W	SD0_CD Setting.
10	drv1_sd0cd	1	R/W	The value of these bits must be 11.
9	drv2_sd0clk	1	R/W	SD0_CLK Setting.
8	drv1_sd0clk	1	R/W	The value of these bits must be 11.
7	drv2_sd0cmd	1	R/W	SD0_CMD Setting.
6	drv1_sd0cmd	1	R/W	The value of these bits must be 11.
5	drv2_sd0data0	1	R/W	SD0_DATA0 Setting.
4	drv1_sd0data0	1	R/W	The value of these bits must be 11.
3	drv2_sd0data1	1	R/W	SD0_DATA1 Setting.
2	drv1_sd0data1	1	R/W	The value of these bits must be 11.

5.3.35 TDSEL Control Register (IOCTRL2)

Function: IOCTRL2 controls the delay of clock of pins in use for the IRQ, DU and Ethernet interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	tdsel1_a10	tdsel0_a10	tdsel1_a16	tdsel0_a16	tdsel1_audioclkb	tdsel0_audioclkb	tdsel1_ethrxer	tdsel0_ethrxer	tdsel1_excs3n	tdsel0_excs3n	tdsel1_i2c1sda	tdsel0_i2c1sda	tdsel1_mmcclk	tdsel0_mmcclk	tdsel1_msiof0sck	tdsel0_msiof0sck
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tdsel1_msiof0sync	tdsel0_msiof0sync	tdsel1_sd0clk	tdsel0_sd0clk	tdsel1_sd1clk	tdsel0_sd1clk	tdsel1_ssisdata0	tdsel0_ssisdata0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	tdsel1_a10	0	R/W	A10 Setting.
30	tdsel0_a10	0	R/W	The value of these bits must be 00.
29	tdsel1_a16	0	R/W	A16 Setting.
28	tdsel0_a16	0	R/W	The value of these bits must be 00.
27	tdsel1_audioclkb	0	R/W	AUDIO_CLKB Setting.
26	tdsel0_audioclkb	0	R/W	The value of these bits must be 00.
25	tdsel1_ethrxer	0	R/W	ETH_RX_ER Setting.
24	tdsel0_ethrxer	0	R/W	The value of these bits must be 00.
23	tdsel1_excs3n	0	R/W	EX_CS3_N Setting.
22	tdsel0_excs3n	0	R/W	The value of these bits must be 00.
21	tdsel1_i2c1sda	0	R/W	I2C1_SDA Setting.
20	tdsel0_i2c1sda	0	R/W	The value of these bits must be 00.
19	tdsel1_mmcclk	0	R/W	MMC_CLK Setting.
18	tdsel0_mmcclk	0	R/W	The value of these bits must be 00.
17	tdsel1_msiof0sck	0	R/W	MSIOF0_SCK Setting.
16	tdsel0_msiof0sck	0	R/W	The value of these bits must be 00.
15	tdsel1_msiof0sync	0	R/W	MSIOF0_SYNC Setting.
14	tdsel0_msiof0sync	0	R/W	The value of these bits must be 00.
13	tdsel1_sd0clk	0	R/W	SD0_CLK Setting.
12	tdsel0_sd0clk	0	R/W	The value of these bits must be 00.
11	tdsel1_sd1clk	0	R/W	SD1_CLK Setting.
10	tdsel0_sd1clk	0	R/W	The value of these bits must be 00.
9	tdsel1_ssisdata0	0	R/W	SSI_SDATA0 Setting.
8	tdsel0_ssisdata0	0	R/W	The value of these bits must be 00.
7 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.