Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	1GHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77450ha02bg-ua

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Item	Description
LBSC-DMAC	• Number of channels: LBSC-DMAC three channels • Address space: Physical address space • Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral • Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side. • Transfer data length: Peripheral (APB-bus) side : 1, 2, 4 bytes Memory (AXI-bus) side : 4 or 16 (channel 2), 32 (channel 0 and 1) bytes • Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01) • Number of transfers — Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00) — Minimum number of transfers: One • Address mode: Dual address mode • Transfer modes: Single transfer mode, continuous transfer mode • Transfer end interrupt: Occurs at the end of the number of transfers specified in the register
DDR3-SDRAM bus state controller (DBSC)	• 1 channel (32-bit bus) • DDR3-SDRAM can be connected directly. • Memory Size: Up to 2 GB (8-Gbit memory × 2) • Data bus width: 32 bits × 1 • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Deep-Power-Down-Mode supported • Auto Pre-charge Mode/Bank Active Mode • DDR Back Up supported
Memory connections	DDR3-SDRAM compliant to JEDEC JESD79-3E Supports from 512-Mbit to 8-Gbit memory unit configurations 32-bit DDR3-1333 (four units with 8-bit width)

1.3.7 Video Processing

Item	Description
Video signal processor 1 (VSP1)	The VSP1 is the successor IP of Renesas' VIO6-IP series, and has the following features. (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) Full HD Video Processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Blending of four picture layers and raster operations (ROPs) (3) Full HD Picture Quality/Color Correction with 1D/3D Look Up Table(LUT) — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) — Hue, brightness, and saturation adjustment — 1D histogram (4) Direct Connection to Display Module — Display unit (DU) supported

Table 4.1 List of Multiplexed Pin Functions

DBSC3 (No.1 to 40): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
1	DBSC3	X
D15	M0CKE0	1.5/1.35V(VDDQ_M0BKUP)/-
	O(L)	-
2	DBSC3	X
E11	M0CKE1	1.5/1.35V(VDDQ_M0 BKUP)/-
	O(L)	-
3	DBSC3	P
D14	M0VREFCA	1.5/1.35V(VDDQ_M0 BKUP)/-
	P	-
4	DBSC3	I
E7	M0BKPRST#	1.5/1.35V(VDDQ_M0 BKUP)/-
	I	-
5	DBSC3	H
D12	M0RESET#	1.5/1.35V(VDDQ_M0BKUP)/-
	O(H to L)	-
6	DBSC3	X
A15	M0CK0	1.5/1.35V(VDDQ_M0)/-
	O	-
7	DBSC3	X
A14	M0CK0#	1.5/1.35V(VDDQ_M0)/-
	O	-
8	DBSC3	X
C11	M0CK1	1.5/1.35V(VDDQ_M0)/-
	O	-
9	DBSC3	X
C10	M0CK1#	1.5/1.35V(VDDQ_M0)/-
	O	-
10	DBSC3	H
C15	M0CS0#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
11	DBSC3	H
E10	M0CS1#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
12	DBSC3	L
B16	M0ODT0	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
13	DBSC3	L
D11	M0ODT1	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
14	DBSC3	IO
D9	M0ZQ	1.5/1.35V(VDDQ_M0)/-
	IO	-
15	DBSC3	H
E14	M0WE#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
16	DBSC3	H
D16	M0RAS#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
17	DBSC3	H
E13	M0CAS#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
18	DBSC3	L
B9	M0A0	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
19	DBSC3	L
B12	M0A1	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
20	DBSC3	L
A11	M0A2	1.5/1.35V(VDDQ_M0)/-
	O(L)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
21	DBSC3	L
B10	M0A3	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
22	DBSC3	L
B13	M0A4	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
23	DBSC3	L
B8	M0A5	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
24	DBSC3	L
A7	M0A6	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
25	DBSC3	L
B14	M0A7	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
26	DBSC3	L
D8	M0A8	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
27	DBSC3	L
B11	M0A9	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
28	DBSC3	L
A8	M0A10	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
29	DBSC3	L
A9	M0A11	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
30	DBSC3	L
A6	M0A12	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
31	DBSC3	L
B7	M0A13	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
32	DBSC3	L
D7	M0A14	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
33	DBSC3	L
A12	M0A15	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
34	DBSC3	L
E12	M0BA0	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
35	DBSC3	L
A10	M0BA1	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
36	DBSC3	L
D13	M0BA2	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
37	DBSC3	P
F12	VDDQ_M0APLL	1.8V(VDDQ_M0APLL)/-
	P	-
38	DBSC3	P
F13	VSSQ_M0APLL	GND(VDDQ_M0APLL)/-
	P	-
39	DBSC3	Z
E20	M0DQ0	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
40	DBSC3	Z
D21	M0DQ1	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-

1/3 (DBSC3)

CPG, RESET, SYSTEM, Debug, USB (No.94 to 116): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
94	CPG	I
V25	EXTAL	1.8V(VCCQ18)/-
	I	-
95	CPG	O
V24	XTAL	1.8V(VCCQ18)/-
	O	-
96	PLL	P
E8	VDD_CPGPLL0	1.8V(VDD_CPGPLL0)/-
	P	-
97	PLL	P
E9	VSS_CPGPLL0	GND(VDD_CPGPLL0)/-
	P	-
98	PLL	P
K15/L15	VDD_CPGPLL1	1.8V(VDD_CPGPLL1)/-
	P	-
99	PLL	P
K16/L16	VSS_CPGPLL1	GND(VDD_CPGPLL1)/-
	P	-
100	PLL	P
K12/L12	VDD_CPGPLL3	1.8V(VDD_CPGPLL3)/-
	P	-
101	PLL	P
K11/L11	VSS_CPGPLL3	GND(VDD_CPGPLL3)/-
	P	-
102	RESET	I(S, L)
V23	PRESET#	1.8V(VCCQ18)/-
	I(S)	-
103	RESET	O(L)
B6	PRESETOUT#	3.3V(VCCQ18)/4mA
	O(L to H)	-
104	SYSTEM	I(S)
R21	BSMODE	1.8V(VCCQ18)/-
	I(S)	-
105	Debug	I
N21	TRST#	1.8V(VCCQ18)/-
	I	On

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
106	Debug	I
N22	TCK	1.8V(VCCQ18)/-
	I	On
107	Debug	I
P21	TMS	1.8V(VCCQ18)/-
	I	On
108	Debug	I
R22	TDI	1.8V(VCCQ18)/-
	I	On
109	Debug	Z
P22	TDO	1.8V(VCCQ18)/4mA
	O(Z)	-
110	Debug	I
U23	ACK	1.8V(VCCQ18)/4mA
	IO(I)	On(pull-down)
111	USB	I
T25	USB_EXTAL	1.8V(VCCQ18)/-
	I	-
112	USB	O
T24	USB_XTAL	1.8V(VCCQ18)/-
	O	-
113	USB	P
P20	VD331	3.3V(VD331)/-
	P	-
114	USB	P
R20	VD181	1.8V(VD181)/-
	P	-
115	USB	P
P23	AVDD	1.8V(AVDD)/-
	P	-
116	USB	P
M20	AVSS	GND(AVDD)/-
	P	-

LBSC, SCIFB, PWM, TPU, SCIFA, MSIOF, IIC, HSCIF, RCAN, QSPI and GPIO (No.177 to 196): Up to 8-Function Multiplexed and Mode Pin assigned (No.177, 180, 182, 186, 188, 191 and 192)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.
When MD[3:1]=000, the LBSC will execute area 0 booting; MD[3:1]≠000, the QSPI will execute QSPI booting.

Function	1	2	3	4	5	6	7	GPIO	
MD[3:1]	=000							≠000	
No.									During POR
Pin No.									V(power)/|IOH|
Mode Pin									Pull-up
177	LBSC	SCIFB0	-	-	-	-	-		I(Mode Pin)
H4	A4	SCIFB0_TXD	-	-	-	-	-	GP0_20	3.3V(VCCQ)/8mA
MD1	O(L)	O	-	-	-	-	-	IO(I)	Off
178	LBSC	SCIFB0	PWM4	TPU	-	-	-		I(GPIO)
F2	A5	SCIFB0_RXD	PWM4_B	TPUTO3_C	-	-	-	GP0_21	3.3V(VCCQ)/8mA
	O(L)	I	O	O	-	-	-	IO(I)	On
179	LBSC	SCIFB0	SCIFA4	TPU	-	-	-		I(GPIO)
G5	A6	SCIFB0_CTS#	SCIFA4_RXD_B	TPUTO2_C	-	-	-	GP0_22	3.3V(VCCQ)/8mA
	O(L)	I	I	O	-	-	-	IO(I)	On
180	LBSC	SCIFB0	SCIFA4	-	-	-	-		I(Mode Pin)
F1	A7	SCIFB0_RTS#	SCIFA4_TXD_B	-	-	-	-	GP0_23	3.3V(VCCQ)/8mA
MD4	O(L)	O	O	-	-	-	-	IO(I)	Off
181	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(GPIO)
J5	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	GP0_24	3.3V(VCCQ)/8mA
	O(L)	I	I	-	-	-	-	IO(I)	On
182	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(Mode Pin)
G2	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	GP0_25	3.3V(VCCQ)/8mA
MD5	O(L)	O	O	-	-	-	-	IO(I)	Off
183	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
J4	A10	MSIOF1_SCK	IIC0_SCL_B	-	-	-	-	GP0_26	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
184	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
H3	A11	MSIOF1_SYNC	IIC0_SDA_B	-	-	-	-	GP0_27	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
185	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(GPIO)
G3	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	GP0_28	3.3V(VCCQ)/8mA
	O(L)	O	I	-	-	-	-	IO(I)	On
186	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(Mode Pin)
G1	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	GP0_29	3.3V(VCCQ)/8mA
MD6	O(L)	O	O	-	-	-	-	IO(I)	Off
187	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(GPIO)
K5	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1#	-	-	-	GP0_30	3.3V(VCCQ)/8mA
	O(L)	I	I	I	-	-	-	IO(I)	On
188	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(Mode Pin)
H1	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	GP0_31	3.3V(VCCQ)/8mA
MD7	O(L)	O	O	O	-	-	-	IO(I)	Off
189	LBSC	MSIOF2	HSCIF0	Reserved	Reserved	RCAN	TPU		I(GPIO)
J2	A16	MSIOF2_SCK	HSCIF0_HSCK_B	-	-	CAN_CLK_C	TPUTO2_B	GP1_0	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	I	O	IO(I)	On
190	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(GPIO)
K4	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	-	-	-	GP1_1	3.3V(VCCQ)/8mA
	O(L)	IO	I	I	-	-	-	IO(I)	On
191	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(Mode Pin)
H2	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	-	-	-	GP1_2	3.3V(VCCQ)/8mA
MDT0	O(L)	O	O	O	-	-	-	IO(I)	Off
192	LBSC	MSIOF2	PWM4	TPU	Reserved	-	-		I(Mode Pin)
K3	A19	MSIOF2_SS2	PWM4	TPUTO2	-	-	-	GP1_3	3.3V(VCCQ)/8mA
MD18	O(L)	O	O	O	-	-	-	IO(I)	Off
193	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K2	A20	SPCLK	-	-	-	-	-	GP1_4	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
194	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K1	A21	MOSI/IO0	-	-	-	-	-	GP1_5	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
195	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
L3	A22	MISO/IO1	-	ATADIR1#	-	-	-	GP1_6	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On
196	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
J3	A23	IO2	-	ATAWR1#	-	-	-	GP1_7	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
148	AA9	MMC_D0	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
149	AA11	MMC_D1	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
150	AC9	MMC_D2	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
151	AA10	MMC_D3	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
152	AB10	MMC_D4	I	-	-	Off	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
153	AD10	MMC_D5	I	-	-	Off	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
154	AB9	MMC_D6	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
155	AB11	MMC_D7	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
156	AC10	VCCQ_MMC_SD2	P	-	-	-	Must be used
157	D6	D0	I	-	Area 0	On	Open
158	E6	D1	I	-	Area 0	On	Open
159	A5	D2	I	-	Area 0	On	Open
160	C6	D3	I	-	Area 0	On	Open
161	A4	D4	I	-	Area 0	On	Open
162	C5	D5	I	-	Area 0	On	Open
163	B4	D6	I	-	Area 0	On	Open
164	B5	D7	I	-	Area 0	On	Open
165	C4	D8	I	-	Area 0	On	Open
166	A3	D9	I	-	Area 0	On	Open
167	E4	D10	I	-	Area 0	On	Open
168	B3	D11	I	-	Area 0	On	Open
169	A2	D12	I	-	Area 0	On	Open
170	D5	D13	I	-	Area 0	On	Open
171	D3	D14	I	-	Area 0	On	Open
172	F5	D15	I	-	Area 0	On	Open
173	F4	A0	L/I	MD3	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
174	F3	A1	L/I	MD0	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
175	G4	A2	L/I	MDT1	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
176	H5	A3	L/I	MD2	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
177	H4	A4	L/I	MD1	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
178	F2	A5	L/I	-	Area 0	On	Open
179	G5	A6	L/I	-	Area 0	On	Open
180	F1	A7	L/I	MD4	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
181	J5	A8	L/I	-	Area 0	On	Open
182	G2	A9	L/I	MD5	Area 0	Off	Pulled-up to VCCQ
183	J4	A10	L/I	-	Area 0	On	Open
184	H3	A11	L/I	-	Area 0	On	Open
185	G3	A12	L/I	-	Area 0	On	Open
186	G1	A13	L/I	MD6	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
187	K5	A14	L/I	-	Area 0	On	Open
188	H1	A15	L/I	MD7	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
189	J2	A16	L/I	-	Area 0	On	Open
190	K4	A17	L/I	-	Area 0	On	Open
191	H2	A18	L/I	MDT0	-	Off	Pulled-up to VCCQ or pulled-down to VSS
192	K3	A19	L/I	MD18	-	Off	Pulled-down to VSS
193	K2	A20	L/I	-	QSPI	On	Open
194	K1	A21	L/I	-	QSPI	On	Open
195	L3	A22	L/I	-	QSPI	On	Open
196	J3	A23	L/I	-	QSPI	On	Open
197	J1	A24	L/I	-	QSPI	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
198	L2	A25	L/I	-	QSPI	On	Open
199	B1	CLKOUT	O	-	Area 0	-	Open
200	E2	CS0#	H/I	-	Area 0	On	Open
201	M5	[CS1#/A26]	[H or L] (*4)/I	-	Area 0	On	Open
202	E1	EX_CS0#	I	-	-	On	Open
203	E3	EX_CS1#	I	-	-	On	Open
204	D1	EX_CS2#	I	-	-	On	Open
205	D2	EX_CS3#	I	-	-	On	Open
206	C1	EX_CS4#	I	-	-	On	Open
207	B2	EX_CS5#	I	-	-	On	Open
208	M4	BS#	H/I	MD8	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
209	M3	RD#	H/I	MD14	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
210	M1	RD/WR#	I	MD9	-	Off	Pulled-up to VCCQ or pulled-down to VSS
211	L1	WE0#	H/I	MD19	Area 0	Off	Pulled-up to VCCQ
212	L4	WE1#	H/I	MD20	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
213	C2	EX_WAIT0	I/I	-	Area 0	On	Open
214	L5	DREQ0#	I	-	-	On	Open
215	M2	DACK0	I	MD21	-	Off	Pulled-up to VCCQ or pulled-down to VSS
216	AA18	DU0_DR0	I	-	-	On	Open
217	AB18	DU0_DR1	I	-	-	On	Open
218	AE19	DU0_DR2	I	-	-	On	Open
219	AC18	DU0_DR3	I	-	-	On	Open
220	AD19	DU0_DR4	I	-	-	On	Open
221	AD17	DU0_DR5	I	-	-	On	Open
222	AC17	DU0_DR6	I	-	-	On	Open
223	AC19	DU0_DR7	I	-	-	On	Open
224	AA17	DU0_DG0	I	-	-	On	Open
225	AB16	DU0_DG1	I	-	-	On	Open
226	AD18	DU0_DG2	I	-	-	On	Open
227	AD16	DU0_DG3	I	-	-	On	Open
228	AB17	DU0_DG4	I	-	-	On	Open
229	AA16	DU0_DG5	I	-	-	On	Open
230	AE16	DU0_DG6	I	-	-	On	Open
231	AC16	DU0_DG7	I	-	-	On	Open
232	AC14	DU0_DB0	I	-	-	On	Open
233	AE17	DU0_DB1	I	-	-	On	Open
234	AA15	DU0_DB2	I	-	-	On	Open
235	AB15	DU0_DB3	I	-	-	On	Open
236	AD14	DU0_DB4	I	-	-	On	Open
237	AD15	DU0_DB5	I	-	-	On	Open
238	AA14	DU0_DB6	I	-	-	On	Open
239	AC15	DU0_DB7	I	-	-	On	Open
240	AE15	DU0_DOTCLKIN	I	-	-	On	Open
241	AE14	DU0_DOTCLKOUT0	I	-	-	On	Open
242	AE13	DU0_DOTCLKOUT1	I	-	-	On	Open
243	AD13	DU0_EXHSYNC/DU0_HSYNC	I	MD11	-	Off	Pulled-up to VCCQ or pulled-down to VSS
244	AB14	DU0_EXVSYNC/DU0_VSYNC	I	MD12	-	Off	Pulled-up to VCCQ or pulled-down to VSS

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[25]	GP-3-25	Peripheral function selected by IP8[5:3]
GP3[26]	GP-3-26	Peripheral function selected by IP8[8:6]
GP3[27]	GP-3-27	Peripheral function selected by IP8[11:9]
GP3[28]	GP-3-28	Peripheral function selected by IP8[14:12]
GP3[29]	GP-3-29	Peripheral function selected by IP8[16:15]
GP3[30]	GP-3-30	Peripheral function selected by IP8[19:17]
GP3[31]	GP-3-31	Peripheral function selected by IP8[22:20]

5.3.12 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP3 [31]	IP3 [30]	IP3 [29]	IP3 [28]	IP3 [27]	IP3 [26]	IP3 [25]	IP3 [24]	IP3 [23]	IP3 [22]	IP3 [21]	IP3 [20]	IP3 [19]	IP3 [18]	IP3 [17]	IP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP3 [15]	IP3 [14]	IP3 [13]	IP3 [12]	IP3 [11]	IP3 [10]	IP3 [9]	IP3 [8]	IP3 [7]	IP3 [6]	IP3 [5]	IP3 [4]	IP3 [3]	IP3 [2]	IP3 [1]	IP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP3[1:0]	A21	MOSI_IO0	Reserved	-	-	-	-	-	-
IP3[3:2]	A22	MISO_IO1	Reserved	ATADIR1_N	-	-	-	-	-
IP3[5:4]	A23	IO2	Reserved	ATAWR1_N	-	-	-	-	-
IP3[7:6]	A24	IO3	EX_WAIT2	-	-	-	-	-	-
IP3[9:8]	A25	SSL	ATARD1_N	-	-	-	-	-	-
IP3[10]	CS0_N	VI1_DATA8	-	-	-	-	-	-	-
IP3[11]	CS1_N_A26	VI1_DATA9	-	-	-	-	-	-	-
IP3[12]	EX_CS0_N	VI1_DATA10	-	-	-	-	-	-	-
IP3[14:13]	EX_CS1_N	TPUTO3_B	SCIFB2_RXD	VI1_DATA11	-	-	-	-	-
IP3[17:15]	EX_CS2_N	PWM0	SCIF4_RXD_C	Reserved	Reserved	TPUTO3	SCIFB2_TXD	Reserved	-
IP3[20:18]	EX_CS3_N	SCIFA2_SCK	SCIF4_TXD_C	Reserved	Reserved	Reserved	SCIFB2_SCK	Reserved	-
IP3[23:21]	EX_CS4_N	SCIFA2_RXD	I2C2_SCL_E	Reserved	Reserved	Reserved	SCIFB2_CTS_N	Reserved	-
IP3[26:24]	EX_CS5_N	SCIFA2_TXD	I2C2_SDA_E	Reserved	Reserved	Reserved	SCIFB2_RTS_N	Reserved	-
IP3[29:27]	BS_N	DRACK0	PWM1_C	TPUTO0_C	ATACS01_N	Reserved	-	-	-
IP3[30]	RD_N	ATACS11_N	-	-	-	-	-	-	-
IP3[31]	RD_WR_N	ATAG1_N	-	-	-	-	-	-	-

Legend: - Setting prohibited

5.3.13 Peripheral Function Select Register 4 (IPSR4)

Function: IPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP4 [31]	IP4 [30]	IP4 [29]	IP4 [28]	IP4 [27]	IP4 [26]	IP4 [25]	IP4 [24]	IP4 [23]	IP4 [22]	IP4 [21]	IP4 [20]	IP4 [19]	IP4 [18]	IP4 [17]	IP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP4 [15]	IP4 [14]	IP4 [13]	IP4 [12]	IP4 [11]	IP4 [10]	IP4 [9]	IP4 [8]	IP4 [7]	IP4 [6]	IP4 [5]	IP4 [4]	IP4 [3]	IP4 [2]	IP4 [1]	IP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP4[1:0]	EX_WAIT0	CAN_CLK_B	SCIF_CLK	Reserved	-	-	-
IP4[4:2]	DU0_DR0	Reserved	SCIF5_RXD_C	I2C2_SCL_D	Reserved	-	-
IP4[7:5]	DU0_DR1	Reserved	SCIF5_TXD_C	I2C2_SDA_D	Reserved	-	-
IP4[9:8]	DU0_DR2	Reserved	Reserved	-	-	-	-
IP4[11:10]	DU0_DR3	Reserved	Reserved	-	-	-	-
IP4[13:12]	DU0_DR4	Reserved	Reserved	-	-	-	-
IP4[15:14]	DU0_DR5	Reserved	Reserved	-	-	-	-
IP4[17:16]	DU0_DR6	Reserved	Reserved	-	-	-	-
IP4[19:18]	DU0_DR7	Reserved	Reserved	-	-	-	-
IP4[22:20]	DU0_DG0	Reserved	SCIFA0_RXD_C	I2C3_SCL_D	Reserved	-	-
IP4[25:23]	DU0_DG1	Reserved	SCIFA0_TXD_C	I2C3_SDA_D	Reserved	-	-
IP4[27:26]	DU0_DG2	Reserved	Reserved	-	-	-	-
IP4[29:28]	DU0_DG3	Reserved	Reserved	-	-	-	-
IP4[31:30]	DU0_DG4	Reserved	Reserved	-	-	-	-

Legend: - Setting prohibited

5.3.15 Peripheral Function Select Register 6 (IPSR6)

Function: IPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP6 [31]	IP6 [30]	IP6 [29]	IP6 [28]	IP6 [27]	IP6 [26]	IP6 [25]	IP6 [24]	IP6 [23]	IP6 [22]	IP6 [21]	IP6 [20]	IP6 [19]	IP6 [18]	IP6 [17]	IP6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP6 [15]	IP6 [14]	IP6 [13]	IP6 [12]	IP6 [11]	IP6 [10]	IP6 [9]	IP6 [8]	IP6 [7]	IP6 [6]	IP6 [5]	IP6 [4]	IP6 [3]	IP6 [2]	IP6 [1]	IP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Notes: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP6[1:0]	DU0_EXVSYNC_DU0_VSYNC	Reserved	Reserved	-	-	-	-	-
IP6[3:2]	DU0_EXODDF_DU0_ODDF_DISP_CDE	Reserved	Reserved	-	-	-	-	-
IP6[5:4]	DU0_DISP	Reserved	Reserved	-	-	-	-	-
IP6[7:6]	DU0_CDE	Reserved	Reserved	-	-	-	-	-
IP6[8]	VI0_CLK	AVB_RX_CLK	-	-	-	-	-	-
IP6[9]	VI0_DATA0_VI0_B0	AVB_RX_DV	-	-	-	-	-	-
IP6[10]	VI0_DATA1_VI0_B1	AVB_RXD0	-	-	-	-	-	-
IP6[11]	VI0_DATA2_VI0_B2	AVB_RXD1	-	-	-	-	-	-
IP6[12]	VI0_DATA3_VI0_B3	AVB_RXD2	-	-	-	-	-	-
IP6[13]	VI0_DATA4_VI0_B4	AVB_RXD3	-	-	-	-	-	-
IP6[14]	VI0_DATA5_VI0_B5	AVB_RXD4	-	-	-	-	-	-
IP6[15]	VI0_DATA6_VI0_B6	AVB_RXD5	-	-	-	-	-	-
IP6[16]	VI0_DATA7_VI0_B7	AVB_RXD6	-	-	-	-	-	-
IP6[19:17]	VI0_CLKENB	I2C3_SCL	SCIFA5_RXD_C	Reserved	AVB_RXD7	-	-	-
IP6[22:20]	VI0_FIELD	I2C3_SDA	SCIFA5_TXD_C	Reserved	AVB_RX_ER	-	-	-
IP6[25:23]	VI0_HSYNC_N	SCIF0_RXD_B	I2C0_SCL_C	Reserved	AVB_COL	-	-	-
IP6[28:26]	VI0_VSYNC_N	SCIF0_TXD_B	I2C0_SDA_C	AUDIO_CLKOUT_B	AVB_TX_EN	-	-	-
IP6[31:29]	ETH_MDIO	VI0_G0	MSIOF2_RXD_B	I2C5_SCL_D	AVB_TX_CLK	Reserved	Reserved	-

Legend: - Setting prohibited

5.3.16 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP7 [31]	IP7 [30]	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP7[2:0]	ETH_CRS_DV	VI0_G1	MSIOF2_TXD_B	I2C5_SDA_D	AVB_TXD0	Reserved	Reserved
IP7[5:3]	ETH_RX_ER	VI0_G2	MSIOF2_SCK_B	CAN0_RX_B	AVB_TXD1	Reserved	Reserved
IP7[8:6]	ETH_RXD0	VI0_G3	MSIOF2_SYNC_B	CAN0_TX_B	AVB_TXD2	Reserved	Reserved
IP7[11:9]	ETH_RXD1	VI0_G4	MSIOF2_SS1_B	SCIF4_RXD_D	AVB_TXD3	Reserved	-
IP7[14:12]	ETH_LINK	VI0_G5	MSIOF2_SS2_B	SCIF4_TXD_D	AVB_TXD4	Reserved	-
IP7[17:15]	ETH_REFCLK	VI0_G6	SCIF2_SCK_C	AVB_TXD5	SSI_SCK5_B	-	-
IP7[20:18]	ETH_TXD1	VI0_G7	SCIF2_RXD_C	IIC0_SCL_D	AVB_TXD6	SSI_WS5_B	-
IP7[23:21]	ETH_TX_EN	VI0_R0	SCIF2_TXD_C	IIC0_SDA_D	AVB_TXD7	SSI_SDATA5_B	-
IP7[26:24]	ETH_MAGIC	VI0_R1	SCIF3_SCK_B	AVB_TX_ER	SSI_SCK6_B	-	-
IP7[29:27]	ETH_TXD0	VI0_R2	SCIF3_RXD_B	I2C4_SCL_E	AVB_GTX_CLK	SSI_WS6_B	-
IP7[31]	DREQ0_N	SCIFB1_RXD	-	-	-	-	-

Legend: - Setting prohibited

5.3.19 Peripheral Function Select Register 10 (IPSR10)

Function: IPSR10 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP10 [31]	IP10 [30]	IP10 [29]	IP10 [28]	IP10 [27]	IP10 [26]	IP10 [25]	IP10 [24]	IP10 [23]	IP10 [22]	IP10 [21]	IP10 [20]	IP10 [19]	IP10 [18]	IP10 [17]	IP10 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP10 [15]	IP10 [14]	IP10 [13]	IP10 [12]	IP10 [11]	IP10 [10]	IP10 [9]	IP10 [8]	IP10 [7]	IP10 [6]	IP10 [5]	IP10 [4]	IP10 [3]	IP10 [2]	IP10 [1]	IP10 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP10[2:0]	SCIF1_RXD	I2C5_SCL	DU1_DG6	SSI_SCK2_B	Reserved	Reserved	-	-
IP10[5:3]	SCIF1_TXD	I2C5_SDA	DU1_DG7	SSI_WS2_B	Reserved	Reserved	-	-
IP10[8:6]	SCIF2_RXD	IIC0_SCL	DU1_DB0	SSI_SDATA2_B	Reserved	Reserved	Reserved	-
IP10[11:9]	SCIF2_TXD	IIC0_SDA	DU1_DB1	SSI_SCK9_B	Reserved	Reserved	Reserved	-
IP10[14:12]	SCIF2_SCK	IRQ1	DU1_DB2	SSI_WS9_B	Reserved	Reserved	Reserved	-
IP10[17:15]	SCIF3_SCK	IRQ2	Reserved	DU1_DB3	SSI_SDATA9_B	Reserved	Reserved	Reserved
IP10[20:18]	SCIF3_RXD	I2C1_SCL_E	Reserved	DU1_DB4	AUDIO_CLKA_C	SSI_SCK4_B	Reserved	Reserved
IP10[23:21]	SCIF3_TXD	I2C1_SDA_E	Reserved	DU1_DB5	AUDIO_CLKB_C	SSI_WS4_B	Reserved	Reserved
IP10[26:24]	I2C2_SCL	SCIFA5_RXD	DU1_DB6	AUDIO_CLKC_C	SSI_SDATA4_B	Reserved	-	-
IP10[29:27]	I2C2_SDA	SCIFA5_TXD	DU1_DB7	AUDIO_CLKOUT_C	Reserved	-	-	-
IP10[31:30]	SSI_SCK5	SCIFA3_SCK	DU1_DOTCLKIN	Reserved	-	-	-	-

Legend: - Setting prohibited

5.3.21 Peripheral Function Select Register 12 (IPSR12)

Function: IPSR12 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP12 [31]	IP12 [30]	IP12 [29]	IP12 [28]	IP12 [27]	IP12 [26]	IP12 [25]	IP12 [24]	IP12 [23]	IP12 [22]	IP12 [21]	IP12 [20]	IP12 [19]	IP12 [18]	IP12 [17]	IP12 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP12 [15]	IP12 [14]	IP12 [13]	IP12 [12]	IP12 [11]	IP12 [10]	IP12 [9]	IP12 [8]	IP12 [7]	IP12 [6]	IP12 [5]	IP12 [4]	IP12 [3]	IP12 [2]	IP12 [1]	IP12 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP12[2:0]	SSI_SCK34	MSIOF1_SYNC_B	SCIFA1_SCK_C	Reserved	Reserved	DREQ1_N_B	-
IP12[5:3]	SSI_WS34	MSIOF1_SS1_B	SCIFA1_RXD_C	Reserved	CAN1_RX_C	DACK1_B	-
IP12[8:6]	SSI_SDATA3	MSIOF1_SS2_B	SCIFA1_TXD_C	Reserved	CAN1_TX_C	DREQ2_N	-
IP12[10:9]	SSI_SCK4	Reserved	Reserved	Reserved	-	-	-
IP12[12:11]	SSI_WS4	Reserved	Reserved	Reserved	-	-	-
IP12[14:13]	SSI_SDATA4	Reserved	Reserved	Reserved	-	-	-
IP12[17:15]	SSI_SDATA8	SCIF1_SCK_B	PWM1_B	IRQ9	Reserved	DACK2	ETH_MDIO_B
IP12[20:18]	SSI_SCK1	SCIF1_RXD_B	IIC0_SCL_C	VI1_CLK	CAN0_RX_D	Reserved	ETH_CRS_DV_B
IP12[23:21]	SSI_WS1	SCIF1_TXD_B	IIC0_SDA_C	VI1_DATA0	CAN0_TX_D	Reserved	ETH_RX_ER_B
IP12[26:24]	SSI_SDATA1	HSCIF1_HRX_B	VI1_DATA1	Reserved	ATAWR0_N	ETH_RXD0_B	-
IP12[29:27]	SSI_SCK2	HSCIF1_HTX_B	VI1_DATA2	Reserved	ATAG0_N	ETH_RXD1_B	-

Legend: - Setting prohibited

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_msi2[0]	+ select pin A14 for function MSIOF2_RXD + select pin A15 for function MSIOF2_TXD + select pin A16 for function MSIOF2_SCK + select pin A17 for function MSIOF2_SYNC + select pin A18 for function MSIOF2_SS1 + select pin A19 for function MSIOF2_SS2	+ select pin ETH_CRS_DV for function MSIOF2_TXD_B + select pin ETH_LINK for function MSIOF2_SS2_B + select pin ETH_MDIO for function MSIOF2_RXD_B + select pin ETH_RXD0 for function MSIOF2_SYNC_B + select pin ETH_RXD1 for function MSIOF2_SS1_B + select pin ETH_RX_ER for function MSIOF2_SCK_B			
sel_rad[0]	+ select pin ETH_CRS_DV for function ADICS_SAMP + select pin ETH_LINK for function ADICHS2 + select pin ETH_MDIO for function ADIDATA + select pin ETH_RXD0 for function ADICHS0 + select pin ETH_RXD1 for function ADICHS1 + select pin ETH_RX_ER for function ADICLK	+ select pin SSI_SCK0129 for function ADIDATA_B + select pin SSI_SCK34 for function ADICHS0_B + select pin SSI_SDATA0 for function ADICLK_B + select pin SSI_SDATA3 for function ADICHS2_B + select pin SSI_WS0129 for function ADICS_SAMP_B + select pin SSI_WS34 for function ADICHS1_B			
sel_scifa0[1:0]	+ select pin MSIOF0_SS1 for function SCIFA0_RXD + select pin MSIOF0_SS2 for function SCIFA0_TXD	+ select pin A8 for function SCIFA0_RXD_B + select pin A9 for function SCIFA0_TXD_B	+ select pin DU0_DG0 for function SCIFA0_RXD_C + select pin DU0_DG1 for function SCIFA0_TXD_C	+ select pin SSI_SDATA2 for function SCIFA0_TXD_D + select pin SSI_WS2 for function SCIFA0_RXD_D	
sel_scifa1[1:0]	+ select pin D13 for function SCIFA1_SCK + select pin D14 for function SCIFA1_RXD + select pin D15 for function SCIFA1_TXD	+ select pin SSI_SCK6 for function SCIFA1_SCK_B + select pin SSI_SDATA6 for function SCIFA1_TXD_B + select pin SSI_WS6 for function SCIFA1_RXD_B	+ select pin SSI_SCK34 for function SCIFA1_SCK_C + select pin SSI_SDATA3 for function SCIFA1_TXD_C + select pin SSI_WS34 for function SCIFA1_RXD_C		
sel_scifa2[0]	+ select pin EX_CS3_N for function SCIFA2_SCK + select pin EX_CS4_N for function SCIFA2_RXD + select pin EX_CS5_N for function SCIFA2_TXD	+ select pin SSI_SCK78 for function SCIFA2_SCK_B + select pin SSI_SDATA7 for function SCIFA2_TXD_B + select pin SSI_WS78 for function SCIFA2_RXD_B			
sel_scifa3[0]	+ select pin SSI_SCK5 for function SCIFA3_SCK + select pin SSI_SDATA5 for function SCIFA3_TXD + select pin SSI_WS5 for function SCIFA3_RXD	+ select pin D0 for function SCIFA3_SCK_B + select pin D1 for function SCIFA3_RXD_B + select pin D2 for function SCIFA3_TXD_B			
sel_scifa4[1:0]	+ select pin HSCIF1_HCTS_N for function SCIFA4_RXD + select pin HSCIF1_HRTS_N for function SCIFA4_TXD	+ select pin A6 for function SCIFA4_RXD_B + select pin A7 for function SCIFA4_TXD_B	+ select pin DU0_DB0 for function SCIFA4_RXD_C + select pin DU0_DB1 for function SCIFA4_TXD_C	+ select pin AUDIO_CLKA for function SCIFA4_RXD_D + select pin AUDIO_CLKB for function SCIFA4_TXD_D	
sel_scifa5[1:0]	+ select pin I2C2_SCL for function SCIFA5_RXD + select pin I2C2_SDA for function SCIFA5_TXD	+ select pin A12 for function SCIFA5_RXD_B + select pin A13 for function SCIFA5_TXD_B	+ select pin VI0_CLKENB for function SCIFA5_RXD_C + select pin VI0_FIELD for function SCIFA5_TXD_C	+ select pin AUDIO_CLKC for function SCIFA5_RXD_D + select pin AUDIO_CLKOUT for function SCIFA5_TXD_D	
sel_tmu[0]	+ select pin D7 for function TCLK1 + select pin SCIF1_SCK for function TCLK2	+ select pin D13 for function TCLK2_B + select pin I2C0_SCL for function TCLK1_B			
sel_can0[1:0]	+ select pin SD1_CD for function CAN0_RX + select pin SD1_WP for function CAN0_TX	+ select pin ETH_RXD0 for function CAN0_TX_B + select pin ETH_RX_ER for function CAN0_RX_B	+ select pin DU0_DB0 for function CAN0_RX_C + select pin DU0_DB1 for function CAN0_TX_C	+ select pin SSI_SCK1 for function CAN0_RX_D + select pin SSI_WS1 for function CAN0_TX_D	
sel_can1[1:0]	+ select pin MMC_D6 for function CAN1_RX + select pin MMC_D7 for function CAN1_TX	+ select pin A17 for function CAN1_RX_B + select pin A18 for function CAN1_TX_B	+ select pin SSI_SDATA3 for function CAN1_TX_C + select pin SSI_WS34 for function CAN1_RX_C	+ select pin I2C0_SCL for function CAN1_RX_D + select pin I2C0_SDA for function CAN1_TX_D	
sel_hscif0[0]	+ select pin HSCIF0_HRX for function HRX0 + select pin HSCIF0_HSCK for function HSCK0 + select pin HSCIF0_HTX for function HTX0	+ select pin A14 for function HRX0_B + select pin A15 for function HTX0_B + select pin A16 for function HSCK0_B			

5.3.29 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR3 [31]	PUPR3 [30]	PUPR3 [29]	PUPR3 [28]	PUPR3 [27]	PUPR3 [26]	PUPR3 [25]	PUPR3 [24]	PUPR3 [23]	PUPR3 [22]	PUPR3 [21]	PUPR3 [20]	PUPR3 [19]	PUPR3 [18]	PUPR3 [17]	PUPR3 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR3 [15]	PUPR3 [14]	PUPR3 [13]	PUPR3 [12]	PUPR3 [11]	PUPR3 [10]	PUPR3 [9]	PUPR3 [8]	PUPR3 [7]	PUPR3 [6]	PUPR3 [5]	PUPR3 [4]	PUPR3 [3]	PUPR3 [2]	PUPR3 [1]	PUPR3 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR3[31:0]	H'FFFF FFFF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR3[31]	I2C1_SDA is pull up
PUPR3[30]	I2C1_SCL is pull up
PUPR3[29]	I2C0_SDA is pull up
PUPR3[28]	I2C0_SCL is pull up
PUPR3[27]	HSCIF0_HSCK is pull up
PUPR3[26]	HSCIF0_HRTS_N is pull up
PUPR3[25]	HSCIF0_HCTS_N is pull up
PUPR3[24]	HSCIF0_HTX is pull up
PUPR3[23]	HSCIF0_HRX is pull up
PUPR3[22]	ETH_MDC is pull up
PUPR3[21]	ETH_TXD0 is pull up
PUPR3[20]	ETH_MAGIC is pull up
PUPR3[19]	ETH_TX_EN is pull up
PUPR3[18]	ETH_TXD1 is pull up
PUPR3[17]	ETH_REF_CLK is pull up
PUPR3[16]	ETH_LINK is pull up
PUPR3[15]	ETH_RXD1 is pull up
PUPR3[14]	ETH_RXD0 is pull up
PUPR3[13]	ETH_RX_ER is pull up
PUPR3[12]	ETH_CRS_DV is pull up
PUPR3[11]	ETH_MDIO is pull up
PUPR3[10]	VI0_VSYNC_N is pull up
PUPR3[9]	VI0_HSYNC_N is pull up
PUPR3[8]	VI0_FIELD is pull up
PUPR3[7]	VI0_CLKENB is pull up

5.3.32 LSI Pin Pull-Up Control Register 6 (PUPR6)

Function: PUPR6 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR6 [31]	PUPR6 [30]	PUPR6 [29]	PUPR6 [28]	PUPR6 [27]	PUPR6 [26]	PUPR6 [25]	PUPR6 [24]	PUPR6 [23]	PUPR6 [22]	PUPR6 [21]	PUPR6 [20]	PUPR6 [19]	PUPR6 [18]	PUPR6 [17]	PUPR6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR6 [15]	PUPR6 [14]	PUPR6 [13]	PUPR6 [12]	PUPR6 [11]	PUPR6 [10]	PUPR6 [9]	PUPR6 [8]	PUPR6 [7]	PUPR6 [6]	PUPR6 [5]	PUPR6 [4]	PUPR6 [3]	PUPR6 [2]	PUPR6 [1]	PUPR6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

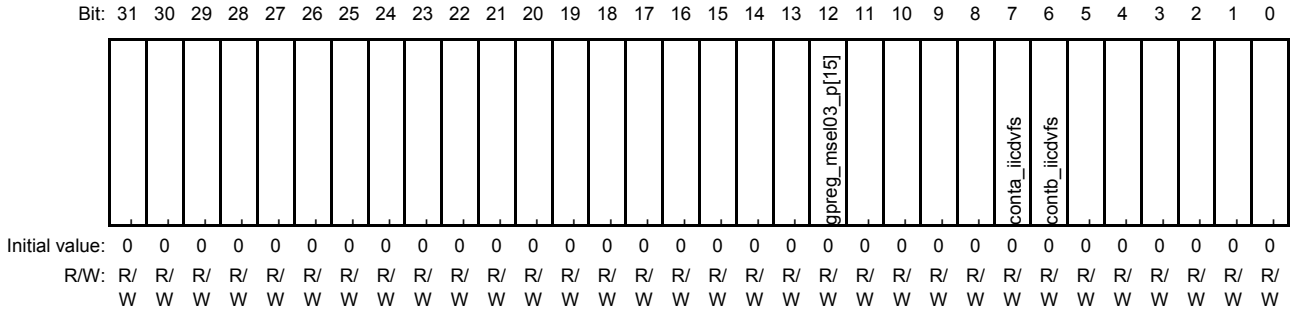
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR6[31:0]	H'0000 0000	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR6[31]	-
PUPR6[30]	-
PUPR6[29]	-
PUPR6[28]	-
PUPR6[27]	-
PUPR6[26]	-
PUPR6[25]	-
PUPR6[24]	-
PUPR6[23]	MMC_D7 is pull up
PUPR6[22]	MMC_D6 is pull up
PUPR6[21]	MMC_D5 is pull up
PUPR6[20]	MMC_D4 is pull up
PUPR6[19]	MMC_D3 is pull up
PUPR6[18]	MMC_D2 is pull up
PUPR6[17]	MMC_D1 is pull up
PUPR6[16]	MMC_D0 is pull up
PUPR6[15]	MMC_CMD is pull up
PUPR6[14]	-
PUPR6[13]	SD1_WP is pull up
PUPR6[12]	SD1_CD is pull up
PUPR6[11]	SD1_DATA3 is pull up
PUPR6[10]	SD1_DATA2 is pull up
PUPR6[9]	SD1_DATA1 is pull up
PUPR6[8]	SD1_DATA0 is pull up
PUPR6[7]	SD1_CMD is pull up

Bit Name	Set Value = 1
PUPR6[6]	SD0_WP is pull up
PUPR6[5]	SD0_CD is pull up
PUPR6[4]	SD0_DATA3 is pull up
PUPR6[3]	SD0_DATA2 is pull up
PUPR6[2]	SD0_DATA1 is pull up
PUPR6[1]	SD0_DATA0 is pull up
PUPR6[0]	SD0_CMD is pull up

5.3.37 IICDVFS and TDBG IO cell control register (IOCTRL7)

Function: IOCTRL7 controls the driving abilities of pins in use for the IIC and IICDVFS interfaces. This register is internal use and reserved; the value of this register should not be changed.



Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R/W	—
12	gpreg_msel03_p [15]	0	R/W	Debug monitor function: 0: Use DU pins for debug monitor function. 1: Use SDHI pins for debug monitor function.
11 to 8	—	All 0	R/W	—
7	conta_iicdvfs	0	R/W	Control TOF value of IICDVFS IO cell (TOF: Output fall time from VIH min to VIL max OR from 0.7VPU to 0.3VPU) 0: 0.3VPU 1: 0.7VPU
6	contb_iicdvfs	0	R/W	Control VIH/VIL value of IICDVFS IO cell (VIH: High level input voltage ; VIL: Low level input voltage) 0: VIL 1: VIH
5 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.