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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1154agk-gak-ax

1.3.4 Internal Bus Module

Item	Description
AXI-bus	• On-chip main bus — Bus protocol : AXI3 with QoS control — Frequency: 260 MHz — Bus width: 256 bits/128 bits • On-chip CPU & GPU main bus — Corelink™ CCI-400 Cache Coherent Interconnect - r0p3 — Bus protocol: AMBA®4 ACE™ and ACE-Lite™ — Frequency: 520 MHz — Bus width: 128 bits
Direct memory access controller (SYS-DMAC)	• 30 channels for ARM domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller (Audio-DMAC)	• 13 channels for Audio domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)

Item	Description	
Video input (VIN)	Input data format	• 8-, 10-, or 12-bit YCbCr422 (CbYCrY format) • 16-bit YCbCr422 (8 bits (Y) + 8 bits (CbCr) format) • 20-bit YCbCr422 (10 bits (Y) + 10 bits (CbCr) format) • 24-bit YCbCr422 (12 bits (Y) + 12 bits (CbCr) format) • 18-bit RGB666 • 24-bit RGB888
	Clipping function	Up to 2048 × 2048
	Horizontal scaling	Uses a 9-tap multi-phase filter. Up to two times, but only scaling down is possible for HD1080i or HD720P data.
	Vertical scaling	Scaling by linear interpolation Up to three times, but only scaling down is possible for HD1080i or HD720P data.
	Output format	RGB-565, ARGB-1555, YCbCr422, RGB888 (channel 0,1), YC separation, and extraction of the Y component

1.3.10 Network

Item	Description
CAN interface (CAN)	• 2 channels • Supports CAN specification 2.0B • ISO-11898-1 compliant • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
Ethernet AVB	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)
Ethernet MAC	• IEEE802.3u MAC (Ether) function • Supports transfer at 10 and 100 Mbps • Flow control conforming to IEEE802.3x or back pressure system • Supports interface conforming to IEEE802.3u • Magic packet detection • Includes DMAC • Supports RMII (Reduced Media Independent Interface)

1.3.11 Timer

Item	Description
Watchdog timer (WDT)	• Single channel • Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable
Timer pulse unit (TPU)	• 4-channels • 16-bit timers • Each channel outputs PWM

Item	Description
Compare match timer 0 (CMT0)	• Two channels • 32-bit timer (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare match timer 1 (CMT1)	• Eight channels • 48-bit timer (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Timer unit (TMU)	• 4 sets of 3-channel 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • 2 channels for input capture

Item	Description
Clock-synchronized serial interface with FIFO (MSIOF)	• 3 channels • Max. speed: 26 Mbps • Internal 64-Byte transmit FIFOs/internal 256-Byte receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
Quad-SPI (QSPI)	• Single/Dual/Quad-SPI: serial slave transfer enabled • Supports master mode • SPCLK clock rate: 1…4080 in master mode; Max. 78 MHz
High-speed serial communication interface with FIFO (HSCIF)	• 3 channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS and HCTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM timer (PWM)	• 7 channels • High-level width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1024 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
Boot Function (BOOT)	• System startup with selectable boot mode at power-on reset • Program downloaded to internal memory (LRAM) • Autorun function for the downloaded program

4. Pin Multiplexing

4.1 List of Multiplexed Pin Functions

Table 4.1 lists the multiplexed pin functions of the RZ/G1E.

The default pin function of each pin after power-on reset is "Function 1" respectively, unless otherwise mentioned.

For details on pin function control, refer to section 3.3, Mode Pin Settings and section 5, Pin Function Controller (PFC).

[Legend]

- Leftmost column of table
  No.: Serial number
  Pin No.: BGA package ball grid number
  Mode Pin (only for corresponding pin): Mode pin is assigned

- Middle column of table
  Function n (n=1, 2, 3, ...)/GPIO: Module or GPIO
  Module: Module abbreviation except for GPIO
  Pin Name: Module or GPIO pin name
  I/O: Input or output,
  i.e., I: Input, I(S): Schmitt input, IO: Input and output, IO (OD): Input and open drain output, O: Output, P: Power supply pin. (I)/(H)/(L)/(X)/(Z) with I, O or IO: Default pin state (only for default pin, except for clock or analog output), H: High level output, L: Low level output, X: Undefined value output, Z: High impedance

"Reserved" in module column is assigned optional function and "-" in module column is internal function or undefined, they must not be specified. This indication is different from that of in section 5, Pin Function Controller (PFC).

- Rightmost column of table
  During POR: Pin state during power-on reset (PRESET# pin input is low-level)
  V(power)/|IOH|: Pin voltage (power domain) and output drive current (nominal value respectively)
  Pull-up: Internal pull-up control function is available or not from a power-on reset
  "On": Pull-up control function is available and default state is pulled-up.
  (No.110, ACK pin is available for internal pull-down function.)
  "Off": Pull-up control function is available and default state is not pulled-up.
  "-": Pull-up control function is not available.
  For details of pull-up control function, refer to PUPR0 through PUPR6 registers in section 5, Pin Function Controller (PFC).

Notes: 1. Pin name that has an identifier for example "XXXX_B", "XXXX_C" etc. are mirror pins of the XXXX pin. Only one pin out of the XXXX pin or its mirror pins can be used. When using mirror pin, specify the suite of pin that has the same identifier for the selected module. It is prohibited to use a suite of pin as mixed two or more identifiers for a selected module.
2. Do not use any pins that of unused modules.
3. Unused pins must be handled as described in section 4.3, Handling of Unused Pins.
4. The terminal state after the reset cancellation has been described as a premise not using the BKPRST (BKRST#=H(fixed)).

LBSC, SCIFB, PWM, TPU, SCIFA, MSIOF, IIC, HSCIF, RCAN, QSPI and GPIO (No.177 to 196): Up to 8-Function Multiplexed and Mode Pin assigned (No.177, 180, 182, 186, 188, 191 and 192)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.
When MD[3:1]=000, the LBSC will execute area 0 booting; MD[3:1]≠000, the QSPI will execute QSPI booting.

Function	1	2	3	4	5	6	7	GPIO	
MD[3:1]	=000							≠000	
No.									During POR
Pin No.									V(power)/|IOH|
Mode Pin									Pull-up
177	LBSC	SCIFB0	-	-	-	-	-		I(Mode Pin)
H4	A4	SCIFB0_TXD	-	-	-	-	-	GP0_20	3.3V(VCCQ)/8mA
MD1	O(L)	O	-	-	-	-	-	IO(I)	Off
178	LBSC	SCIFB0	PWM4	TPU	-	-	-		I(GPIO)
F2	A5	SCIFB0_RXD	PWM4_B	TPUTO3_C	-	-	-	GP0_21	3.3V(VCCQ)/8mA
	O(L)	I	O	O	-	-	-	IO(I)	On
179	LBSC	SCIFB0	SCIFA4	TPU	-	-	-		I(GPIO)
G5	A6	SCIFB0_CTS#	SCIFA4_RXD_B	TPUTO2_C	-	-	-	GP0_22	3.3V(VCCQ)/8mA
	O(L)	I	I	O	-	-	-	IO(I)	On
180	LBSC	SCIFB0	SCIFA4	-	-	-	-		I(Mode Pin)
F1	A7	SCIFB0_RTS#	SCIFA4_TXD_B	-	-	-	-	GP0_23	3.3V(VCCQ)/8mA
MD4	O(L)	O	O	-	-	-	-	IO(I)	Off
181	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(GPIO)
J5	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	GP0_24	3.3V(VCCQ)/8mA
	O(L)	I	I	-	-	-	-	IO(I)	On
182	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(Mode Pin)
G2	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	GP0_25	3.3V(VCCQ)/8mA
MD5	O(L)	O	O	-	-	-	-	IO(I)	Off
183	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
J4	A10	MSIOF1_SCK	IIC0_SCL_B	-	-	-	-	GP0_26	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
184	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
H3	A11	MSIOF1_SYNC	IIC0_SDA_B	-	-	-	-	GP0_27	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
185	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(GPIO)
G3	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	GP0_28	3.3V(VCCQ)/8mA
	O(L)	O	I	-	-	-	-	IO(I)	On
186	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(Mode Pin)
G1	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	GP0_29	3.3V(VCCQ)/8mA
MD6	O(L)	O	O	-	-	-	-	IO(I)	Off
187	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(GPIO)
K5	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1#	-	-	-	GP0_30	3.3V(VCCQ)/8mA
	O(L)	I	I	I	-	-	-	IO(I)	On
188	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(Mode Pin)
H1	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	GP0_31	3.3V(VCCQ)/8mA
MD7	O(L)	O	O	O	-	-	-	IO(I)	Off
189	LBSC	MSIOF2	HSCIF0	Reserved	Reserved	RCAN	TPU		I(GPIO)
J2	A16	MSIOF2_SCK	HSCIF0_HSCK_B	-	-	CAN_CLK_C	TPUTO2_B	GP1_0	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	I	O	IO(I)	On
190	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(GPIO)
K4	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	-	-	-	GP1_1	3.3V(VCCQ)/8mA
	O(L)	IO	I	I	-	-	-	IO(I)	On
191	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(Mode Pin)
H2	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	-	-	-	GP1_2	3.3V(VCCQ)/8mA
MDT0	O(L)	O	O	O	-	-	-	IO(I)	Off
192	LBSC	MSIOF2	PWM4	TPU	Reserved	-	-		I(Mode Pin)
K3	A19	MSIOF2_SS2	PWM4	TPUTO2	-	-	-	GP1_3	3.3V(VCCQ)/8mA
MD18	O(L)	O	O	O	-	-	-	IO(I)	Off
193	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K2	A20	SPCLK	-	-	-	-	-	GP1_4	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
194	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K1	A21	MOSI/IO0	-	-	-	-	-	GP1_5	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
195	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
L3	A22	MISO/IO1	-	ATADIR1#	-	-	-	GP1_6	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On
196	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
J3	A23	IO2	-	ATAWR1#	-	-	-	GP1_7	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On

VIN, I2C, SCIFA, EthernetAVB, ADG, EtherMAC, MSIOF, RCAN, SCIF, IIC, SSI, HSCIF and GPIO (No.257 to 277): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	GPIO	
No.									During POR
Pin No.									V(power)/|IOH|
									Pull-up
257	VIN0	I2C3	SCIFA5	Reserved	EthernetAVB	-	-		I(GPIO)
AA1	VI0_CLKENB	I2C3_SCL	SCIFA5_RXD_C	-	AVB_RXD7	-	-	GP3_9	3.3V(VCCQ)/4mA
	I	IO	I	-	I	-	-	IO(I)	On
258	VIN0	I2C3	SCIFA5	Reserved	EthernetAVB	-	-		I(GPIO)
W2	VI0_FIELD	I2C3_SDA	SCIFA5_TXD_C	-	AVB_RX_ER	-	-	GP3_10	3.3V(VCCQ)/4mA
	I	IO	O	-	I	-	-	IO(I)	On
259	VIN0	SCIF0	I2C0	Reserved	EthernetAVB	-	-		I(GPIO)
Y1	VI0_HSYNC#	SCIF0_RXD_B	I2C0_SCL_C	-	AVB_COL	-	-	GP3_11	3.3V(VCCQ)/4mA
	I	I	IO	-	I	-	-	IO(I)	On
260	VIN0	SCIF0	I2C0	ADG	EthernetAVB	-	-		I(GPIO)
W1	VI0_VSYNC#	SCIF0_TXD_B	I2C0_SDA_C	AUDIO_CLKOUT_B	AVB_TX_EN	-	-	GP3_12	3.3V(VCCQ)/8mA
	I	O	IO	O	O	-	-	IO(I)	On
261	EtherMAC	VIN0	MSIOF2	I2C5	EthernetAVB	Reserved	Reserved		I(GPIO)
T5	ETH_MDIO	VI0_G0	MSIOF2_RXD_B	I2C5_SCL_D	AVB_TX_CLK	-	-	GP3_13	3.3V(VCCQ)/4mA
	IO	I	I	IO	I	-	-	IO(I)	On
262	EtherMAC	VIN0	MSIOF2	I2C5	EthernetAVB	Reserved	Reserved		I(GPIO)
V4	ETH_CRS_DV	VI0_G1	MSIOF2_TXD_B	I2C5_SDA_D	AVB_TXD0	-	-	GP3_14	3.3V(VCCQ)/8mA
	I	I	O	IO	O	-	-	IO(I)	On
263	EtherMAC	VIN0	MSIOF2	RCAN0	EthernetAVB	Reserved	Reserved		I(GPIO)
U5	ETH_RX_ER	VI0_G2	MSIOF2_SCK_B	CAN0_RX_B	AVB_TXD1	-	-	GP3_15	3.3V(VCCQ)/8mA
	I	I	IO	I	O	-	-	IO(I)	On
264	EtherMAC	VIN0	MSIOF2	RCAN0	EthernetAVB	Reserved	Reserved		I(GPIO)
V3	ETH_RXD0	VI0_G3	MSIOF2_SYNC_B	CAN0_TX_B	AVB_TXD2	-	-	GP3_16	3.3V(VCCQ)/8mA
	I	I	IO	O	O	-	-	IO(I)	On
265	EtherMAC	VIN0	MSIOF2	SCIF4	EthernetAVB	Reserved	-		I(GPIO)
U4	ETH_RXD1	VI0_G4	MSIOF2_SS1_B	SCIF4_RXD_D	AVB_TXD3	-	-	GP3_17	3.3V(VCCQ)/8mA
	I	I	O	I	O	-	-	IO(I)	On
266	EtherMAC	VIN0	MSIOF2	SCIF4	EthernetAVB	Reserved	-		I(GPIO)
V5	ETH_LINK	VI0_G5	MSIOF2_SS2_B	SCIF4_TXD_D	AVB_TXD4	-	-	GP3_18	3.3V(VCCQ)/8mA
	I	I	O	O	O	-	-	IO(I)	On
267	EtherMAC	VIN0	SCIF2	EthernetAVB	SSI	-	-		I(GPIO)
V1	ETH_REF_CLK	VI0_G6	SCIF2_SCK_C	AVB_TXD5	SSI_SCK5_B	-	-	GP3_19	3.3V(VCCQ)/8mA
	I	I	IO	O	IO	-	-	IO(I)	On
268	EtherMAC	VIN0	SCIF2	IIC0 (I2C6)	EthernetAVB	SSI	-		I(GPIO)
V2	ETH_TXD1	VI0_G7	SCIF2_RXD_C	IIC0_SCL_D	AVB_TXD6	SSI_WS5_B	-	GP3_20	3.3V(VCCQ)/8mA
	O	I	I	IO	O	IO	-	IO(I)	On
269	EtherMAC	VIN0	SCIF2	IIC0 (I2C6)	EthernetAVB	SSI	-		I(GPIO)
U3	ETH_TX_EN	VI0_R0	SCIF2_TXD_C	IIC0_SDA_D	AVB_TXD7	SSI_SDATA5_B	-	GP3_21	3.3V(VCCQ)/8mA
	O	I	O	IO	O	IO	-	IO(I)	On
270	EtherMAC	VIN0	SCIF3	EthernetAVB	SSI	-	-		I(GPIO)
W4	ETH_MAGIC	VI0_R1	SCIF3_SCK_B	AVB_TX_ER	SSI_SCK6_B	-	-	GP3_22	3.3V(VCCQ)/8mA
	O	I	IO	O	IO	-	-	IO(I)	On
271	EtherMAC	VIN0	SCIF3	I2C4	EthernetAVB	SSI	-		I(GPIO)
U2	ETH_TXD0	VI0_R2	SCIF3_RXD_B	I2C4_SCL_E	AVB_GTX_CLK	SSI_WS6_B	-	GP3_23	3.3V(VCCQ)/8mA
	O	I	I	IO	O	IO	-	IO(I)	On
272	EtherMAC	VIN0	SCIF3	I2C4	EthernetAVB	SSI	-		I(GPIO)
W5	ETH_MDC	VI0_R3	SCIF3_TXD_B	I2C4_SDA_E	AVB_MDC	SSI_SDATA6_B	-	GP3_24	3.3V(VCCQ)/8mA
	O	I	O	IO	O	IO	-	IO(I)	On
273	HSCIF0	VIN0	I2C1	ADG	EthernetAVB	SSI	-		I(GPIO)
U1	HSCIF0_HRX	VI0_R4	I2C1_SCL_C	AUDIO_CLKA_B	AVB_MDIO	SSI_SCK78_B	-	GP3_25	3.3V(VCCQ)/8mA
	I	I	IO	I	IO	IO	-	IO(I)	On
274	HSCIF0	VIN0	I2C1	ADG	EthernetAVB	SSI	-		I(GPIO)
T4	HSCIF0_HTX	VI0_R5	I2C1_SDA_C	AUDIO_CLKB_B	AVB_LINK	SSI_WS78_B	-	GP3_26	3.3V(VCCQ)/8mA
	O	I	IO	I	I	IO	-	IO(I)	On
275	HSCIF0	VIN0	SCIF0	I2C0	EthernetAVB	SSI	-		I(GPIO)
T3	HSCIF0_HCTS#	VI0_R6	SCIF0_RXD_D	I2C0_SCL_E	AVB_MAGIC	SSI_SDATA7_B	-	GP3_27	3.3V(VCCQ)/8mA
	IO	I	I	IO	O	IO	-	IO(I)	On
276	HSCIF0	VIN0	SCIF0	I2C0	EthernetAVB	SSI	-		I(GPIO)
T2	HSCIF0_HRTS#	VI0_R7	SCIF0_TXD_D	I2C0_SDA_E	AVB_PHY_INT	SSI_SDATA8_B	-	GP3_28	3.3V(VCCQ)/8mA
	IO	I	O	IO	I	IO	-	IO(I)	On
277	HSCIF0	SCIF	EthernetAVB	ADG	-	-	-		I(GPIO)
T1	HSCIF0_HSCK	SCIF_CLK_B	AVB_CRS	AUDIO_CLKC_B	-	-	-	GP3_29	3.3V(VCCQ)/8mA
	IO	I	I	I	-	-	-	IO(I)	On

ADG, I2C, SCIFA, VIN, EtherMAC, IIC and GPIO (No.335 to 340): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset except for No.339 and 340. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	GPIO	
No.										During POR
Pin No.										V(power)/|IOH|
										Pull-up
335	ADG	I2C0	SCIFA4	VIN1	Reserved	Reserved	EtherMAC	-		I(GPIO)
AD1	AUDIO_CLKA	I2C0_SCL_B	SCIFA4_RXD_D	VI1_CLKENB	-	-	ETH_TXD0_B	-	GP5_20	3.3V(VCCQ)/8mA
	I	IO	I	I	-	-	O	-	IO(I)	On
336	ADG	I2C0	SCIFA4	VIN1	Reserved	Reserved	Reserved	EtherMAC		I(GPIO)
AE2	AUDIO_CLKB	I2C0_SDA_B	SCIFA4_TXD_D	VI1_FIELD	-	-	-	ETH_MDC_B	GP5_21	3.3V(VCCQ)/8mA
	I	IO	O	I	-	-	-	O	IO(I)	On
337	ADG	I2C4	SCIFA5	VIN1	Reserved	Reserved	Reserved	Reserved		I(GPIO)
AC1	AUDIO_CLKC	I2C4_SCL_B	SCIFA5_RXD_D	VI1_HSYNC#	-	-	-	-	GP5_22	3.3V(VCCQ)/8mA
	I	IO	I	I	-	-	-	-	IO(I)	On
338	ADG	I2C4	SCIFA5	VIN1	Reserved	Reserved	Reserved	Reserved		I(GPIO)
AC2	AUDIO_CLKOUT	I2C4_SDA_B	SCIFA5_TXD_D	VI1_VSYNC#	-	-	-	-	GP5_23	3.3V(VCCQ)/8mA
	O	IO	O	I	-	-	-	-	IO(I)	On
339	IIC1	-	-	-	-	-	-	-	-	Z
W21	IIC1_SCL	-	-	-	-	-	-	-	-	1.8V(VCCQ18)*/-
	IO(OD, Z)	-	-	-	-	-	-	-	-	-
340	IIC1	-	-	-	-	-	-	-	-	Z
V22	IIC1_SDA	-	-	-	-	-	-	-	-	1.8V(VCCQ18)*/-
	IO(OD, Z)	-	-	-	-	-	-	-	-	-

Note: No.339 and 340 (IIC1_SCL and IIC1_SDA) pin voltage: Input/output 3.3V tolerant pins
When using these pins as 3.3 V tolerant, all the external pull-up power supply for these pins must be kept the same power on/off sequence as the VCCQ of this LSI.

- End of Table 4.1 -

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
99	K16/L16	VSS_CPGPLL1	-	P	-	P	-
100	K12/L12	VDD_CPGPLL3	-	P	-	P	-
101	K11/L11	VSS_CPGPLL3	-	P	-	P	-
102	V23	PRESET#	I	I(L)	PRESET#	I	-
103	B6	PRESETOUT#	O	L	PRESETOUT#	L to H	-
104	R21	BSMODE	I	I	BSMODE	I	-
105	N21	TRST#	I	I(L)	TRST#	I	On
106	N22	TCK	I	I	TCK	I	On
107	P21	TMS	I	I	TMS	I	On
108	R22	TDI	I	I	TDI	I	On
109	P22	TDO	O	Z	TDO	Z	-
110	U23	ACK	IO	I	ACK	I	On(pulldown)
111	T25	USB_EXTAL	I	I	USB_EXTAL	I	-
112	T24	USB_XTAL	O	O	USB_XTAL	O	-
113	P20	VD331	-	P	-	P	-
114	R20	VD181	-	P	-	P	-
115	P23	AVDD	-	P	-	P	-
116	M20	AVSS	-	P	-	P	-
117	P24	USB0_DP	IO	I	USB0_DP	I	-
118	P25	USB0_DM	IO	I	USB0_DM	I	-
119	M25	USB0_RREF	-	P	-	P	-
120	U21	USB0_PWEN	O	Z	USB0_PWEN	L	-
121	U22	USB0_OVC	I	I	USB0_OVC	I	-
122	N24	USB1_DP	IO	I	USB1_DP	I	-
123	N25	USB1_DM	IO	I	USB1_DM	I	-
124	M24	USB1_RREF	-	P	-	P	-
125	T21	USB1_PWEN	O	Z	USB1_PWEN	L	-
126	T22	USB1_OVC	I	I	USB1_OVC	I	-
127	R23	NMI	I	I	NMI	I	-
128	AE12	SD0_CLK	O	I	GP6_0	I	-
129	AD12	SD0_CMD	IO	I	GP6_1	I	Off
130	AC11	SD0_DATA0	IO	I	GP6_2	I	Off
131	AD11	SD0_DATA1	IO	I	GP6_3	I	Off
132	AE11	SD0_DATA2	IO	I	GP6_4	I	Off
133	AA12	SD0_DATA3	IO	I	GP6_5	I	Off
134	AB12	SD0_CD	I	I	GP6_6	I	Off
135	AA13	SD0_WP	I	I	GP6_7	I	Off
136	AC12	VCCQ_SD0	-	P	-	P	-
137	AE8	SD1_CLK	O	I/Z(*2)	GP6_8/TDO2(*2)	I/Z(*2)	-
138	AA8	SD1_CMD	IO	I	GP6_9/TRST2#(*2)	I	Off/-(*3)
139	AD7	SD1_DATA0	IO	I	GP6_10/TCK2(*2)	I	Off/-(*3)
140	AE7	SD1_DATA1	IO	I	GP6_11/TMS2(*2)	I	Off/-(*3)
141	AB8	SD1_DATA2	IO	I	GP6_12/TDI2(*2)	I	Off/-(*3)
142	AC8	SD1_DATA3	IO	I	GP6_13(*2)	I	Off/-(*3)
143	AD8	SD1_CD	I	I	GP6_14	I	Off
144	AE9	SD1_WP	I	I	GP6_15	I	Off
145	AC7	VCCQ_SD1	-	P	-	P	-
146	AE10	MMC_CLK	O	I/Z(*2)	GP6_16/TDO3(*2)	I/Z(*2)	-
147	AD9	MMC_CMD	IO	I	GP6_17/TRST3#(*2)	I	Off/-(*3)
148	AA9	MMC_D0	IO	I	GP6_18/TCK3(*2)	I	Off/-(*3)

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
199	B1	CLKOUT	O	O	CLKOUT	O	-
200	E2	CS0#	O	I	CS0#/GP1_10(*4)	H/I	On
201	M5	CS1#/A26	O	I	[CS1#/A26]/GP1_11	[H/L] (*5)/I	On
202	E1	EX_CS0#	O	I	GP1_12	I	On
203	E3	EX_CS1#	O	I	GP1_13	I	On
204	D1	EX_CS2#	O	I	GP1_14	I	On
205	D2	EX_CS3#	O	I	GP1_15	I	On
206	C1	EX_CS4#	O	I	GP1_16	I	On
207	B2	EX_CS5#	O	I	GP1_17	I	On
208	M4	BS#	O	I(MD8)	BS#/GP1_18(*4)	H/I	Off
209	M3	RD#	O	I(MD14)	RD#GP1_19(*4)	H/I	Off
210	M1	RD/WR#	O	I(MD9)	GP1_20	I	Off
211	L1	WE0#	O	I(MD19)	WE0#/ GP1_21(*4)	H/I	Off
212	L4	WE1#	O	I(MD20)	WE1#/ GP1_22(*4)	H/I	Off
213	C2	EX_WAIT0	I	I	EX_WAIT0/ GP1_23(*4)	I/I	On
214	L5	DREQ0#	I	I	GP1_24	I	On
215	M2	DACK0	O	I(MD21)	GP1_25	I	Off
216	AA18	DU0_DR0	O	I	GP2_0	I	On
217	AB18	DU0_DR1	O	I	GP2_1	I	On
218	AE19	DU0_DR2	O	I	GP2_2	I	On
219	AC18	DU0_DR3	O	I	GP2_3	I	On
220	AD19	DU0_DR4	O	I	GP2_4	I	On
221	AD17	DU0_DR5	O	I	GP2_5	I	On
222	AC17	DU0_DR6	O	I	GP2_6	I	On
223	AC19	DU0_DR7	O	I	GP2_7	I	On
224	AA17	DU0_DG0	O	I	GP2_8	I	On
225	AB16	DU0_DG1	O	I	GP2_9	I	On
226	AD18	DU0_DG2	O	I	GP2_10	I	On
227	AD16	DU0_DG3	O	I	GP2_11	I	On
228	AB17	DU0_DG4	O	I	GP2_12	I	On
229	AA16	DU0_DG5	O	I	GP2_13	I	On
230	AE16	DU0_DG6	O	I	GP2_14	I	On
231	AC16	DU0_DG7	O	I	GP2_15	I	On
232	AC14	DU0_DB0	O	I	GP2_16	I	On
233	AE17	DU0_DB1	O	I	GP2_17	I	On
234	AA15	DU0_DB2	O	I	GP2_18	I	On
235	AB15	DU0_DB3	O	I	GP2_19	I	On
236	AD14	DU0_DB4	O	I	GP2_20	I	On
237	AD15	DU0_DB5	O	I	GP2_21	I	On
238	AA14	DU0_DB6	O	I	GP2_22	I	On
239	AC15	DU0_DB7	O	I	GP2_23	I	On
240	AE15	DU0_DOTCLKIN	I	I	GP2_24	I	On
241	AE14	DU0_DOTCLKOUT0	O	I	GP2_25	I	On
242	AE13	DU0_DOTCLKOUT1	O	I	GP2_26	I	On
243	AD13	DU0_EXHSYNC/DU0_HSYNC	IO	I(MD11)	GP2_27	I	Off
244	AB14	DU0_EXVSYNC/DU0_VSYNC	IO	I(MD12)	GP2_28	I	Off
245	AC13	DU0_EXODDF/DU0_ODDF/DISP/CDE	IO	I	GP2_29	I	On
246	AE18	DU0_DISP	O	I(MD10)	GP2_30	I	Off
247	AB13	DU0_CDE	O	I(MD13)	GP2_31	I	Off
248	AB1	VI0_CLK	I	I	GP3_0	I	On

4.3 Handling of Unused Pins

Table 4.3 shows a handling of unused pins of the RZ/G1E.

"Unused pin" means all modules that are multiplexed to the pin should be disable and unused in this section. For handling of some unused pin which belongs to the enable module should be handled following the notification of the module manual. Unless otherwise specified in the module manual, follow the Table 4.3 for handling of unused pins.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin multiplex table, Default State: Pin state of default pin function (function 1, GPIO or DBG).

Mode Pin: Mode pin assigned.

Boot: These pins will be used in boot operation (LBSC area 0 or QSPI).

Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.

"On": Pull-up control function is available and default state is pulled-up.

(No.110, ACK pin is available internal pull-down function.)

"Off": Pull-up control function is available and default state is not pulled-up.

"-": Pull-up control function is not available.

For details of pull-up control function, refer to PUPR0 through PUPR12 registers in section 5, Pin Function Controller (PFC).

Notes: 1. All power supply pins and ground pins including VCCQ, VCCQ18, VDD, VDDQ_M0, VDDQ_M0BKUP and VSS pins which are not described in Table 4.3 must be used.

2. All mode pins (MD[21:18],[14:0] and MDT[1:0]) must be used during power-on reset. For details of mode pins setting, refer to section 3.3, Mode Pin Settings.

3. Boot related pins (LBSC or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[0]	GP-0-0	peripheral function selected by IP0[23:22]
GP0[1]	GP-0-1	peripheral function selected by IP0[24]
GP0[2]	GP-0-2	peripheral function selected by IP0[25]
GP0[3]	GP-0-3	peripheral function selected by IP0[27:26]
GP0[4]	GP-0-4	peripheral function selected by IP0[29:28]
GP0[5]	GP-0-5	peripheral function selected by IP0[31:30]
GP0[6]	GP-0-6	peripheral function selected by IP1[1:0]
GP0[7]	GP-0-7	peripheral function selected by IP1[3:2]
GP0[8]	GP-0-8	peripheral function selected by IP1[5:4]
GP0[9]	GP-0-9	peripheral function selected by IP1[7:6]
GP0[10]	GP-0-10	peripheral function selected by IP1[10:8]
GP0[11]	GP-0-11	peripheral function selected by IP1[12:11]
GP0[12]	GP-0-12	peripheral function selected by IP1[14:13]
GP0[13]	GP-0-13	peripheral function selected by IP1[17:15]
GP0[14]	GP-0-14	peripheral function selected by IP1[19:18]
GP0[15]	GP-0-15	peripheral function selected by IP1[21:20]
GP0[16]	GP-0-16	peripheral function selected by IP1[23:22]
GP0[17]	GP-0-17	peripheral function selected by IP1[24]
GP0[18]	GP-0-18	A2
GP0[19]	GP-0-19	peripheral function selected by IP1[26]
GP0[20]	GP-0-20	peripheral function selected by IP1[27]
GP0[21]	GP-0-21	peripheral function selected by IP1[29:28]
GP0[22]	GP-0-22	peripheral function selected by IP1[31:30]
GP0[23]	GP-0-23	peripheral function selected by IP2[1:0]
GP0[24]	GP-0-24	peripheral function selected by IP2[3:2]
GP0[25]	GP-0-25	peripheral function selected by IP2[5:4]
GP0[26]	GP-0-26	peripheral function selected by IP2[7:6]
GP0[27]	GP-0-27	peripheral function selected by IP2[9:8]
GP0[28]	GP-0-28	peripheral function selected by IP2[11:10]
GP0[29]	GP-0-29	peripheral function selected by IP2[13:12]
GP0[30]	GP-0-30	peripheral function selected by IP2[15:14]
GP0[31]	GP-0-31	peripheral function selected by IP2[17:16]

5.3.11 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP2 [31]	IP2 [30]	IP2 [29]	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP2[1:0]	A7	SCIFB0_RTS_N	SCIFA4_TXD_B	-	-	-	-	-	-
IP2[3:2]	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	-	-
IP2[5:4]	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	-	-
IP2[7:6]	A10	MSIOF1_SCK	IIC0_SCL_B (I2C6)	-	-	-	-	-	-
IP2[9:8]	A11	MSIOF1_SYNC	IIC0_SDA_B (I2C6)	-	-	-	-	-	-
IP2[11:10]	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	-	-
IP2[13:12]	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	-	-
IP2[15:14]	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1_N	-	-	-	-	-
IP2[17:16]	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	-	-
IP2[20:18]	A16	MSIOF2_SCK	HSCIF0_HSCK_B	Reserved	Reserved	CAN_CLK_C	TPUTO2_B	-	-
IP2[23:21]	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	Reserved	-	-	-	-
IP2[26:24]	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	Reserved	-	-	-	-
IP2[29:27]	A19	MSIOF2_SS2	PWM4	TPUTO2	Reserved	-	-	-	-
IP2[31:30]	A20	SPCLK	Reserved	-	-	-	-	-	-

Legend: - Setting prohibited

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_msi2[0]	+ select pin A14 for function MSIOF2_RXD + select pin A15 for function MSIOF2_TXD + select pin A16 for function MSIOF2_SCK + select pin A17 for function MSIOF2_SYNC + select pin A18 for function MSIOF2_SS1 + select pin A19 for function MSIOF2_SS2	+ select pin ETH_CRS_DV for function MSIOF2_TXD_B + select pin ETH_LINK for function MSIOF2_SS2_B + select pin ETH_MDIO for function MSIOF2_RXD_B + select pin ETH_RXD0 for function MSIOF2_SYNC_B + select pin ETH_RXD1 for function MSIOF2_SS1_B + select pin ETH_RX_ER for function MSIOF2_SCK_B			
sel_rad[0]	+ select pin ETH_CRS_DV for function ADICS_SAMP + select pin ETH_LINK for function ADICHS2 + select pin ETH_MDIO for function ADIDATA + select pin ETH_RXD0 for function ADICHS0 + select pin ETH_RXD1 for function ADICHS1 + select pin ETH_RX_ER for function ADICLK	+ select pin SSI_SCK0129 for function ADIDATA_B + select pin SSI_SCK34 for function ADICHS0_B + select pin SSI_SDATA0 for function ADICLK_B + select pin SSI_SDATA3 for function ADICHS2_B + select pin SSI_WS0129 for function ADICS_SAMP_B + select pin SSI_WS34 for function ADICHS1_B			
sel_scifa0[1:0]	+ select pin MSIOF0_SS1 for function SCIFA0_RXD + select pin MSIOF0_SS2 for function SCIFA0_TXD	+ select pin A8 for function SCIFA0_RXD_B + select pin A9 for function SCIFA0_TXD_B	+ select pin DU0_DG0 for function SCIFA0_RXD_C + select pin DU0_DG1 for function SCIFA0_TXD_C	+ select pin SSI_SDATA2 for function SCIFA0_TXD_D + select pin SSI_WS2 for function SCIFA0_RXD_D	
sel_scifa1[1:0]	+ select pin D13 for function SCIFA1_SCK + select pin D14 for function SCIFA1_RXD + select pin D15 for function SCIFA1_TXD	+ select pin SSI_SCK6 for function SCIFA1_SCK_B + select pin SSI_SDATA6 for function SCIFA1_TXD_B + select pin SSI_WS6 for function SCIFA1_RXD_B	+ select pin SSI_SCK34 for function SCIFA1_SCK_C + select pin SSI_SDATA3 for function SCIFA1_TXD_C + select pin SSI_WS34 for function SCIFA1_RXD_C		
sel_scifa2[0]	+ select pin EX_CS3_N for function SCIFA2_SCK + select pin EX_CS4_N for function SCIFA2_RXD + select pin EX_CS5_N for function SCIFA2_TXD	+ select pin SSI_SCK78 for function SCIFA2_SCK_B + select pin SSI_SDATA7 for function SCIFA2_TXD_B + select pin SSI_WS78 for function SCIFA2_RXD_B			
sel_scifa3[0]	+ select pin SSI_SCK5 for function SCIFA3_SCK + select pin SSI_SDATA5 for function SCIFA3_TXD + select pin SSI_WS5 for function SCIFA3_RXD	+ select pin D0 for function SCIFA3_SCK_B + select pin D1 for function SCIFA3_RXD_B + select pin D2 for function SCIFA3_TXD_B			
sel_scifa4[1:0]	+ select pin HSCIF1_HCTS_N for function SCIFA4_RXD + select pin HSCIF1_HRTS_N for function SCIFA4_TXD	+ select pin A6 for function SCIFA4_RXD_B + select pin A7 for function SCIFA4_TXD_B	+ select pin DU0_DB0 for function SCIFA4_RXD_C + select pin DU0_DB1 for function SCIFA4_TXD_C	+ select pin AUDIO_CLKA for function SCIFA4_RXD_D + select pin AUDIO_CLKB for function SCIFA4_TXD_D	
sel_scifa5[1:0]	+ select pin I2C2_SCL for function SCIFA5_RXD + select pin I2C2_SDA for function SCIFA5_TXD	+ select pin A12 for function SCIFA5_RXD_B + select pin A13 for function SCIFA5_TXD_B	+ select pin VI0_CLKENB for function SCIFA5_RXD_C + select pin VI0_FIELD for function SCIFA5_TXD_C	+ select pin AUDIO_CLKC for function SCIFA5_RXD_D + select pin AUDIO_CLKOUT for function SCIFA5_TXD_D	
sel_tmu[0]	+ select pin D7 for function TCLK1 + select pin SCIF1_SCK for function TCLK2	+ select pin D13 for function TCLK2_B + select pin I2C0_SCL for function TCLK1_B			
sel_can0[1:0]	+ select pin SD1_CD for function CAN0_RX + select pin SD1_WP for function CAN0_TX	+ select pin ETH_RXD0 for function CAN0_TX_B + select pin ETH_RX_ER for function CAN0_RX_B	+ select pin DU0_DB0 for function CAN0_RX_C + select pin DU0_DB1 for function CAN0_TX_C	+ select pin SSI_SCK1 for function CAN0_RX_D + select pin SSI_WS1 for function CAN0_TX_D	
sel_can1[1:0]	+ select pin MMC_D6 for function CAN1_RX + select pin MMC_D7 for function CAN1_TX	+ select pin A17 for function CAN1_RX_B + select pin A18 for function CAN1_TX_B	+ select pin SSI_SDATA3 for function CAN1_TX_C + select pin SSI_WS34 for function CAN1_RX_C	+ select pin I2C0_SCL for function CAN1_RX_D + select pin I2C0_SDA for function CAN1_TX_D	
sel_hscif0[0]	+ select pin HSCIF0_HRX for function HRX0 + select pin HSCIF0_HSCK for function HSCK0 + select pin HSCIF0_HTX for function HTX0	+ select pin A14 for function HRX0_B + select pin A15 for function HTX0_B + select pin A16 for function HSCK0_B			

5.3.25 Module Select Register 3 (MOD_SEL3)

Function: MOD_SEL3 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 and ssi7 (in MOD_SEL3 register) are to be used simultaneously, the values of sel_ssi8[0] and sel_ssi7[0] must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_scif 0[1]	sel_scif 0[0]	sel_scif 1[1]	sel_scif 1[0]	sel_scif 2[1]	sel_scif 2[0]	sel_scif 3[0]	sel_scif 4[2]	sel_scif 4[1]	sel_scif 4[0]	sel_scif 5[1]	sel_scif 5[0]	sel_ssi 1[0]	sel_ssi 2[0]	sel_ssi 4[0]	sel_ssi 5[0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ssi 6[0]	sel_ssi 7[0]	sel_ssi 8[0]	sel_ssi 9[0]	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scif0[1:0]	+ select pin EX_WAIT0 for function SCIF_CLK + select pin MMC_D6 for function SCIF0_RXD + select pin MMC_D7 for function SCIF0_TX0	+ select pin HSCIF0_HSCK for function SCIF_CLK_B + select pin VI0_HSYNC_N for function SCIF0_RXD_B + select pin VI0_VSYNC_N for function SCIF0_TXD_B	+ select pin I2C0_SCL for function SCIF0_RXD_C + select pin I2C0_SDA for function SCIF0_TXD_C	+ select pin HSCIF0_HCTS_N for function SCIF0_RXD_D + select pin HSCIF0_HRTS_N for function SCIF0_TXD_D	
sel_scif1[1:0]	+ select pin SCIF1_RXD for function SCIF1_RXD + select pin SCIF1_SCK for function SCIF1_SCK + select pin SCIF1_TXD for function SCIF1_TXD	+ select pin SSI_SCK1 for function SCIF1_RXD_B + select pin SSI_SDATA8 for function SCIF1_SCK_B + select pin SSI_WS1 for function SCIF1_TXD_B	+ select pin D10 for function SCIF1_SCK_C + select pin D11 for function SCIF1_RXD_C + select pin D12 for function SCIF1_TXD_C		
sel_scif2[2:0]	+ select pin SCIF2_RXD for function SCIF2_RXD + select pin SCIF2_SCK for function SCIF2_SCK + select pin SCIF2_TXD for function SCIF2_TXD	+ select pin SSI_SCK9 for function SCIF2_SCK_B + select pin SSI_SDATA9 for function SCIF2_TXD_B + select pin SSI_WS9 for function SCIF2_RXD_B	+ select pin ETH_REF_CLK for function SCIF2_SCK_C + select pin ETH_TXD1 for function SCIF2_RXD_C + select pin ETH_TX_EN for function SCIF2_TXD_C		
sel_scif3[0]	+ select pin SCIF3_RXD for function SCIF3_RXD + select pin SCIF3_SCK for function SCIF3_SCK + select pin SCIF3_TXD for function SCIF3_TXD	+ select pin ETH_MAGIC for function SCIF3_SCK_B + select pin ETH_MDC for function SCIF3_TXD_B + select pin ETH_TXD0 for function SCIF3_RXD_B			
sel_scif4[2:0]	+ select pin I2C1_SCL for function SCIF4_RXD + select pin I2C1_SDA for function SCIF4_TXD	+ select pin D5 for function SCIF4_RXD_B + select pin D6 for function SCIF4_TXD_B	+ select pin EX_CS2_N for function SCIF4_RXD_C + select pin EX_CS3_N for function SCIF4_TXD_C	+ select pin ETH_LINK for function SCIF4_TXD_D + select pin ETH_RXD1 for function SCIF4_RXD_D	+ select pin A17 for function SCIF4_RXD_E + select pin A18 for function SCIF4_TXD_E

5.3.26 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR0 [31]	PUPR0 [30]	PUPR0 [29]	PUPR0 [28]	PUPR0 [27]	PUPR0 [26]	PUPR0 [25]	PUPR0 [24]	PUPR0 [23]	PUPR0 [22]	PUPR0 [21]	PUPR0 [20]	PUPR0 [19]	PUPR0 [18]	PUPR0 [17]	PUPR0 [16]
Initial value:	0	1	0	1	1	1	0	1	0	1	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR0 [15]	PUPR0 [14]	PUPR0 [13]	PUPR0 [12]	PUPR0 [11]	PUPR0 [10]	PUPR0 [9]	PUPR0 [8]	PUPR0 [7]	PUPR0 [6]	PUPR0 [5]	PUPR0 [4]	PUPR0 [3]	PUPR0 [2]	PUPR0 [1]	PUPR0 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR0[31:0]	H'5D60 FFFF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Bit Name	Set Value = 1
PUPR0[31]	A15 is pull up
PUPR0[30]	A14 is pull up
PUPR0[29]	A13 is pull up
PUPR0[28]	A12 is pull up
PUPR0[27]	A11 is pull up
PUPR0[26]	A10 is pull up
PUPR0[25]	A9 is pull up
PUPR0[24]	A8 is pull up
PUPR0[23]	A7 is pull up
PUPR0[22]	A6 is pull up
PUPR0[21]	A5 is pull up
PUPR0[20]	A4 is pull up
PUPR0[19]	A3 is pull up
PUPR0[18]	A2 is pull up
PUPR0[17]	A1 is pull up
PUPR0[16]	A0 is pull up
PUPR0[15]	D15 is pull up
PUPR0[14]	D14 is pull up
PUPR0[13]	D13 is pull up
PUPR0[12]	D12 is pull up
PUPR0[11]	D11 is pull up
PUPR0[10]	D10 is pull up
PUPR0[9]	D9 is pull up
PUPR0[8]	D8 is pull up
PUPR0[7]	D7 is pull up

5.3.29 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR3 [31]	PUPR3 [30]	PUPR3 [29]	PUPR3 [28]	PUPR3 [27]	PUPR3 [26]	PUPR3 [25]	PUPR3 [24]	PUPR3 [23]	PUPR3 [22]	PUPR3 [21]	PUPR3 [20]	PUPR3 [19]	PUPR3 [18]	PUPR3 [17]	PUPR3 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR3 [15]	PUPR3 [14]	PUPR3 [13]	PUPR3 [12]	PUPR3 [11]	PUPR3 [10]	PUPR3 [9]	PUPR3 [8]	PUPR3 [7]	PUPR3 [6]	PUPR3 [5]	PUPR3 [4]	PUPR3 [3]	PUPR3 [2]	PUPR3 [1]	PUPR3 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR3[31:0]	H'FFFF FFFF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR3[31]	I2C1_SDA is pull up
PUPR3[30]	I2C1_SCL is pull up
PUPR3[29]	I2C0_SDA is pull up
PUPR3[28]	I2C0_SCL is pull up
PUPR3[27]	HSCIF0_HSCK is pull up
PUPR3[26]	HSCIF0_HRTS_N is pull up
PUPR3[25]	HSCIF0_HCTS_N is pull up
PUPR3[24]	HSCIF0_HTX is pull up
PUPR3[23]	HSCIF0_HRX is pull up
PUPR3[22]	ETH_MDC is pull up
PUPR3[21]	ETH_TXD0 is pull up
PUPR3[20]	ETH_MAGIC is pull up
PUPR3[19]	ETH_TX_EN is pull up
PUPR3[18]	ETH_TXD1 is pull up
PUPR3[17]	ETH_REF_CLK is pull up
PUPR3[16]	ETH_LINK is pull up
PUPR3[15]	ETH_RXD1 is pull up
PUPR3[14]	ETH_RXD0 is pull up
PUPR3[13]	ETH_RX_ER is pull up
PUPR3[12]	ETH_CRS_DV is pull up
PUPR3[11]	ETH_MDIO is pull up
PUPR3[10]	VI0_VSYNC_N is pull up
PUPR3[9]	VI0_HSYNC_N is pull up
PUPR3[8]	VI0_FIELD is pull up
PUPR3[7]	VI0_CLKENB is pull up

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