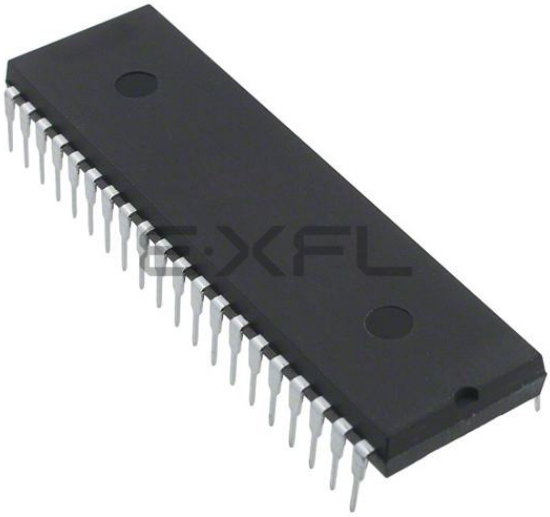

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Supplier Device Package	-
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SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
IP1	INTERRUPT PRIORITY 1	F8H	PCAP	PBO	-	PWDI	-	-	PKB	PI2	00x0 xx00B
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PBOH	-	PWDIH	-	-	PKBH	PI2H	00x0 xx00B
B	B REGISTER	F0H	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	0000 0000B
P5M2	PORT 5 OUTPUT MODE 2	EEH	-	-	-	-	-	-	P5M2.1	P5M2.0	CONFIG0.PMODE=1; Xxxx xx00B CONFIG0.PMODE=0; Xxxx xx11B
P5M1	PORT 5 OUTPUT MODE 1	EDH	-	-	-	-	-	ENCLK	P5M1.1	P5M1.0	CONFIG0.PMODE=1; Xxxx x000B CONFIG0.PMODE=0; Xxxx x011B
PORTS	PORT SHMITT REGISTER	ECH	-	-	P5S	-	P3S	P2S	P1S	P0S	xx0x 0000B
KBL	KEYBOARD LEVEL REGISTER	E9H	KBL.7	KBL.6	KBL.5	KBL.4	KBL.3	KBL.2	KBL.1	KBL.0	0000 0000B
EIE	INTERRUPT ENABLE 1	E8H	ECPTF	EBO	-	EWDI	-	-	EKB	EI2	00x0 xx00B
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000B
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000B
ACC	ACCUMULATOR	E0H	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	0000 0000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	-	-	CLRPWM	-	-	-	-	0xx0 xxxxB
PWM1L	PWM 1 LOW BITS REGISTER	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	WDRUN	POR	-	-	WDIF	WTRF	EWRST	WDCLR	POR: X1xx 0000B External reset: Xxxx 0xx0B Watchdog reset: Xxxx 01x0B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	PWM1OE	PWM0OE	PCLK.1	PCLK.0	FP1	FP0	Xx00 0000B
PSW	PROGRAM STATUS WORD	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000B
NVMDATA	NVM DATA	CFH	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA.3	NVMDATA.2	NVMDATA.1	NVMDATA.0	0000 0000B
NVMCON	NVM CONTROL	CEH	EER	EWR	EnNVM	-	-	-	-	-	000x xxxxB
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000B
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000B
T2MOD	TIMER 2 MODE	C9H	-	-	-	ICEN0	T2CR	1	T2OE	DCEN	Xxx0 0100B
T2CON	TIMER 2 CONTROL	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL	0000 0000B
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B
NVMADDR	NVM LOW BYTE ADDRESS	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	0000 0000B
STATUS	STATUS REGISTER	C5H	-	-	-	-	-	-	SPTA0	SPRA0	Xxxx xx00B
PMR	POWER MANAGEMENT REGISTER	C4H	CD1	CD0	SWB	-	-	ALE-OFF	-	-	010x xxxxB
ROMMAP	ROMMAP REGISTER	C2H	WS	1	-	-	-	1	1	0	01xxx110B
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxxxxx0B

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	Xxxx xxxxB
SCON	SERIAL CONTROL	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000B
P5	PORT5	94H	-	-	-	-	-	-	P5.1	P5.0	Xxxx xx11B
			-	-	-	-	-	-	XTAL1	XTAL2	
			-	-	-	-	-	-	-	CLKOUT	
P1	PORT 1	90H	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	1111 1111B
			-	-	PWM1	PWM0	SCL	SDA	T2EX	T2	
CKCON	CLOCK CONTROL	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000B
TH0	TIMER HIGH 0	8CH	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	0000 0000B
TL1	TIMER LOW 1	8BH	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	0000 0000B
TL0	TIMER LOW 0	8AH	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	0000 0000B
TMOD	TIMER MODE	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B
TCON	TIMER CONTROL	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000B
PCON	POWER CONTROL	87H	SM0D	SMOD0	BOF	-	GF1	GF0	PD	IDL	001x 0000B
DPS	DATA POINTER SELECT	86H	-	-	-	-	-	-	-	DPS.0	Xxxx xxx0B
DPH1	DATA POINTER HIGH 1	85H	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0	0000 0000B
DPL1	DATA POINTER LOW 1	84H	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0	0000 0000B
DPH	DATA POINTER HIGH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	0000 0000B
DPL	DATA POINTER LOW	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	0000 0000B
SP	STACK POINTER	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	0000 0111B
P0	PORT 0	80H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	1111 1111B
			AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
			KB7	KB6	KB5	KB4	KB3	KB2	KB1	KB0	

8.2 SFR Detail Bit Descriptions

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain bi-directional I/O port. This port provides a multiplexed low order address/data bus during accesses to external memory. The ports also support alternate input function for Keyboard pins (KB0-7).

BIT	NAME	FUNCTION
7	P0.7	AD7 or KB7 or I/O pin by alternative.
6	P0.6	AD6 or KB6 or I/O pin by alternative.
5	P0.5	AD5 or KB5 or I/O pin by alternative.
4	P0.4	AD4 or KB4 or I/O pin by alternative.
3	P0.3	AD3 or KB3 or I/O pin by alternative.
2	P0.2	AD2 or KB2 or I/O pin by alternative.
1	P0.1	AD1 or KB1 or I/O pin by alternative.
0	P0.0	AD0 or KB0 or I/O pin by alternative.

Note: The initial value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0

2-1	-	Reserved.
0	CPTF0	External input capture 0 interrupt flag. It can be cleared by software.

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3~0	P4.3~0	Port 4 is a bi-directional I/O port with internal pull-ups. Port 4 can not use bit-addressable instruction (SETB or CLR).

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	-	Reserved.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

PORT 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

9. INSTRUCTION

The N79E352(R) executes all the instructions of the standard 8052 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the N79E352(R), each machine cycle consists of 4 clock periods, while in the standard 8052 it consists of 12 clock periods. Also, in the N79E352(R) there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8052 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the N79E352(R) has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the N79E352(R) reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8052.

Table 9-1: Instructions that affect Flag settings

Instruction	Carry	Overflow	Auxiliary Carry	Instruction	Carry	Overflow	Auxiliary Carry
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

A "X" indicates that the modification is as per the result of instruction.

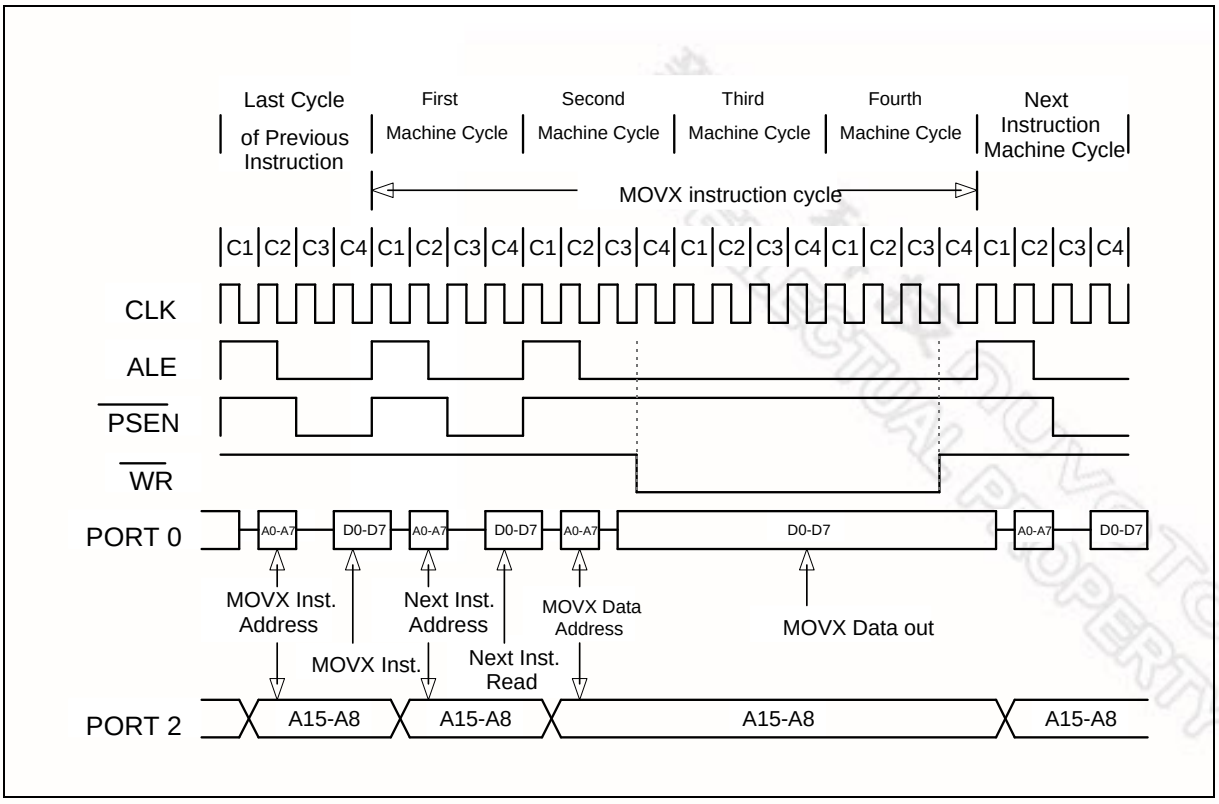


Figure 9-8: Data Memory Write with Stretch Value = 2

9.4 Wait State Control Signal

Either with the software using stretch value to change the required machine cycle of MOVX instruction, the N79E352(R) provides another hardware signal $\overline{\text{WAIT}}$ to implement the wider duration of external data access timing. This wait state control signal is the alternate function of P4.0. The wait state control signal can be enabled by setting WS (SFR ROMMAP.7) bit. When enabled, the setting of stretch value decides the minimum length of MOVX instruction cycle and the device will sample the $\overline{\text{WAIT}}$ pin at each C2 state before the rising edge of read/write strobe signal during MOVX instruction. Once this signal being recongnized, one more machine cycle (wait state cycle) will be inserted into next cycle. The inserted wait state cycles are unlimited, so the MOVX instruction cycle will end in which the wait state control signal is deactivated. Using wait state control signal allows a dynamically access timimg to a selected external peripheral. The WS bit is accessed by the Timed Access Protection procedure.

reducing of operating speed is restricted. In order to solve these dilemmas, the N79E352(R) offers a switchback feature which allows the CPU back to clock/4 mode immediately when triggered by serial operation (uart and I2C) or external interrupts. The switchback feature is enabled by setting the SWB bit (PMR.5). A serial port/I2C reception/transmission or qualified external interrupt which is enabled and acknowledged without block conditions will cause CPU to return to divide by 4 mode. For the serial port reception, a switchback is generated by a falling edge associated with start bit if the serial port reception is enabled. When a serial port transmission, an instruction which writes a byte of data to serial port buffer will cause a switchback to ensure the correct transmission. The switchback feature is unaffected by serial port interrupt flags. Similarly for I2C reception/transmission, a switchback is generated when a start condition is determined. After a switchback is generated, the software can manually return the CPU to Economy mode. Note that the modification of clock control bits CD0 and CD1 will be ignored during I2C or serial port transmit/receive when switchback is enabled. The Watchdog timer reset, power-on/fail reset, software reset, brownout reset or external reset will force the CPU to return to divide by 4 mode.

10.3 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and $\overline{\text{PSEN}}$ pins are pulled low. The port pins output the values held by their respective SFRs.

The N79E352(R) will exit the Power Down mode with a reset or by an external interrupt pin. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power down mode are external interrupts, keyboard interrupt (KBI), brownout reset (BOR), and watchdog timer interrupt (if WDTCK = 0).

The N79E352(R) can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the low level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one which put the device into Power Down mode and continues from there.

executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock speed. The reset will occur, when enabled, 512 clocks after the time-out has occurred.

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 20 KHZ
0	0	2^6	64	3.2 mS
0	1	2^9	512	25.6 mS
1	0	2^{13}	8192	409.6 mS
1	1	2^{15}	32768	1638.4 mS

Table 14-1: Time-out values for the Watchdog timer.

The default Watchdog time-out is 2^6 clocks, which is the shortest time-out period. The EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTCK is located at bit 7 of CONFIG0 register. This bit is for user to configure the clock source of watchdog timer either from the internal RC or from the uC clock.

15.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The N79E352(R) has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the N79E352(R) it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

15.6 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the N79E352(R), the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100
SADEN 1111 1010
Given 1010 0x0x

Slave 2:

SADDR 1010 0111
SADEN 1111 1001
Given 1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical ORing of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

16.2 The I2C Control Registers:

The I2C has 1 control register (I2CON) to control the transmit/receive flow, 1 data register (I2DAT) to buffer the Tx/Rx data, 1 status register (I2STATUS) to catch the state of Tx/Rx, recognizable slave address register for slave mode use and 1 clock rate control block for master mode to generate the variable baud rate.

16.2.1 The Address Registers, I2ADDR

I2C port is equipped with one slave address register. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR are matched with the received slave address.

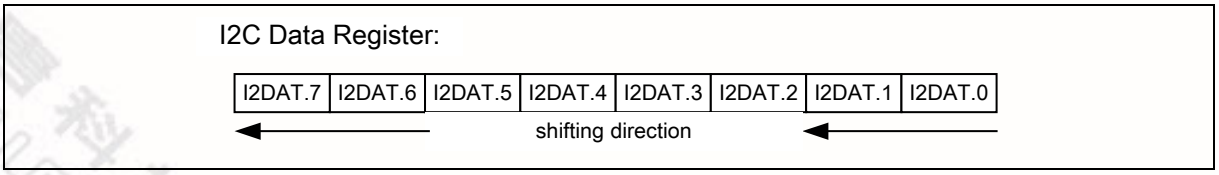
The I2C ports support the "General Call" function. If the GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

When GC bit is set, the I2C is in Slave mode, it can be received the general call address by 00H after Master send general call address to I2C bus, then it will follow status of GC mode. If it is in Master mode, the AA bit must be cleared when it will send general call address of 00H to I2C bus.

16.2.2 The Data Register, I2DAT

This register contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from or write to this 8-bit directly addressable SFR while it is not in the process of shifting a byte. This occurs when the bus is in a defined state and the serial interrupt flag (SI) is set. Data in I2DAT remains stable as long as SI bit is set. While data is being shifted out, data on the bus is simultaneously being shifted in; I2DAT always contains the last data byte present on the bus. Thus, in the event of arbitration lost, the transition from master transmitter to slave receiver is made with the correct data in I2DAT.

I2DAT and the acknowledge bit form a 9-bit shift register, the acknowledge bit is controlled by the hardware and cannot be accessed by the CPU. Serial data is shifted through the acknowledge bit into I2DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2DAT, the serial data is available in I2DAT, and the acknowledge bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I2DAT on the falling edges of SCL clock pulses, and is shifted into I2DAT on the rising edges of SCL clock pulses.



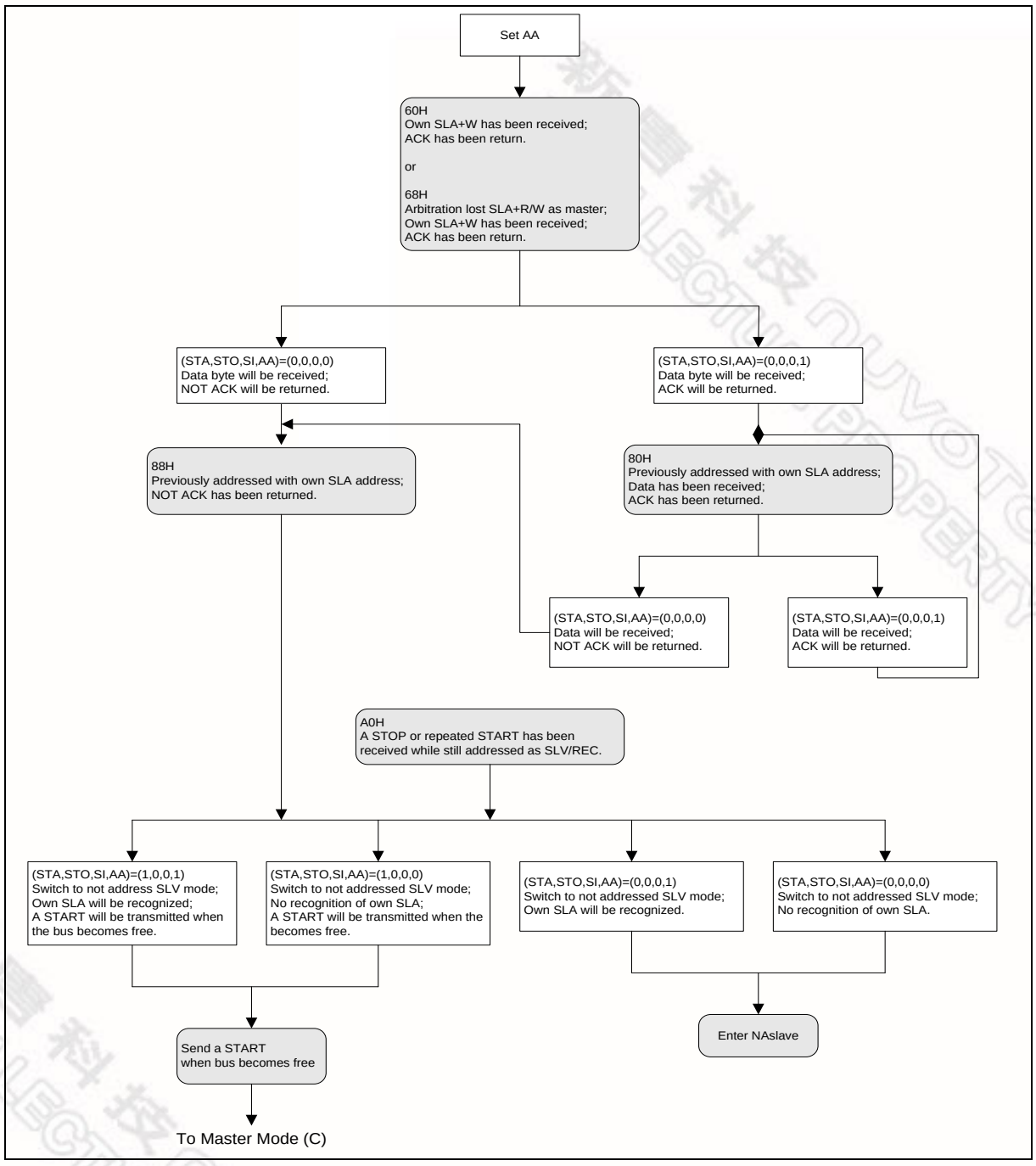


Figure 16-7: Slave Receiver Mode

transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the device is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Management for details.

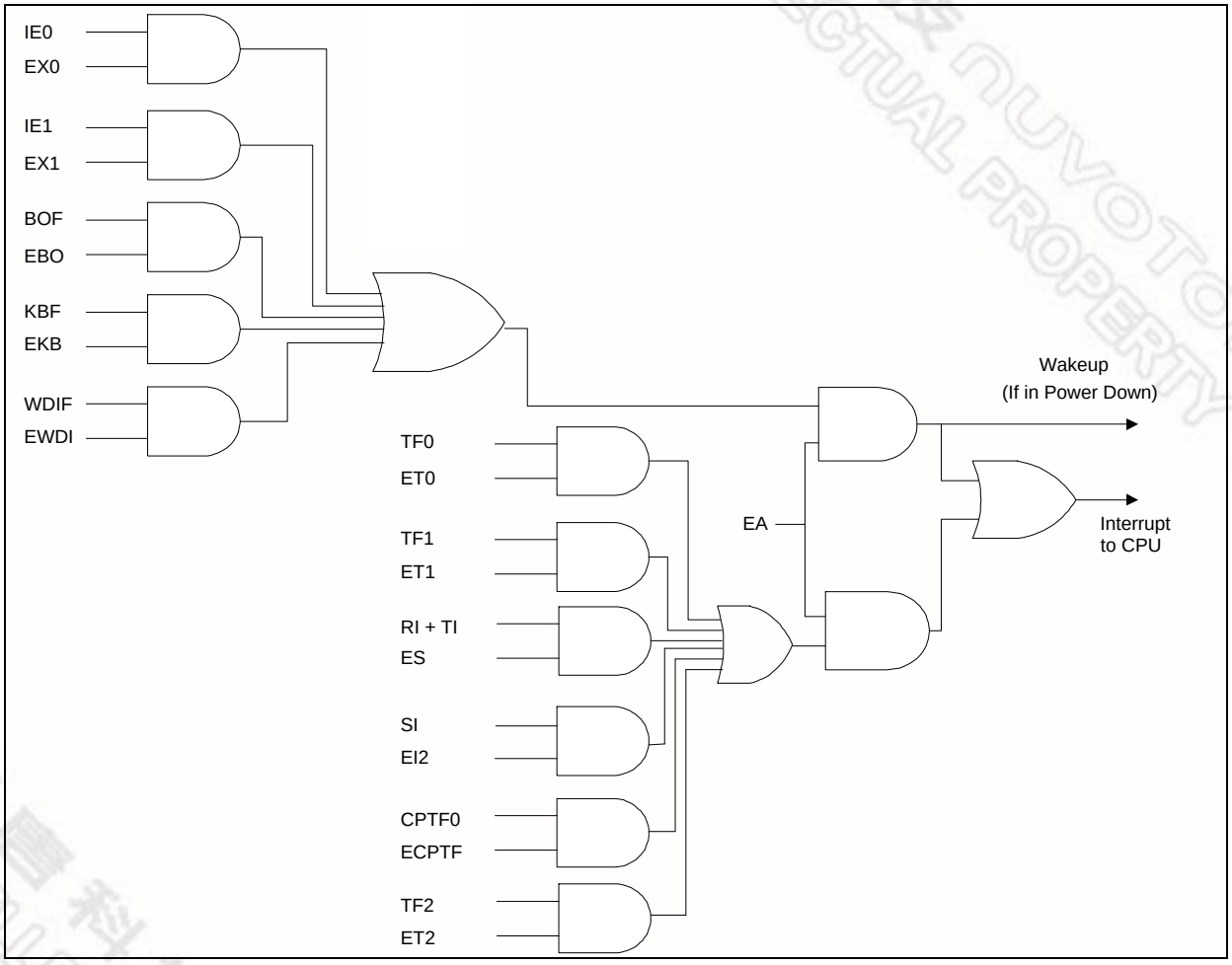


Figure 18- 1: Interrupt inputs

19. KEYBOARD FUNCTION

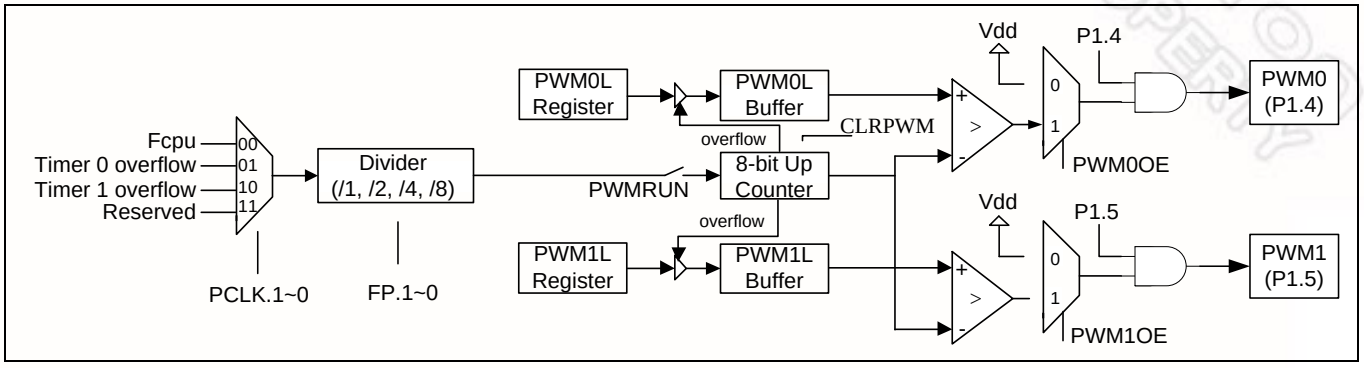
The N79E352(R) provideds 8 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad

21. PULSE WIDTH MODULATED OUTPUTS (PWM)

The N79E352(R) contains two Pulse Width Modulated (PWM) channels which generate pulses of programmable length and interval. The output for PWM0 is on P1.4 and PWM1 on P1.5. After chip reset the internal output of the each PWM channel is a “1” (if PRHI=1). The PWM block diagram is shown as below figure. The interval between successive outputs is controlled by a 8–bit up-counter which uses the selectable clock sources. The clock sources supported are cpu clock, timer 0 overflow and timer 1 overflow, selectable by PWMCON3.PCLK.1~0 bits. The clock sources can be further divided with programmable PWMCON3.FP1~0 bits. When the counter reaches overflow, it is reloaded with zero.

The width of each PWM output pulse is determined by the value in the appropriate Compare registers, PWMnL (n=0,1). When the counter described above matches compare register value the PWM output is forced low. It remains low until the counter value overflow. The number of clock pulses that the PWMn output is low is given by:

t_{LO} = (FFh – PWMn+1)



A compare value of all zeroes, 00H, causes the output to remain permanently high. A compare value of all ones, FFH, results in the PWM output remaining permanently low.

The overall functioning of the PWM module is controlled by the contents of the PWMCON1 and PWMCON3 registers. The operation of most of the control bits are straightforward. The transfer Compare registers to the buffer registers is controlled by 8-bit counter overflow, while PWMCON1.7 (PWMRUN) allows the PWM to be either in the run or idle state. It has a CLRPWM bit to clear 8-bt up counter.

When the PWMRUN is cleared, the PWM outputs take on the state they had just prior to the bit being cleared. In general this state is not known. In order to place the outputs in a known state when PWMRUN is cleared the Compare registers can be written to either the “all 1” or “all 0” so the output will have the output desired when the counter is halted.

Note:

During PWM initial run, user is recommended to configure proper PWMn and/or PWM output pin (default high) follow by setting PWMRUN and CLRPWM bits, prior to enable PWMnOE. This is to avoid unexpected PWM output.

The default port output configuration for standard N79E352(R) I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again. The quasi-bidirectional port configuration is shown as below.

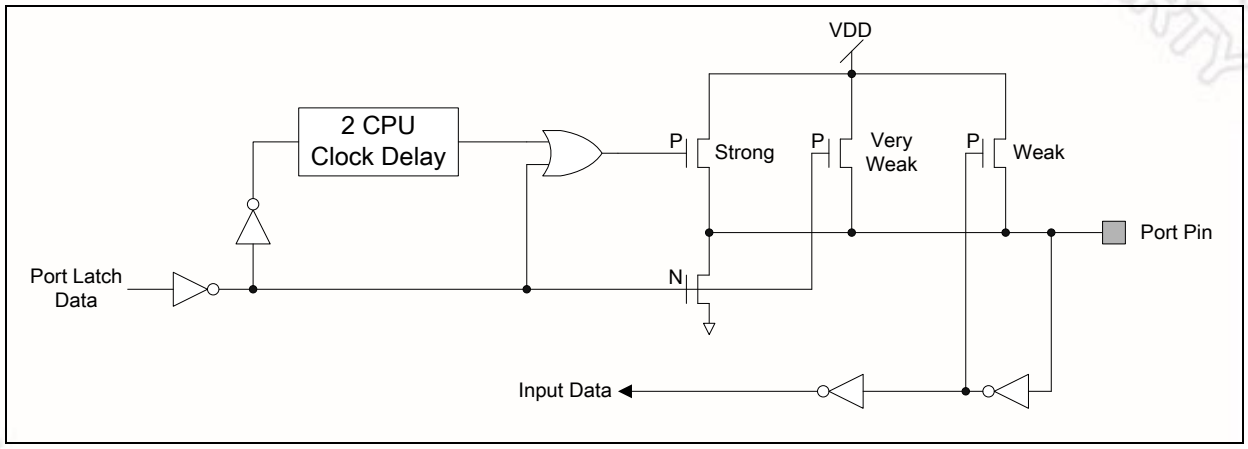


Figure 22-1: Quasi-Bidirectional Output

22.2 Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to VDD. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open drain port configuration is shown as below.

23. OSCILLATOR

N79E352(R) provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 24MHz, and without capacitor or resister.

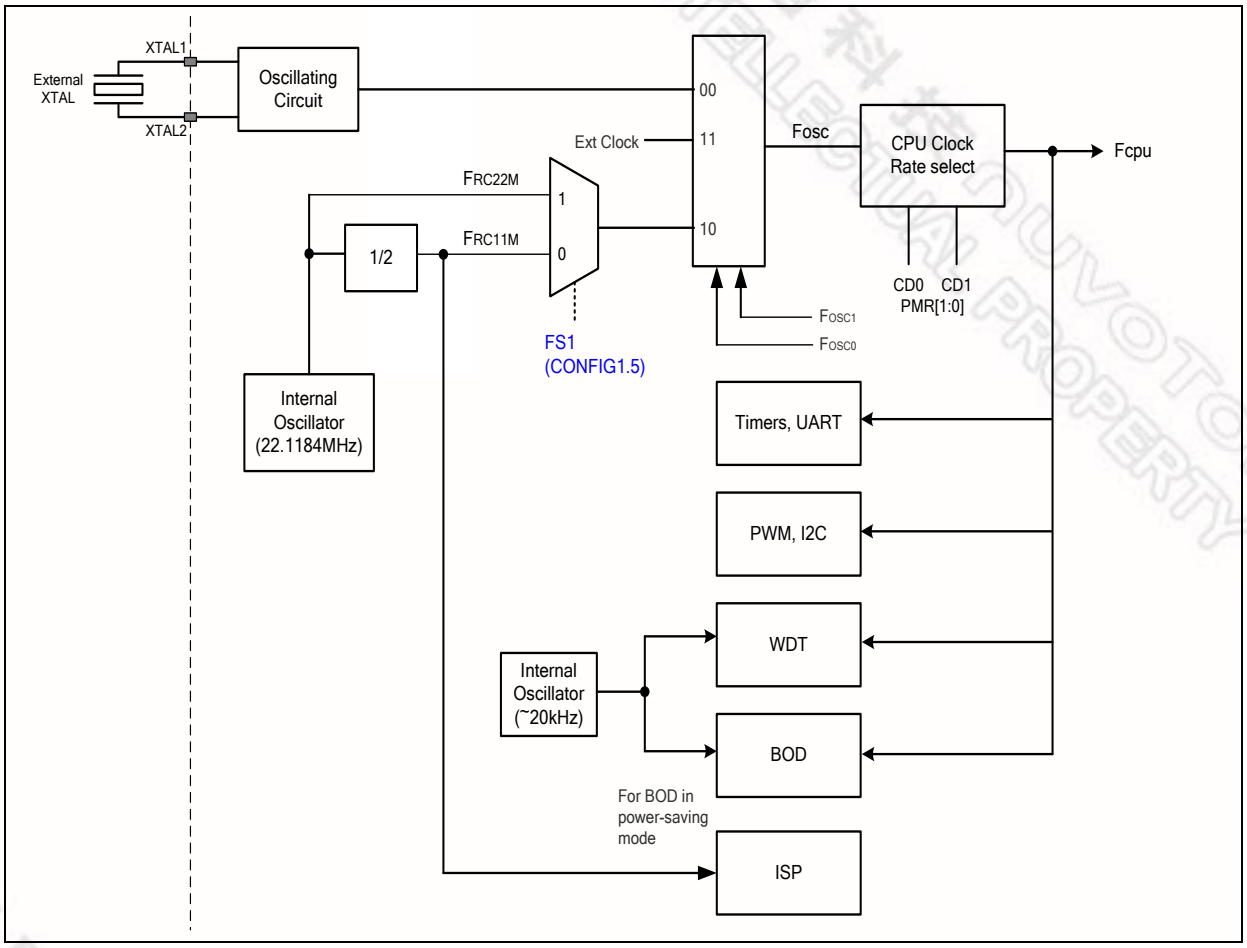


Figure 23-1: Oscillator

23.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is fixed at 11.0592MHz or 22.1184MHz (selectable by FS1 config bit) ±2% for N79E352R, ±25% for N79E352 frequency to support clock source. When FOSC1, FOSC0 = 01b, the On-Chip RC Oscillator is enabled.

23.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is ffrom 0Hz up to 24MHz.

The device supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the device. When enabled, via the ENCLK bit in the P5M1 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering

25. ICP(IN-CIRCUIT PROGRAM) FLASH PROGRAM

The ICP(In-Circuit-Program) mode is another approach to access the Flash EPROM. There are only 3 pins needed to perform the ICP function. One is mode input, shared with RST pin, which must be kept in Vdd voltage in the entire ICP working period. One is clock input, shared with P1.7, which accepts serial clock from external device. Another is data I/O pin, shared with P1.6, that an external ICP program tool shifts in/out data via P1.6 synchronized with clock(P1.7) to access the Flash EPROM of N79E352(R).

(Note, While PRHI=0, P1.6, P1.7 are still quasi high during reset period. During reset period , P1.6, P1.7 cann't switch to open-drain by setting config).

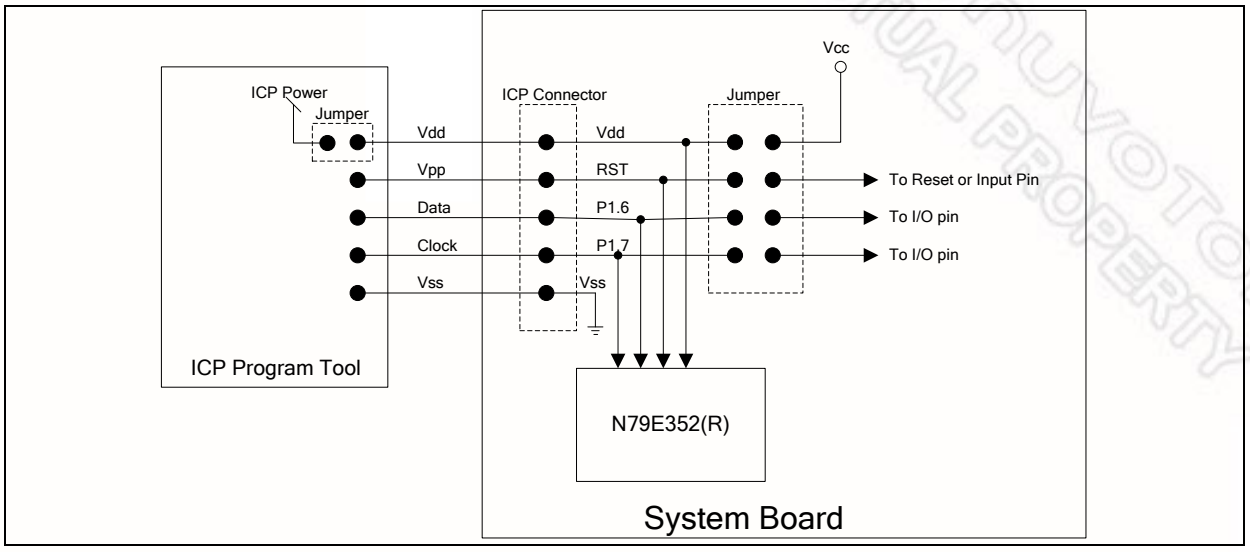


Figure 26-1: ICP Writer Tool connector pin assign

Note:

1. When using ICP to upgrade code, the RST, P1.6 and P1.7 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.
3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.
4. During ICP mode, all PWM pins will be tri-stated.

27.2 D.C. Characteristics

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4		5.5	V	V_{DD}=4.5V ~ 5.5V @ 24MHz V_{DD}=2.7V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 4MHz
Operating Current	I_{DD1}			5	mA	No load, RST = V_{DD}, V_{DD}= 3.0V @ 11.0592MHz
	I_{DD2}			15	mA	No load, RST = V_{DD}, V_{DD}= 5.0V @ 22.1184MHz
Idle Current	I_{IDLE}			4	mA	No load, V_{DD} = 3.0V @ 11.0592MHz
Power Down Current	I_{PWDN}		1	5	µA	No load, V_{DD} = 5.5V @ Disable BOV function
			1	5	uA	No load, V_{DD} = 3.0V @ Disable BOV function
Input / Output						
Input Current P0, P1, P2, P3, P4, P5	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current P1.5(RST pin)[1]	I_{IN2}	-48	-32	-24	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2, P3, P5 (Open Drain)	I_{LK}	-10	-	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4, P5	I_{TL} [*3]	-450	-	-246	µA	V_{DD} = 5.5V, V_{IN}<2.0V
		-93	-	-56		V_{DD}=2.4 Vin = 1.3v
Input Low Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6 1.0		V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 2.4V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		0.2V_{DD}		V	
Input Low Voltage RST [*1]	V_{IL21}	-	1.0	1.6	V	V_{DD}=4.5V

27.4 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
Frequency accuracy of On-chip RC oscillator (for N79E352)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
Frequency accuracy of On-chip RC oscillator with calibration[1] (for N79E352R)	-2		2	%	V_{DD}=4.5V~5.5V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		9	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

Note:

1. These values are for design guidance only and are not tested.

27.5 Typical Application Circuit

CRYSTAL	C1	C2	R
4MHz ~ 24MHz	without	without	without

The above table shows the reference values for crystal applications.