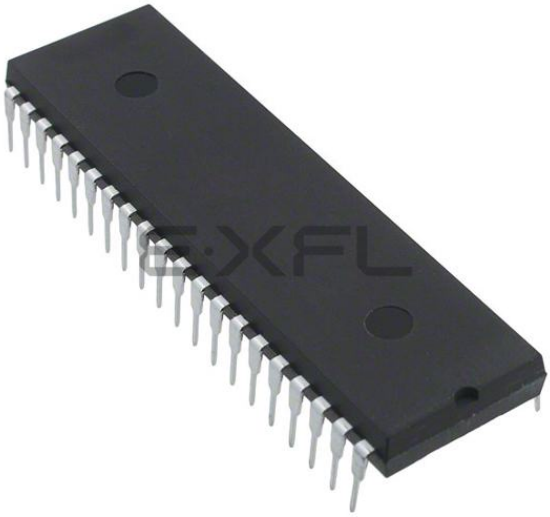
Nuvoton Technology Corporation - N79E352RADG Datasheet



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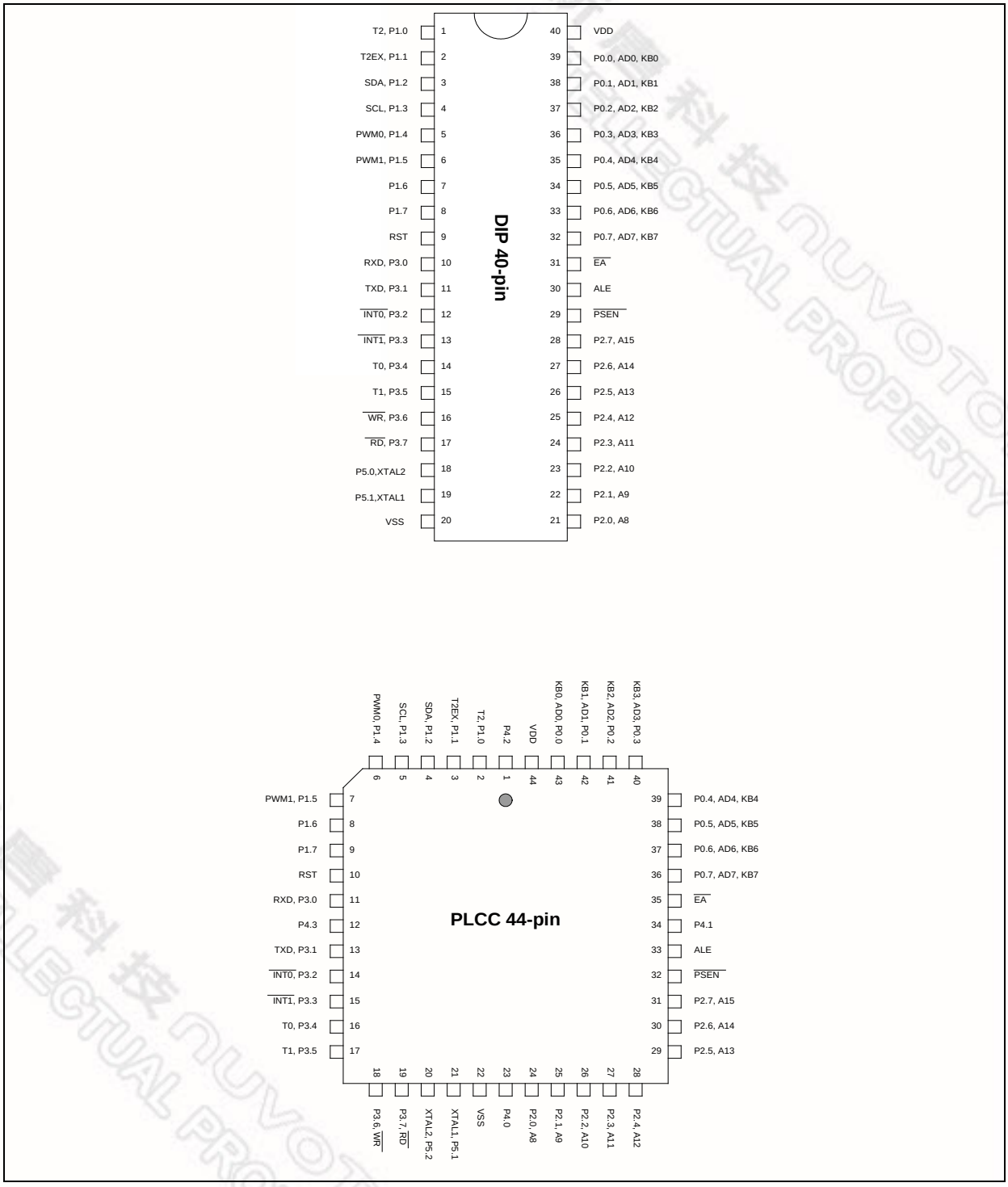
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e352radg

4. PIN CONFIGURATIONS



P2.0		A8	I/O	**PORT2:** Support 4 mode output and 2 mode input. Multifunction pins for A8-A15,.
P2.1		A9	I/O	
P2.2		A10	I/O	
P2.3		A11	I/O	
P2.4		A12	I/O	
P2.5		A13	I/O	
P2.6		A14	I/O	
P2.7		A15	I/O	
P3.0		RXD	I/O	**PORT3:** Support 4 mode output and 2 mode input. Multifunction pins for RXD & TXD (uart), /INT0, /INT1, T0, T1, /WR and /RD.
P3.1		TXD	I/O	
P3.2		/INT0	I/O	
P3.3		/INT1	I/O	
P3.4		T0	I/O	
P3.5		T1	I/O	
P3.6		/WR	I/O	
P3.7		/RD	I/O	
P4.0			I/O	**PORT4:** Quasi output with internal pull up.
P4.1			I/O	
P4.2			I/O	
P4.3			I/O	

* Note: TYPE I: input, O: output, I/O: bi-directional.

In application if any pins need external pull-up, it is recommended to add a pull-up resistor (10kΩ) between pin and power (V_{DD}) instead of directly wiring pin to V_{DD} for enhancing EMC.

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
IP1	INTERRUPT PRIORITY 1	F8H	PCAP	PBO	-	PWDI	-	-	PKB	PI2	00x0 xx00B
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PBOH	-	PWDIH	-	-	PKBH	PI2H	00x0 xx00B
B	B REGISTER	F0H	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	0000 0000B
P5M2	PORT 5 OUTPUT MODE 2	EEH	-	-	-	-	-	-	P5M2.1	P5M2.0	CONFIG0.PMODE=1; Xxxx xx00B CONFIG0.PMODE=0; Xxxx xx11B
P5M1	PORT 5 OUTPUT MODE 1	EDH	-	-	-	-	-	ENCLK	P5M1.1	P5M1.0	CONFIG0.PMODE=1; Xxxx x000B CONFIG0.PMODE=0; Xxxx x011B
PORTS	PORT SHMITT REGISTER	ECH	-	-	P5S	-	P3S	P2S	P1S	P0S	xx0x 0000B
KBL	KEYBOARD LEVEL REGISTER	E9H	KBL.7	KBL.6	KBL.5	KBL.4	KBL.3	KBL.2	KBL.1	KBL.0	0000 0000B
EIE	INTERRUPT ENABLE 1	E8H	ECPTF	EBO	-	EWDI	-	-	EKB	EI2	00x0 xx00B
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000B
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000B
ACC	ACCUMULATOR	E0H	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	0000 0000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	-	-	CLRPWM	-	-	-	-	0xx0 xxxxB
PWM1L	PWM 1 LOW BITS REGISTER	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	WDRUN	POR	-	-	WDIF	WTRF	EWRST	WDCLR	POR: X1xx 0000B External reset: Xxxx 0xx0B Watchdog reset: Xxxx 01x0B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	PWM1OE	PWM0OE	PCLK.1	PCLK.0	FP1	FP0	Xx00 0000B
PSW	PROGRAM STATUS WORD	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000B
NVMDATA	NVM DATA	CFH	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA.3	NVMDATA.2	NVMDATA.1	NVMDATA.0	0000 0000B
NVMCON	NVM CONTROL	CEH	EER	EWR	EnNVM	-	-	-	-	-	000x xxxxB
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000B
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000B
T2MOD	TIMER 2 MODE	C9H	-	-	-	ICEN0	T2CR	1	T2OE	DCEN	Xxx0 0100B
T2CON	TIMER 2 CONTROL	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL	0000 0000B
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B
NVMADDR	NVM LOW BYTE ADDRESS	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	0000 0000B
STATUS	STATUS REGISTER	C5H	-	-	-	-	-	-	SPTA0	SPRA0	Xxxx xx00B
PMR	POWER MANAGEMENT REGISTER	C4H	CD1	CD0	SWB	-	-	ALE-OFF	-	-	010x xxxxB
ROMMAP	ROMMAP REGISTER	C2H	WS	1	-	-	-	1	1	0	01xxx110B
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxxxxx0B

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
I2CON	I2C CONTROL REGISTER	C0H	-	ENSI	STA	STO	SI	AA	-	-	x00000xxB
I2TIMER	I2C TIMER COUNTER REGISTER	BFH	-	-	-	-	-	ENTI	DIV4	TIF	Xxxx x000B
I2CLK	I2C CLOCK RATE	BEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C STATUS	BDH	I2STATUS.7	I2STATUS.6	I2STATUS.5	I2STATUS.4	I2STATUS.3	I2STATUS.2	I2STATUS.1	I2STATUS.0	1111 1000B
I2DAT	I2C DATA	BCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxxxxxxB
SADEN	SLAVE ADDRESS MASK	B9H	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0	00000000B
IP0	INTERRUPT PRIORITY	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	Xx00 0000B
IP0H	INTERRUPT HIGH PRIORITY	B7H	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	Xx00 0000B
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	P1M2.6	P1M2.5	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	1111 1111B
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	1111 1111B
P3	PORT3	B0H	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	1111 1111B
			/RD	/WR	T1	T0	/INT1	/INT0	TXD	RXD	
SADDR	SLAVE ADDRESS	A9H	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0	0000 0000B
IE	INTERRUPT ENABLE	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0	0x00 0000B
P4	PORT4	A5H	-	-	-	-	P4.3	P4.2	P4.1	P4.0	Xxxx 1111B
CAPCON1	CAPTURE CONTROL 1	A4H	0	T0CC	-	-	ENF0	-	-	CPTF0	00xx 0xx0B
CAPCON0	CAPTURE CONTROL 0	A3H	-	-	-	-	CCT0.1	CCT0.0	-	-	Xxxx 00xxB
AUXR1	AUX FUNCTION REGISTER 1	A2H	KBF	BOD	BOI	LPBOV	SRST	BOV1	BOV0	BOS	0000 0000B
KBI	KEYBOARD INTERRUPT	A1H	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0	0000 0000B
P2	PORT 2	A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	1111 1111B
			A15	A14	A13	A12	A11	A10	A9	A8	
P3M2	PORT 3 OUTPUT MODE 2	9FH	P3M2.7	P3M2.6	P3M2.5	P3M2.4	P3M2.3	P3M2.2	P3M2.1	P3M2.0	CONFIG0.PMODE=1; 0000 0000B CONFIG0.PMODE=0; 1111 1111B

TIMER 2 CAPTURE MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

BIT	NAME	FUNCTION
7-0	RCAP2H	Timer 2 Capture MSB: This register is used to capture the TH2 value when a timer 2 is configured in capture mode. RCAP2H is also used as the MSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

TIMER 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

TIMER 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	EnNVM	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit: 0: Without erase NVM page(n). 1: Set this bit to erase page(n) of NVM. The NVM has **8** pages and each page have 16 bytes data memory. Initiate page select by programming NVMADDL registers, which will automatically enable page area. When user set this bit, the page erase process will begin and program counter will halt at this instruction. After the erase process is completed, program counter will continue executing next instruction.
6	EWR	NVM data write bit: 0: Without write NVM data.

The instruction timing for the N79E352(R) is an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the N79E352(R) and the standard 8052. In the N79E352(R) each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2 C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the N79E352(R) does one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the N79E352(R) are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8052, the MOVX instruction is always two machine cycles long. However in the N79E352(R), the user has a facility to stretch the duration of this instruction from 2 machine cycles to 9 machine cycles. The $\overline{RD}$ and $\overline{WR}$ strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. The rest of the instructions are either three, four or five machine cycle instructions. Note that in the N79E352(R), based on the number of machine cycles, there are five different types, while in the standard 8052 there are only three. However, in the N79E352(R) each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8052. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8052 in terms of clock periods.

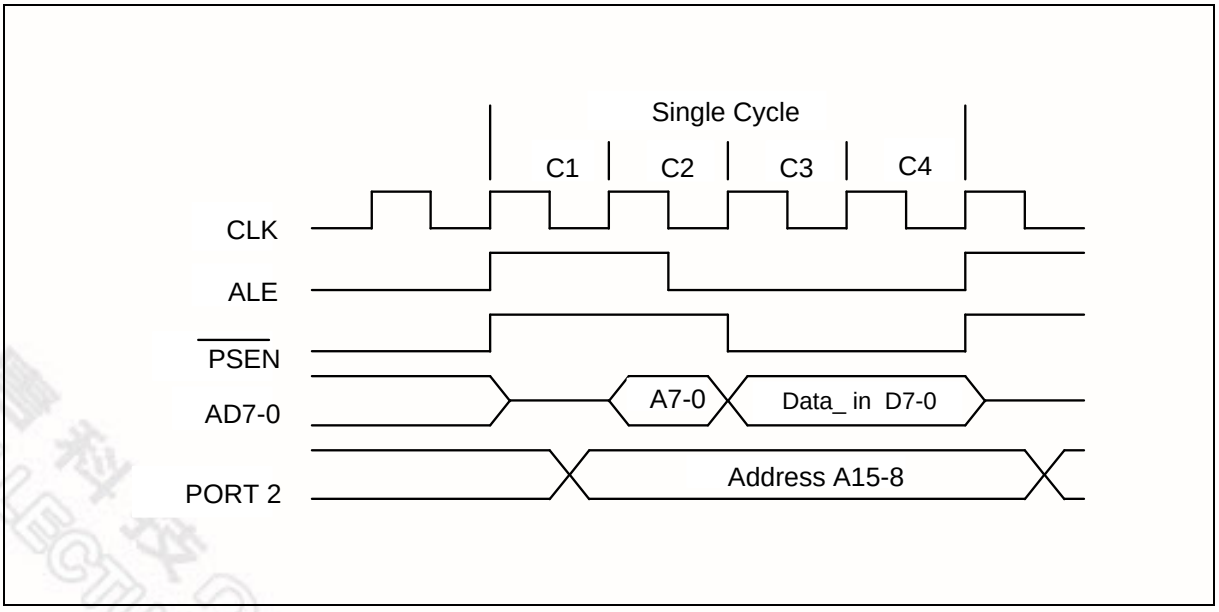


Figure 9-1: Single Cycle Instruction Timing

9.2 MOVX Instruction

The N79E352(R), like the standard 8052, uses the MOVX instruction to access external Data Memory. This Data Memory includes both off-chip memory as well as memory mapped peripherals. While the results of the MOVX instruction are the same as in the standard 8052, the operation and the timing of the strobe signals have been modified in order to give the user much greater flexibility.

The MOVX instruction is of two types, the MOVX @Ri and MOVX @DPTR. In the MOVX @Ri, the address of the external data comes from two sources. The lower 8-bits of the address are stored in the Ri register of the selected working register bank. The upper 8-bits of the address come from the port 2 SFR. In the MOVX @DPTR type, the full 16-bit address is supplied by the Data Pointer.

Since the N79E352(R) has two Data Pointers, DPTR and DPTR1, the user has to select between the two by setting or clearing the DPS bit. The Data Pointer Select bit (DPS) is the LSB of the DPS SFR, which exists at location 86h. No other bits in this SFR have any effect, and they are set to 0. When DPS is 0, then DPTR is selected, and when set to 1, DPTR1 is selected. The user can switch between DPTR and DPTR1 by toggling the DPS bit. The quickest way to do this is by the INC instruction. The advantage of having two Data Pointers is most obvious while performing block move operations. The accompanying code shows how the use of two separate Data Pointers speeds up the execution time for code performing the same task.

Block Move with single Data Pointer:

; SH and SL are the high and low bytes of Source Address
; DH and DL are the high and low bytes of Destination Address
; CNT is the number of bytes to be moved

			Machine Cycles of N79E352(R) #
MOV	R2, #CNT	; Load R2 with the count value	2
MOV	R3, #SL	; Save low byte of Source Address in R3	2
MOV	R4, #SH	; Save high byte of Source address in R4	2
MOV	R5, #DL	; Save low byte of Destination Address in R5	2
MOV	R6, #DH	; Save high byte of Destination address in R6	2
LOOP:			
MOV	DPL, R3	; Load DPL with low byte of Source address	2
MOV	DPH, R4	; Load DPH with high byte of Source address	2
MOVX	A, @DPTR	; Get byte from Source to Accumulator	2
INC	DPTR	; Increment Source Address to next byte	2
MOV	R3, DPL	; Save low byte of Source address in R3	2
MOV	R4, DPH	; Save high byte of Source Address in R4	2
MOV	DPL, R5	; Load low byte of Destination Address in DPL	2
MOV	DPH, R6	; Load high byte of Destination Address in DPH	2
MOVX	@DPTR, A	; Write data to destination	2
INC	DPTR	; Increment Destination Address	2
MOV	DPL, R5	; Save low byte of new destination address in R5	2
MOV	DPH, R6	; Save high byte of new destination address in R6	2
DJNZ	R2, LOOP	; Decrement count and do LOOP again if count <> 0	2

11. RESET CONDITIONS

The user has several hardware related options for placing the N79E352(R) into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 Sources of reset

11.1.1 External Reset

The device samples the RST pin every machine cycle during state C4. The RST pin must be held high for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as RST pin is high and remains high up to two machine cycles after RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

11.1.2 Power-On Reset (POR)

When the power supply rises to the configured level, V_{RST}, the device will perform a power on reset and set the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets.

11.1.3 Brown-Out Reset (BOR)

If the power supply falls below brownout voltage of V_{BOV}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a brownout reset.

11.1.4 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

11.1.5 Software Reset

N79E352(R) is enhanced by a software reset. This allows the program code to reset the whole system in software approach. Just writer 1 to SRET bit in AUXR1.3, a software reset will perform. Note that SRST require Timed Access procedure to write. Please refer TA register description

11.2 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

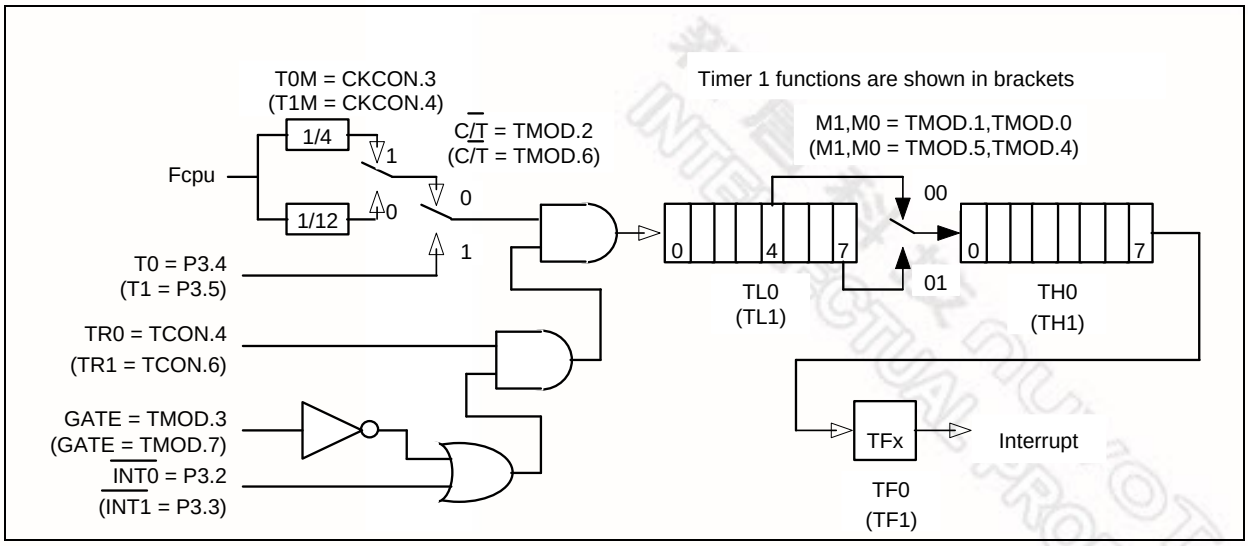


Figure 12-1: Timer/Counter Mode 0 & Mode 1

12.3.5 Programmable Clock-out

Timer 2 is equipped with a new clock-out feature which outputs a 50% duty cycle clock on P1.0. It can be invoked as a programmable clock generator. To configure Timer 2 with clock-out mode, software must initiate it by setting bit T2OE = 1, C/T2 = 0 and CP/RL = 0. Setting bit TR2 will start the timer. This mode is similar to the baud rate generator mode, it will not generate an interrupt while Timer 2 overflow. So it is possible to use Timer 2 as a baud rate generator and a clock generator at the same time. The clock-out frequency is determined by the following equation:

The Clock-Out Frequency = Oscillator Frequency / [4 X 65536-(RCAP2H, RCAP2L)]

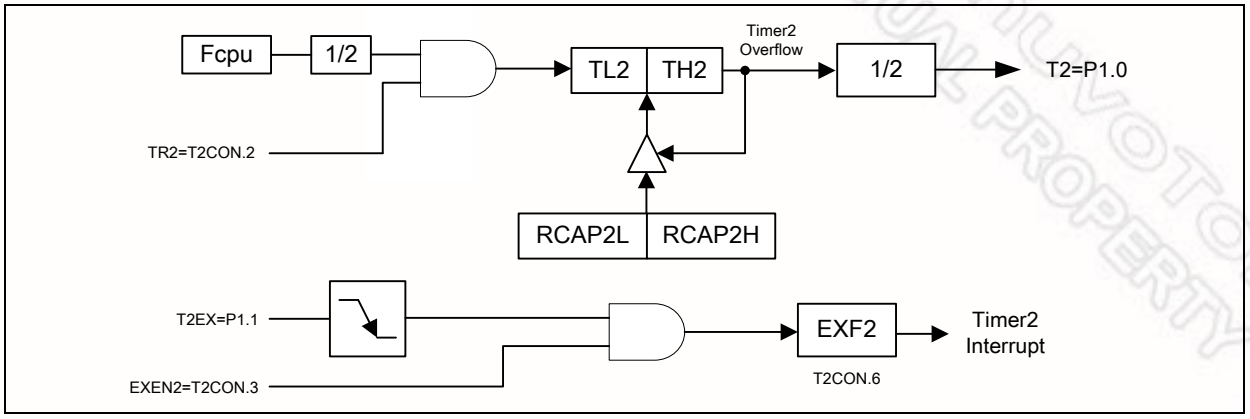


Figure 12-8: Programmable Clock-Out Mode

15. UART SERIAL PORT

Serial port in the N79E352(R) is a full duplex port. The N79E352(R) provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the N79E352(R) generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receive buffer register. The serial port can operate in four different modes as described below.

15.1 Mode 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the N79E352(R) whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This baud rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the N79E352(R).

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the N79E352(R) and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

17. TIMED ACCESS PROTECTION

The N79E352(R) has several new features, like the Watchdog timer, on-chip ROM size adjustment, wait state control signal and Power on/fail reset flag, which are crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the N79E352(R) has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access(TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG    0C7h          ; define new register TA, located at 0C7h
MOV     TA, #0AAh
MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below

Example 1: Valid access

```
MOV     TA, #0AAh          3 M/C
MOV     TA, #055h          3 M/C
MOV     WDCON, #00h        3 M/C
```

Note: M/C = Machine Cycles

Example 2: Valid access

```
MOV     TA, #0AAh          3 M/C
MOV     TA, #055h          3 M/C
NOP                        1 M/C
SETB    EWRST              2 M/C
```

Example 3: Valid access

```
MOV     TA, #0Aah          3 M/C
MOV     TA, #055h          3 M/C
ORL     WDCON, #00000010B  3M/C
```

Example 4: Invalid access

```
MOV     TA, #0AAh          3 M/C
MOV     TA, #055h          3 M/C
NOP                        1 M/C
NOP                        1 M/C
CLR     POR                2 M/C
```

Example 5: Invalid Access

```
MOV     TA, #0AAh          3 M/C
NOP                        1 M/C
```

18. INTERRUPTS

N79E352(R) has four priority level interrupts structure with 11 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

18.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1 (SFR TCON). The bits IE0 and IE1 in TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The timer 2 interrupt is generated through TF2 (timer 2 overflow/compare match). The hardware does not clear these flags when a timer 2 interrupt is executed.

The uart serial block can generate interrupt on reception or transmission. There are two interrupt sources from the uart block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

This device also provide an independent I2C serial port. When new I2C state is present in I2STATUS, the SI flag is set by hardware, and if EA and EI2 bits are both set, the I2C interrupt is requested. SI must be cleared by software.

Keyboard interrupt is generated when any of the keypad connected to P0 pins is pressed. Each keypad interrupt can be individually enabled or disabled. User will have to software clear the flag bit.

The input capture 0 interrupt is generated through CPTF0 flag. CPTF0 flag is set by input capture events. The hardware does not clear this flag when the capture interrupt is executed. Software has to clear the flag.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBO (EIE.6) and global interrupt enable are set.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003H	Timer 0 Overflow	000BH
External Interrupt 1	0013H	Timer 1 Overflow	001BH
Serial Port	0023H	Brownout Interrupt	002BH
I2C Interrupt	0033H	KBI Interrupt	003BH
Timer 2 Overflow	0043H	-	004BH
Watchdog Timer	0053H	-	005BH

23. OSCILLATOR

N79E352(R) provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 24MHz, and without capacitor or resister.

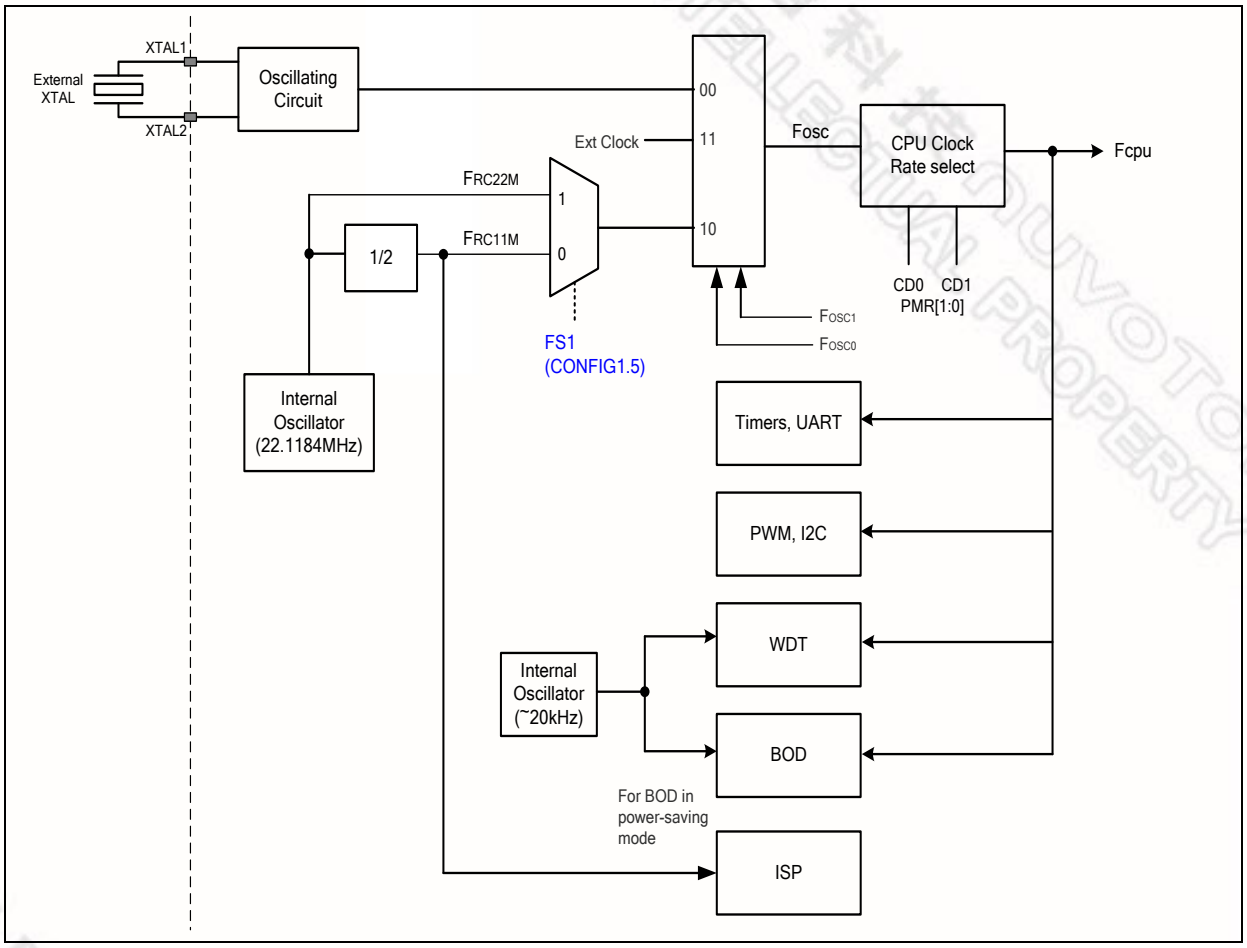


Figure 23-1: Oscillator

23.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is fixed at 11.0592MHz or 22.1184MHz (selectable by FS1 config bit) ±2% for N79E352R, ±25% for N79E352 frequency to support clock source. When FOSC1, FOSC0 = 01b, the On-Chip RC Oscillator is enabled.

23.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is ffrom 0Hz up to 24MHz.

The device supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the device. When enabled, via the ENCLK bit in the P5M1 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering

25. ICP(IN-CIRCUIT PROGRAM) FLASH PROGRAM

The ICP(In-Circuit-Program) mode is another approach to access the Flash EPROM. There are only 3 pins needed to perform the ICP function. One is mode input, shared with RST pin, which must be kept in Vdd voltage in the entire ICP working period. One is clock input, shared with P1.7, which accepts serial clock from external device. Another is data I/O pin, shared with P1.6, that an external ICP program tool shifts in/out data via P1.6 synchronized with clock(P1.7) to access the Flash EPROM of N79E352(R).

(Note, While PRHI=0, P1.6, P1.7 are still quasi high during reset period. During reset period , P1.6, P1.7 cann't switch to open-drain by setting config).

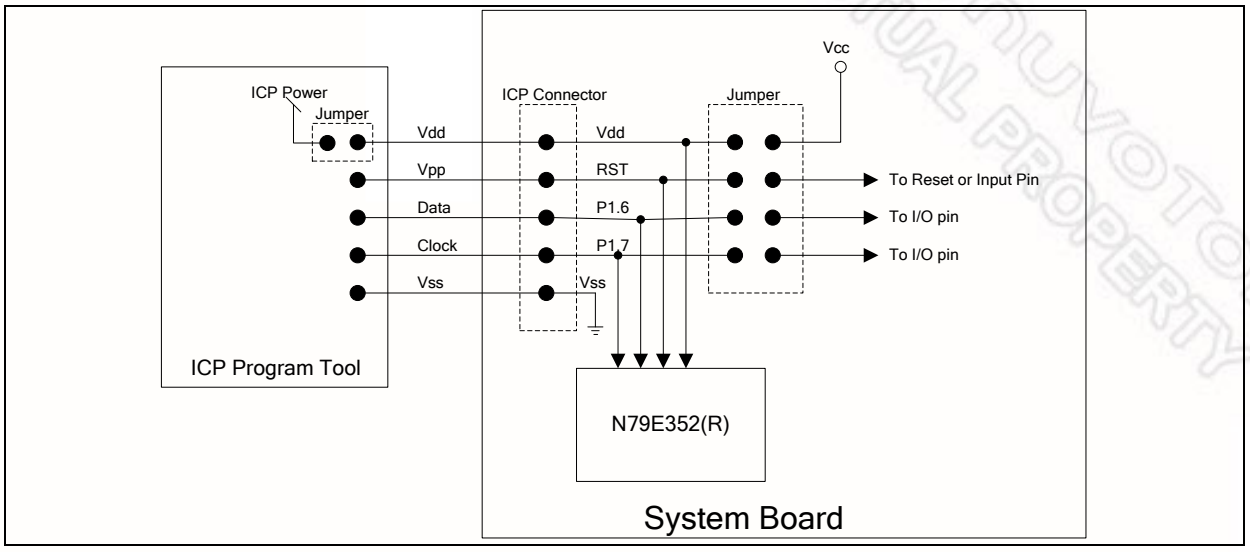


Figure 26-1: ICP Writer Tool connector pin assign

Note:

1. When using ICP to upgrade code, the RST, P1.6 and P1.7 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.
3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.
4. During ICP mode, all PWM pins will be tri-stated.

27.2 D.C. Characteristics

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4		5.5	V	V_{DD}=4.5V ~ 5.5V @ 24MHz V_{DD}=2.7V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 4MHz
Operating Current	I_{DD1}			5	mA	No load, RST = V_{DD}, V_{DD}= 3.0V @ 11.0592MHz
	I_{DD2}			15	mA	No load, RST = V_{DD}, V_{DD}= 5.0V @ 22.1184MHz
Idle Current	I_{IDLE}			4	mA	No load, V_{DD} = 3.0V @ 11.0592MHz
Power Down Current	I_{PWDN}		1	5	µA	No load, V_{DD} = 5.5V @ Disable BOV function
			1	5	uA	No load, V_{DD} = 3.0V @ Disable BOV function
Input / Output						
Input Current P0, P1, P2, P3, P4, P5	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current P1.5(RST pin)[1]	I_{IN2}	-48	-32	-24	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2, P3, P5 (Open Drain)	I_{LK}	-10	-	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4, P5	I_{TL} [*3]	-450	-	-246	µA	V_{DD} = 5.5V, V_{IN}<2.0V
		-93	-	-56		V_{DD}=2.4 Vin = 1.3v
Input Low Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6 1.0		V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 2.4V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		0.2V_{DD}		V	
Input Low Voltage RST [*1]	V_{IL21}	-	1.0	1.6	V	V_{DD}=4.5V

27.3.8 I2C Bus Timing Characteristics

PARAMETER	SYMBOL	Standard Mode I2C Bus		UNIT
		Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	uS
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{Hd;STA}$	4.0	-	uS
Low period of the SCL clock	t_{LOW}	4.7	-	uS
HIGH period of the SCL clock	t_{HIGH}	4.0	-	uS
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	uS
Data hold time	$t_{HD;DAT}$	5.0	-	uS
Data set-up time	$t_{SU;DAT}$	250	-	nS
Rise time of both SDA and SCL signals	t_r	-	1000	nS
Fall time of both SDA and SCL signals	t_f	-	300	nS
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	uS
Capacitive load for each bus line	C_b	-	400	pF

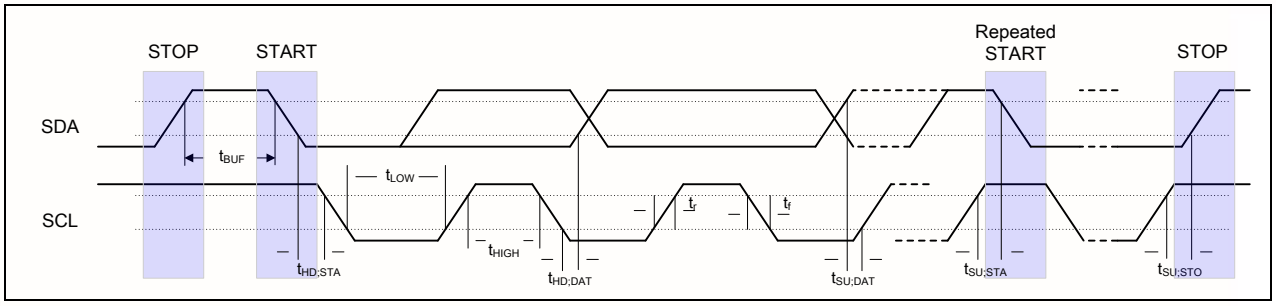


Figure 26-5: I2C Bus Timing

EXPLANATION OF LOGIC SYMBOLS

In order to maintain compatibility with the original 8051 family, this device specifies the same parameter as such device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{PSEN}$
Q	Output Data	R	$\overline{RD}$ signal
V	Valid	W	$\overline{WR}$ signal
X	No longer a valid state	Z	Tri-state

29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Aug, 14, 2008	-	Initial Issued
A02	Aug, 21, 2008	7,8	Update pin configurations.
A03	Feb, 2, 2009	-	Add access external memory diagram
A04	Feb, 9, 2009	-	Modify the part no. with each package 1. 40DIP: N79E352ADG, N79E352RADG 2. 44PLCC: N79E352APG, N79E352RAPG 3. 44PQFP: N79E352AFG, N79E352RAFG 4. 48LQFP: N79E352ALG, N79E352RALG
A05	Apr, 22, 2009	- 108~109 124~125 115	1. Correct typo errors. 2. Release input capture 0 function in Section 20. 3. Re-arrange section sequency after Section 20. 2. Update D.C specification. 3. Renew Figure 0-1: Oscillator
A06	Jul, 29, 2009	119	1. Add ICP description.

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