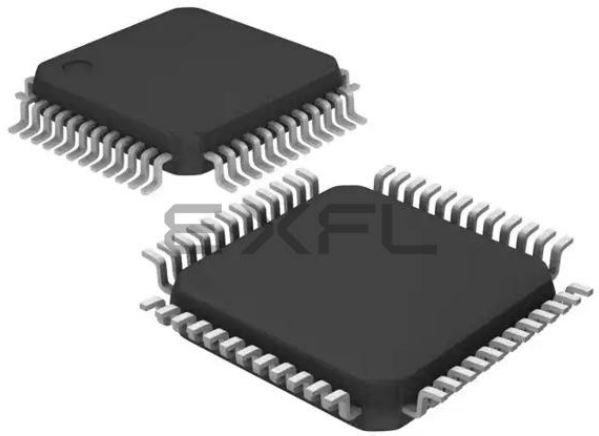
Nuvoton Technology Corporation - N79E352RALG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e352ralg

SMOD	SMOD0	BOF	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	-	Reserved.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	WD1~0	Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period. WD1 WD0 Interrupt time-out Reset time-out 0 0 2^6 $2^6 + 512$ 0 1 2^9 $2^9 + 512$ 1 0 2^{13} $2^{13} + 512$ 1 1 2^{15} $2^{15} + 512$

-	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0

Mnemonic: NVMADDR Address: C6h

BIT	NAME	FUNCTION
7	-	Reserved
6~0	NVMADDR.[6:0]	The NVM address: The register indicates NVM data memory address on On-Chip code memory space.

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

TIMER 2 CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / $\overline{T2}$	CP / $\overline{RL2}$

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down count mode. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.
6	EXF2	Timer 2 External Flag: A negative transition on the T2EX pin (P1.1) or timer 2 overflow will cause this flag to set based on the CP / $\overline{RL2}$, EXEN2 and DCEN bits. If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on T2EX pin will force a timer interrupt if enabled.
5	RCLK	Receive Clock Flag: This bit determines the serial port time-base when receiving data in serial modes 1 or 3. If it is 0, then timer 1 overflow is used for baud rate generation, otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.

INPUT CAPTURE 0 HIGH REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0

Mnemonic: CCH0 Address: E4h

BIT	NAME	FUNCTION
7-0	CCH0	Capture 0 high byte.

IINTERRUPT ENABLE REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	ECPTF	EBO	-	EWDI	-	-	EKB	EI2

Mnemonic: EIE Address: E8h

BIT	NAME	FUNCTION
7	ECPTF	0: Disable capture interrupt. 1: Enable capture interrupt.
6	EBO	Enable brownout interrupt. 0: Disable brownout interrupt. 1: Enable brownout interrupt.
5	-	Reserved.
4	EWDI	0: Disable Watchdog Timer Interrupt. 1: Enable Watchdog Timer Interrupt.
3~2	-	Reserved.
1	EKB	0: Disable Keypad Interrupt. 1: Enable Keypad Interrupt.
0	EI2	0: Disable I2C Interrupt. 1: Enable I2C Interrupt.

KEYBOARD LEVEL

Bit:	7	6	5	4	3	2	1	0
	KBL.7	KBL.6	KBL.5	KBL.4	KBL.3	KBL.2	KBL.1	KBL.0

Mnemonic: KBL Address: E9h

BIT	NAME	FUNCTION
7~0	KBL.7~0	Keyboard trigger level. 0: Low level trigger.x pin. 1: High level trigger on KBI.x pin. [x = 0-7]

PORTS SHMITT REGISTER

Bit:	7	6	5	4	3	2	1	0

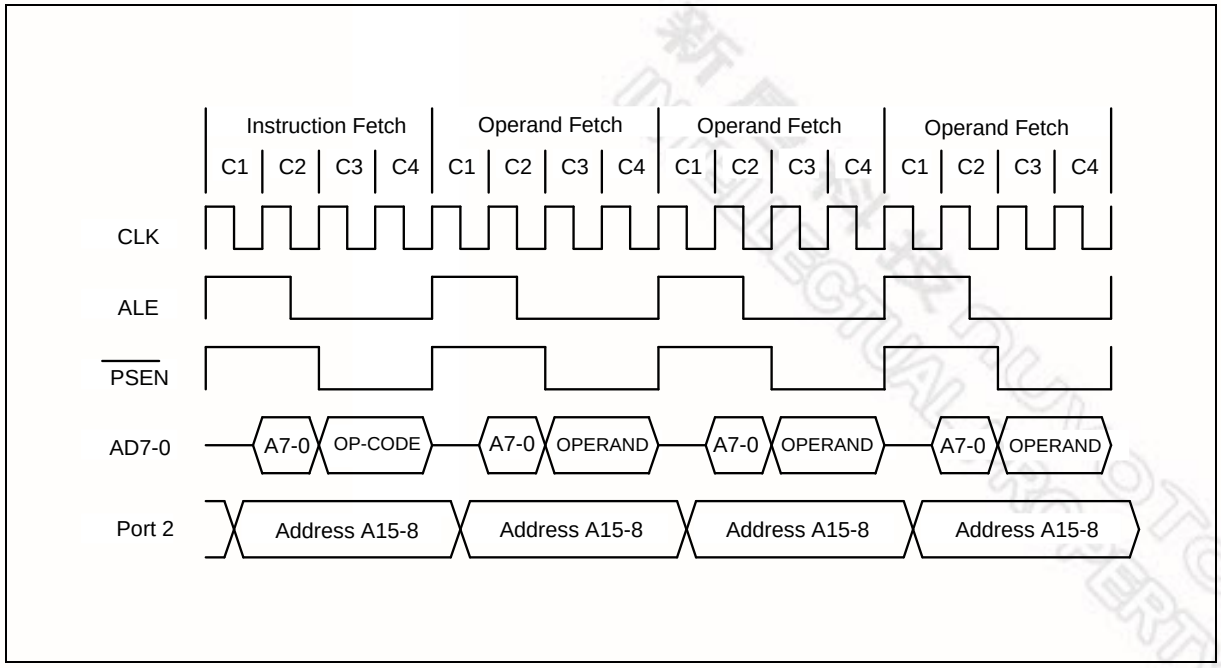


Figure 9-4: Four Cycle Instruction Timing

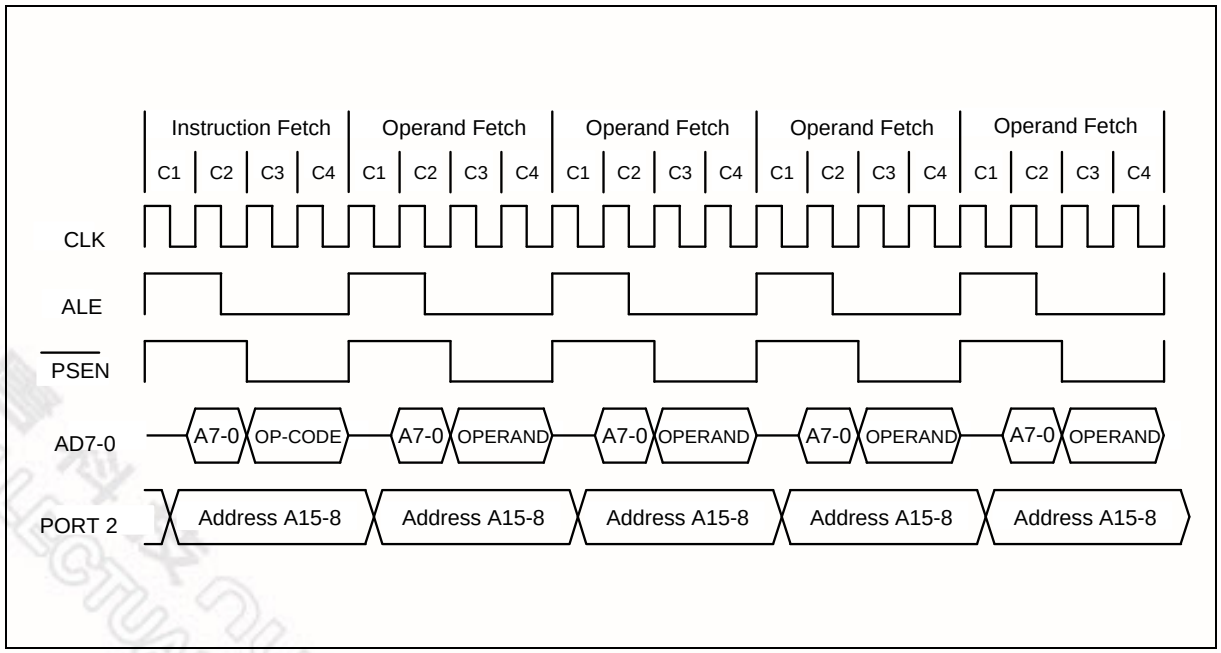


Figure 9-5: Five Cycle Instruction Timing

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2V, the minimum operating voltage for the RAM. If VDD falls below 2V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset.

	External reset	Watchdog reset	Power on reset
WDCON	0xxx0x00b	0xxx0100b	01xx0000b

The POR bit WDCON.6 is set only by the power on reset. WTRF bit WDCON.2 is set when the Watchdog timer causes a reset. A power on reset will also clear this bit. The EWRST bit WDCON.1 is cleared by all reset. This disables the Watchdog timer resets.

All the bits in this SFR have unrestricted read access. WDRUN, POR, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses.

12. PROGRAMMABLE TIMERS/COUNTERS

The N79E352(R) has three 16-bit programmable timer/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other two timers.

12.1 Timer/Counters 0 & 1

Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

12.2 Time-base Selection

The N79E352(R) gives the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the N79E352(R) and the standard 8051 can be matched. This is the default mode of operation of the N79E352(R) timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bits in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

12.2.1 Mode 0

In Mode 0, the timer/counters act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer/counter. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. When $C/\overline{T}$ is set to 0, then it will count clock cycles, and if $C/\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur. Note that when used as a timer, the time-base may be either clock cycles/12 or clock cycles/4 as selected by the bits TxM of the CKCON SFR.

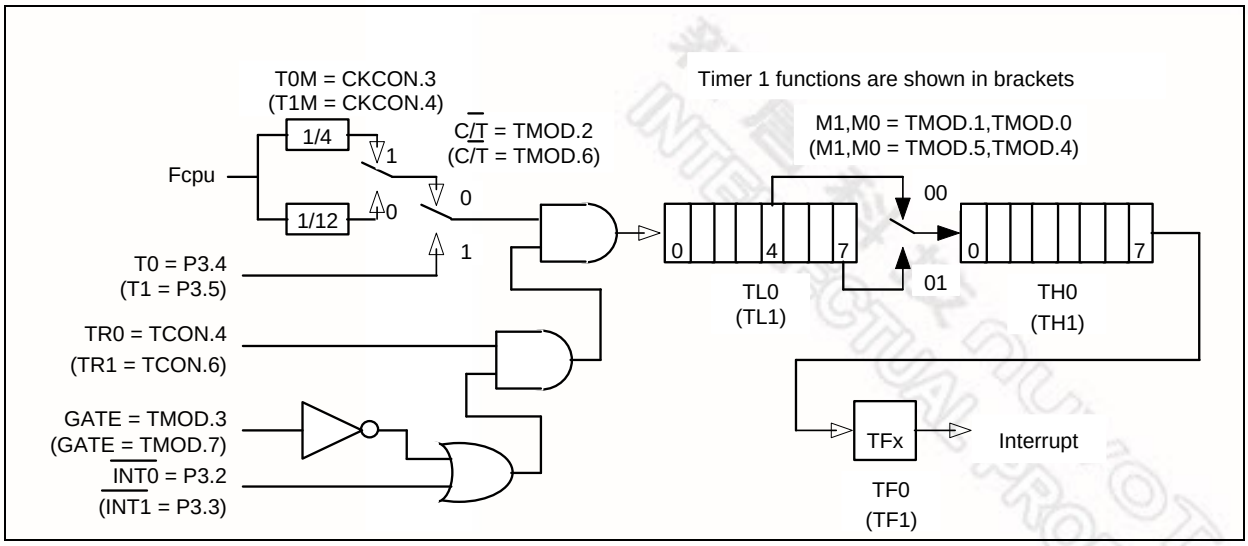


Figure 12-1: Timer/Counter Mode 0 & Mode 1

12.2.2 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16 bit counter, rather than a 13 bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

12.2.3 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

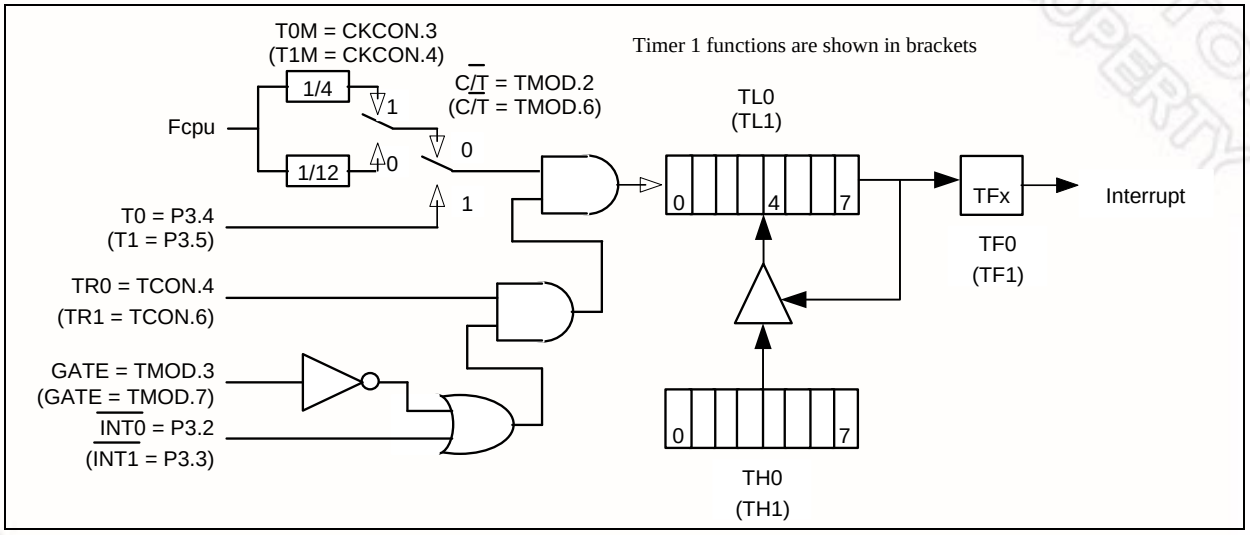


Figure 12-2: Timer/Counter Mode 2

12.2.4 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits C / $\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2., but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

16.2 The I2C Control Registers:

The I2C has 1 control register (I2CON) to control the transmit/receive flow, 1 data register (I2DAT) to buffer the Tx/Rx data, 1 status register (I2STATUS) to catch the state of Tx/Rx, recognizable slave address register for slave mode use and 1 clock rate control block for master mode to generate the variable baud rate.

16.2.1 The Address Registers, I2ADDR

I2C port is equipped with one slave address register. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR are matched with the received slave address.

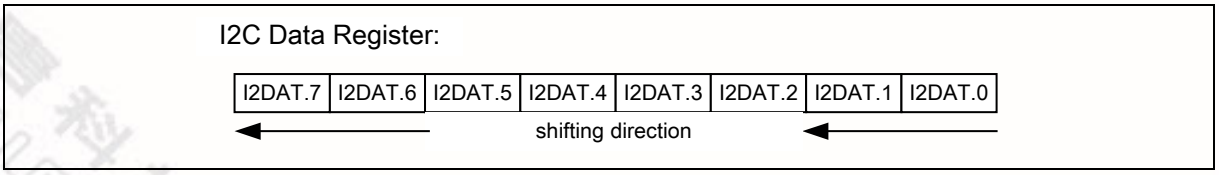
The I2C ports support the "General Call" function. If the GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

When GC bit is set, the I2C is in Slave mode, it can be received the general call address by 00H after Master send general call address to I2C bus, then it will follow status of GC mode. If it is in Master mode, the AA bit must be cleared when it will send general call address of 00H to I2C bus.

16.2.2 The Data Register, I2DAT

This register contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from or write to this 8-bit directly addressable SFR while it is not in the process of shifting a byte. This occurs when the bus is in a defined state and the serial interrupt flag (SI) is set. Data in I2DAT remains stable as long as SI bit is set. While data is being shifted out, data on the bus is simultaneously being shifted in; I2DAT always contains the last data byte present on the bus. Thus, in the event of arbitration lost, the transition from master transmitter to slave receiver is made with the correct data in I2DAT.

I2DAT and the acknowledge bit form a 9-bit shift register, the acknowledge bit is controlled by the hardware and cannot be accessed by the CPU. Serial data is shifted through the acknowledge bit into I2DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2DAT, the serial data is available in I2DAT, and the acknowledge bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I2DAT on the falling edges of SCL clock pulses, and is shifted into I2DAT on the rising edges of SCL clock pulses.



16.3.3 Slave Receiver Mode

Serial data and the serial clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

16.3.4 Slave Transmitter Mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via SDA while the serial clock is input through SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

16.4 Data Transfer Flow in Five Operating Modes

The five operating modes are: Master/Transmitter, Master/Receiver, Slave/Transmitter, Slave/Receiver and GC Call. Bits STA, STO and AA in I2CON register will determine the next state of the I2C hardware after SI flag is cleared. Upon complexion of the new action, a new status code will be updated and the SI flag will be set. If the I2C interrupt control bits (EA and EI2) are enable, appropriate action or software branch of the new status code can be performed in the Interrupt service routine.

Data transfers in each mode are shown in the following figures.

*** Legend for the following five figures:

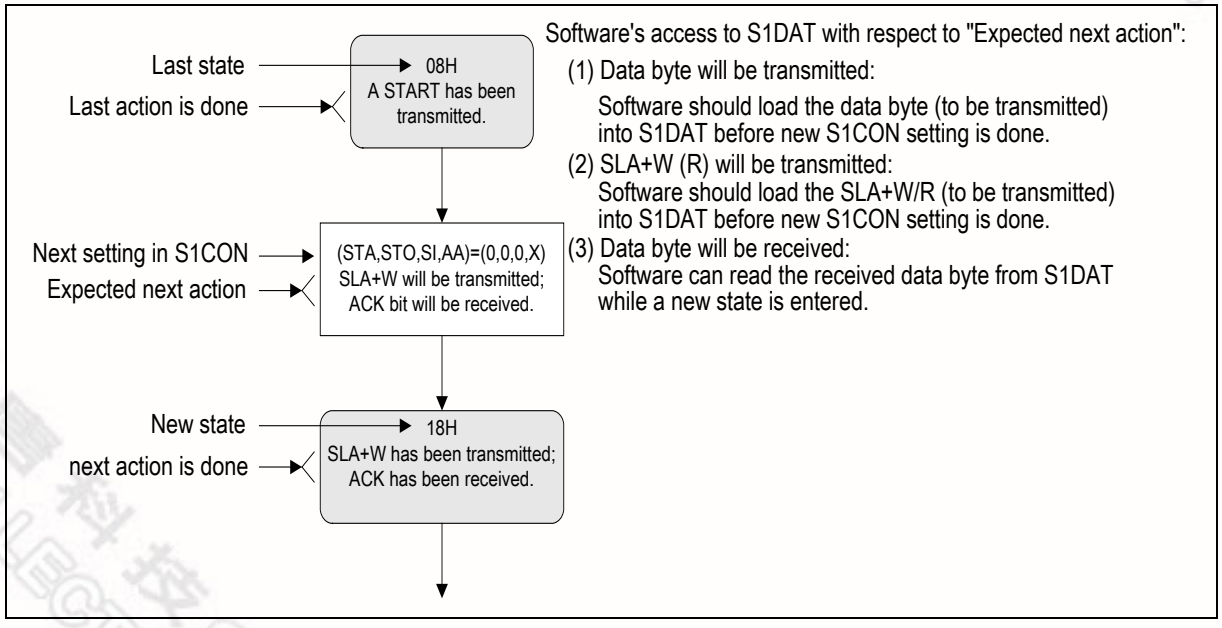


Figure 16-3: Legen for the following four figures

18. INTERRUPTS

N79E352(R) has four priority level interrupts structure with 11 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

18.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1 (SFR TCON). The bits IE0 and IE1 in TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The timer 2 interrupt is generated through TF2 (timer 2 overflow/compare match). The hardware does not clear these flags when a timer 2 interrupt is executed.

The uart serial block can generate interrupt on reception or transmission. There are two interrupt sources from the uart block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

This device also provide an independent I2C serial port. When new I2C state is present in I2STATUS, the SI flag is set by hardware, and if EA and EI2 bits are both set, the I2C interrupt is requested. SI must be cleared by software.

Keyboard interrupt is generated when any of the keypad connected to P0 pins is pressed. Each keypad interrupt can be individually enabled or disabled. User will have to software clear the flag bit.

The input capture 0 interrupt is generated through CPTF0 flag. CPTF0 flag is set by input capture events. The hardware does not clear this flag when the capture interrupt is executed. Software has to clear the flag.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBO (EIE.6) and global interrupt enable are set.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003H	Timer 0 Overflow	000BH
External Interrupt 1	0013H	Timer 1 Overflow	001BH
Serial Port	0023H	Brownout Interrupt	002BH
I2C Interrupt	0033H	KBI Interrupt	003BH
Timer 2 Overflow	0043H	-	004BH
Watchdog Timer	0053H	-	005BH

	0063H	Input Capture 0 Interrupt	006BH

Table 18- 1: N79E352(R) interrupt vector table

18.2 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low and lowest. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table 18- 2: Four-level interrupts priority.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being execute.

3. The current instruction does not involve a write to IE, EIE, IP0, IP0H, IP1 or IPH1 registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on Table 18- 3: Summary of interrupt sources. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

N79E352(R) uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the interrupt sources.

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPXH	IPX	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 18- 2: Four-level interrupts priority

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE or EIE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table below summarizes the interrupt sources, flag bits, vector address, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Enable bit	Flag cleared by	Priority bit	Arbitration ranking	Power-down wakeup
External Interrupt 0	IE0	0003H	EX0 (IE.0)	Hardware, Software	IP0H.0, IP0.0	1(highest)	Yes
Brownout Detect	BOF	002BH	EBO (EIE.6)	Hardware	IP1H.6, IP1.6	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (EIE.4)	Software	IP1H.4, IP1.4	3	Yes
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	Hardware, Software	IP0H.1, IP0.1	4	No
I2C Interrupt	SI + TIF	0033h	EI2 (EIE.0)	Software	IP1H.0, IP1.0	5	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	Hardware, Software	IP0H.2, IP0.2	6	Yes
KBI	KBF	003BH	EKB (EIE.1)	Software	IP1H.1, IP1.1	7	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	Hardware, Software	IP0H.3, IP0.3	8	No
UART	RI + TI	0023H	ES (IE.4)	Software	IP0H.4, IP0.4	9	No

The default port output configuration for standard N79E352(R) I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again. The quasi-bidirectional port configuration is shown as below.

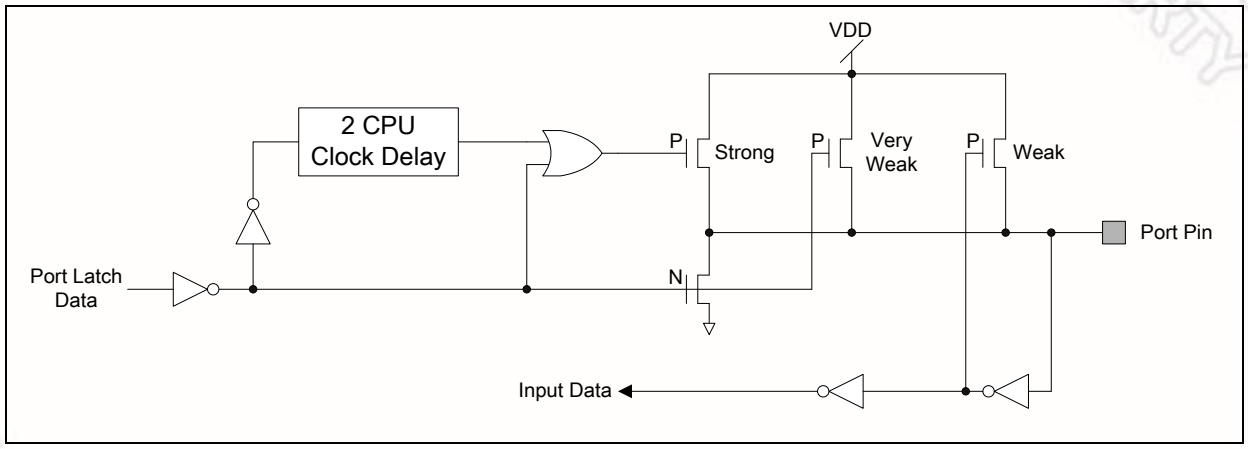


Figure 22-1: Quasi-Bidirectional Output

22.2 Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to VDD. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open drain port configuration is shown as below.

27.2 D.C. Characteristics

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4		5.5	V	V_{DD}=4.5V ~ 5.5V @ 24MHz V_{DD}=2.7V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 4MHz
Operating Current	I_{DD1}			5	mA	No load, RST = V_{DD}, V_{DD}= 3.0V @ 11.0592MHz
	I_{DD2}			15	mA	No load, RST = V_{DD}, V_{DD}= 5.0V @ 22.1184MHz
Idle Current	I_{IDLE}			4	mA	No load, V_{DD} = 3.0V @ 11.0592MHz
Power Down Current	I_{PWDN}		1	5	µA	No load, V_{DD} = 5.5V @ Disable BOV function
			1	5	uA	No load, V_{DD} = 3.0V @ Disable BOV function
Input / Output						
Input Current P0, P1, P2, P3, P4, P5	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current P1.5(RST pin)[1]	I_{IN2}	-48	-32	-24	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2, P3, P5 (Open Drain)	I_{LK}	-10	-	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4, P5	I_{TL} [*3]	-450	-	-246	µA	V_{DD} = 5.5V, V_{IN}<2.0V
		-93	-	-56		V_{DD}=2.4 Vin = 1.3v
Input Low Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6 1.0		V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 2.4V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		0.2V_{DD}		V	
Input Low Voltage RST [*1]	V_{IL21}	-	1.0	1.6	V	V_{DD}=4.5V

27.3.1 External Clock Characteristics

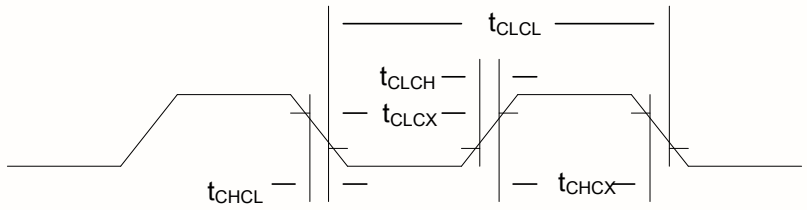
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	22.6	-	-	nS	
Clock Low Time	t_{CLCX}	22.6	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

27.3.2 AC Specification

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	24	MHz

27.3.3 External clock Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	12.5			ns	
Clock Low Time	t_{CLCX}	12.5			ns	
Clock Rise Time	t_{CLCH}			10	ns	
Clock Fall Time	t_{CLCL}			10	ns	



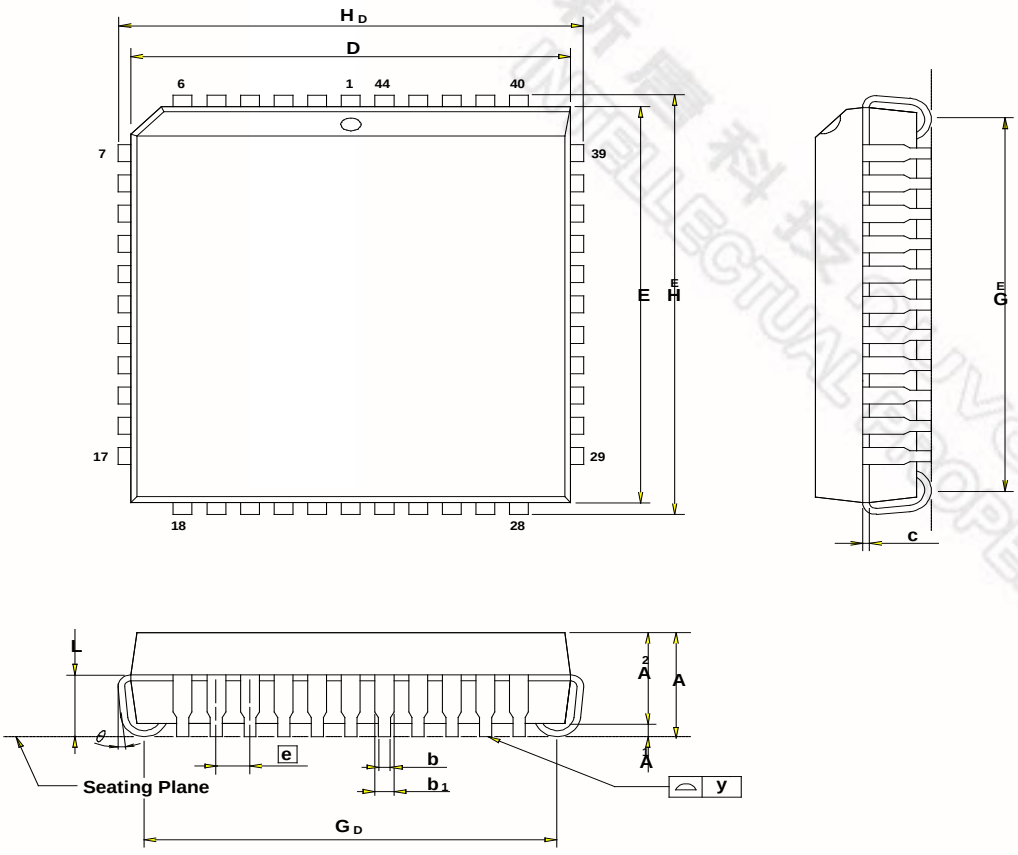
Note: Duty cycle is 50%

Figure 26-1 External clock characteristics

27.3.4 Serial Port Mode 0 Timing Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XLXL}		 12 t_{CLCL} 4 t_{CLCL}		ns	
Output Data Setup to Clock Rising Edge SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{QVXH}		 10 t_{CLCL} 3 t_{CLCL}		ns	

28.2 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Aug, 14, 2008	-	Initial Issued
A02	Aug, 21, 2008	7,8	Update pin configurations.
A03	Feb, 2, 2009	-	Add access external memory diagram
A04	Feb, 9, 2009	-	Modify the part no. with each package 1. 40DIP: N79E352ADG, N79E352RADG 2. 44PLCC: N79E352APG, N79E352RAPG 3. 44PQFP: N79E352AFG, N79E352RAFG 4. 48LQFP: N79E352ALG, N79E352RALG
A05	Apr, 22, 2009	- 108~109 124~125 115	1. Correct typo errors. 2. Release input capture 0 function in Section 20. 3. Re-arrange section sequency after Section 20. 2. Update D.C specification. 3. Renew Figure 0-1: Oscillator
A06	Jul, 29, 2009	119	1. Add ICP description.

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