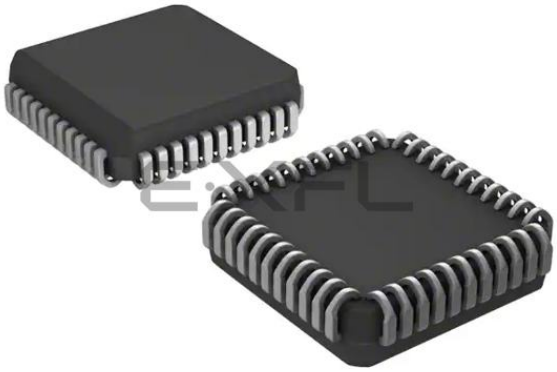

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Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n79e352rapg

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1. GENERAL DESCRIPTION

The N79E352(R) is an 8-bit Turbo 51 microcontroller which has Flash EPROM programmable hardware writer. The instruction set of the N79E352(R) is fully compatible with the standard 8052. The N79E352(R) contains a 8Kbytes of main Flash EPROM; a 256 bytes of RAM; 128 bytes NVM Data Flash EPROM; three 16-bit timer/counters; 2-channel 8-bit PWM; 1-channel UART and 1 additional input capture. These peripherals are supported by 11 interrupt sources four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the N79E352(R) allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security. N79E352(R) is designed for cost effective applications which can serve industrial devices, and other low power applications.

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
IP1	INTERRUPT PRIORITY 1	F8H	PCAP	PBO	-	PWDI	-	-	PKB	PI2	00x0 xx00B
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PBOH	-	PWDIH	-	-	PKBH	PI2H	00x0 xx00B
B	B REGISTER	F0H	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	0000 0000B
P5M2	PORT 5 OUTPUT MODE 2	EEH	-	-	-	-	-	-	P5M2.1	P5M2.0	CONFIG0.PMODE=1; Xxxx xx00B CONFIG0.PMODE=0; Xxxx xx11B
P5M1	PORT 5 OUTPUT MODE 1	EDH	-	-	-	-	-	ENCLK	P5M1.1	P5M1.0	CONFIG0.PMODE=1; Xxxx x000B CONFIG0.PMODE=0; Xxxx x011B
PORTS	PORT SHMITT REGISTER	ECH	-	-	P5S	-	P3S	P2S	P1S	P0S	xx0x 0000B
KBL	KEYBOARD LEVEL REGISTER	E9H	KBL.7	KBL.6	KBL.5	KBL.4	KBL.3	KBL.2	KBL.1	KBL.0	0000 0000B
EIE	INTERRUPT ENABLE 1	E8H	ECPTF	EBO	-	EWDI	-	-	EKB	EI2	00x0 xx00B
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000B
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000B
ACC	ACCUMULATOR	E0H	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	0000 0000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	-	-	CLRPWM	-	-	-	-	0xx0 xxxxB
PWM1L	PWM 1 LOW BITS REGISTER	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	WDRUN	POR	-	-	WDIF	WTRF	EWRST	WDCLR	POR: X1xx 0000B External reset: Xxxx 0xx0B Watchdog reset: Xxxx 01x0B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	PWM1OE	PWM0OE	PCLK.1	PCLK.0	FP1	FP0	Xx00 0000B
PSW	PROGRAM STATUS WORD	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000B
NVMDATA	NVM DATA	CFH	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA.3	NVMDATA.2	NVMDATA.1	NVMDATA.0	0000 0000B
NVMCON	NVM CONTROL	CEH	EER	EWR	EnNVM	-	-	-	-	-	000x xxxxB
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000B
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000B
T2MOD	TIMER 2 MODE	C9H	-	-	-	ICEN0	T2CR	1	T2OE	DCEN	Xxx0 0100B
T2CON	TIMER 2 CONTROL	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL	0000 0000B
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B
NVMADDR	NVM LOW BYTE ADDRESS	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	0000 0000B
STATUS	STATUS REGISTER	C5H	-	-	-	-	-	-	SPTA0	SPRA0	Xxxx xx00B
PMR	POWER MANAGEMENT REGISTER	C4H	CD1	CD0	SWB	-	-	ALE-OFF	-	-	010x xxxxB
ROMMAP	ROMMAP REGISTER	C2H	WS	1	-	-	-	1	1	0	01xxx110B
I2ADDR	I2C ADDRESS1	C1H	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxxxxx0B

		$\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	WD1~0	Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period. WD1 WD0 Interrupt time-out Reset time-out 0 0 2^6 $2^6 + 512$ 0 1 2^9 $2^9 + 512$ 1 0 2^{13} $2^{13} + 512$ 1 1 2^{15} $2^{15} + 512$

BIT	NAME	FUNCTION
3	P1.3	SCL or I/O pin by alternative.
2	P1.2	SDA or I/O pin by alternative.
1	P1.1	T2EX or I/O pin by alternative.
0	P1.0	T2 or I/O pin by alternative.

PORT 5

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P5.1/ XTAL1	P5.0/ XTAL2/ CLKOUT

Mnemonic: P5 Address: 94h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1	P5.1	XTAL1 clock input or I/O pin by alternative.
0	P5.0	XTAL2 or CLKOUT pin or I/O pin by alternative.

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is

3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

I2C DATA REGISTER

Bit:	7	6	5	4	3	2	1	0
	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0

Mnemonic: I2DAT Address: BCh

BIT	NAME	FUNCTION
7-0	I2DAT.[7:0]	The data register of I2C.

I2C STATUS REGISTER

Bit:	7	6	5	4	3	2	1	0
	I2STATUS.7	I2STATUS.6	I2STATUS.5	I2STATUS.4	I2STATUS.3	-	-	-

Mnemonic: I2STATUS Address: BDh

BIT	NAME	FUNCTION
7-0	I2STATUS.[7:0]	The status register of I2C: The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. In addition, states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

I2C BAUD RATE CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0

Table 9-2: Instruction Timing for N79E352(R)

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5

Instruction Timing for N79E352(R), continued

Instruction	HEX Op-Code	Bytes	N79E352(R) Machine Cycles	N79E352(R) Clock Cycles	8052 Clock Cycles	N79E352(R) vs. 8052 Speed Ratio
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
JMP @A+DPTR	73	1	2	8	24	3
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
LCALL addr16	12	3	4	16	24	1.5
LJMP addr16	02	3	4	16	24	1.5
MUL AB	A4	1	5	20	48	2.4
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3

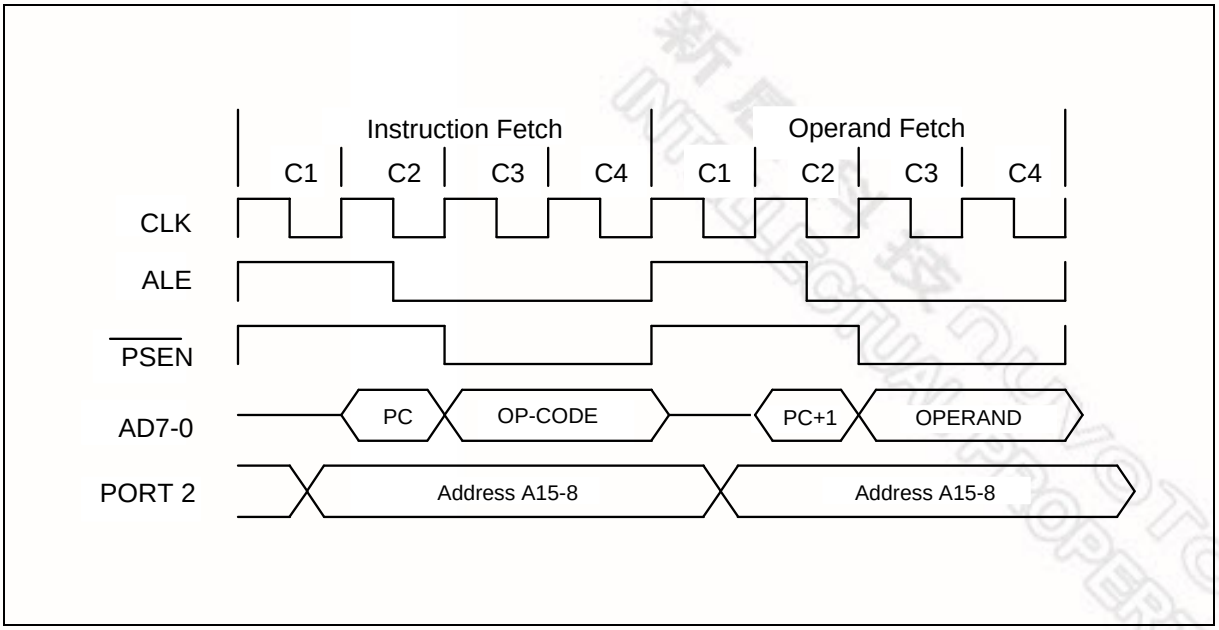


Figure 9-2: Two Cycle Instruction Timing

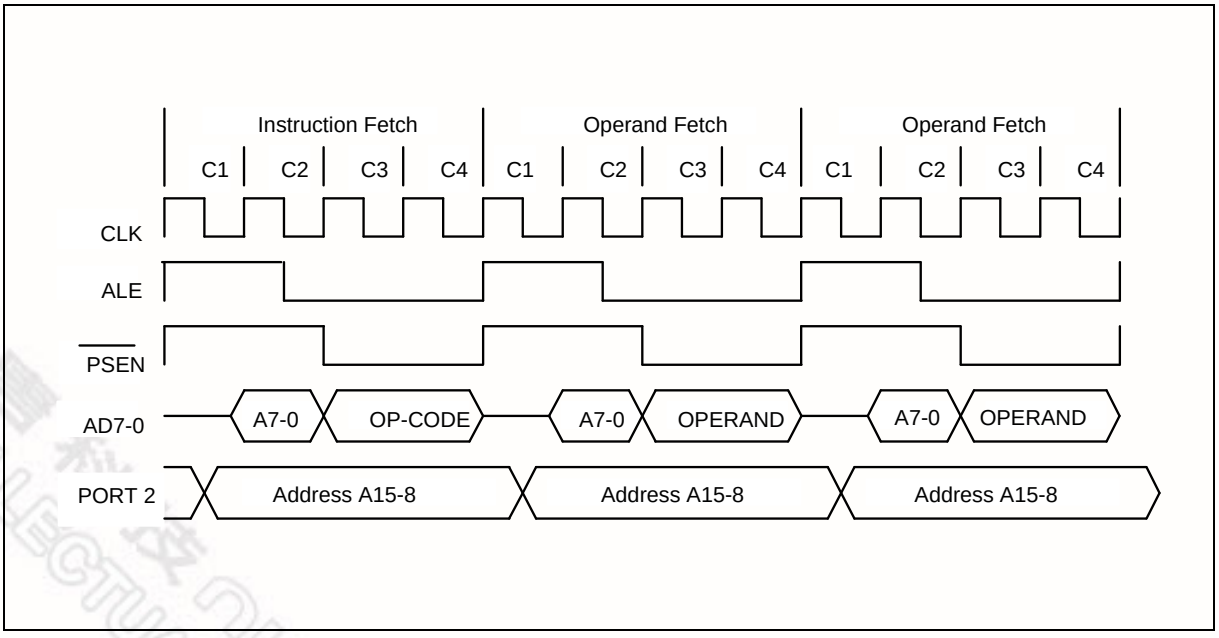


Figure 9-3: Three Cycle Instruction Timing

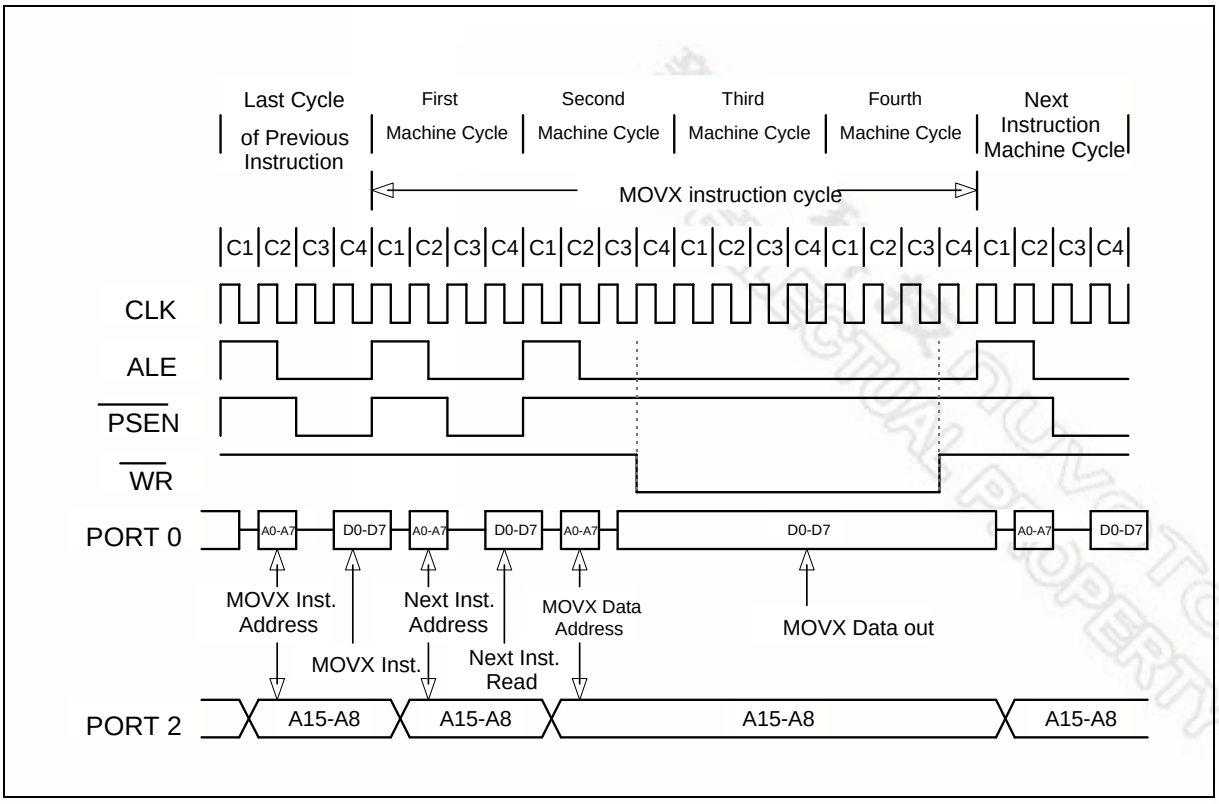


Figure 9-8: Data Memory Write with Stretch Value = 2

9.4 Wait State Control Signal

Either with the software using stretch value to change the required machine cycle of MOVX instruction, the N79E352(R) provides another hardware signal $\overline{\text{WAIT}}$ to implement the wider duration of external data access timing. This wait state control signal is the alternate function of P4.0. The wait state control signal can be enabled by setting WS (SFR ROMMAP.7) bit. When enabled, the setting of stretch value decides the minimum length of MOVX instruction cycle and the device will sample the $\overline{\text{WAIT}}$ pin at each C2 state before the rising edge of read/write strobe signal during MOVX instruction. Once this signal being recongnized, one more machine cycle (wait state cycle) will be inserted into next cycle. The inserted wait state cycles are unlimited, so the MOVX instruction cycle will end in which the wait state control signal is deactivated. Using wait state control signal allows a dynamically access timimg to a selected external peripheral. The WS bit is accessed by the Timed Access Protection procedure.

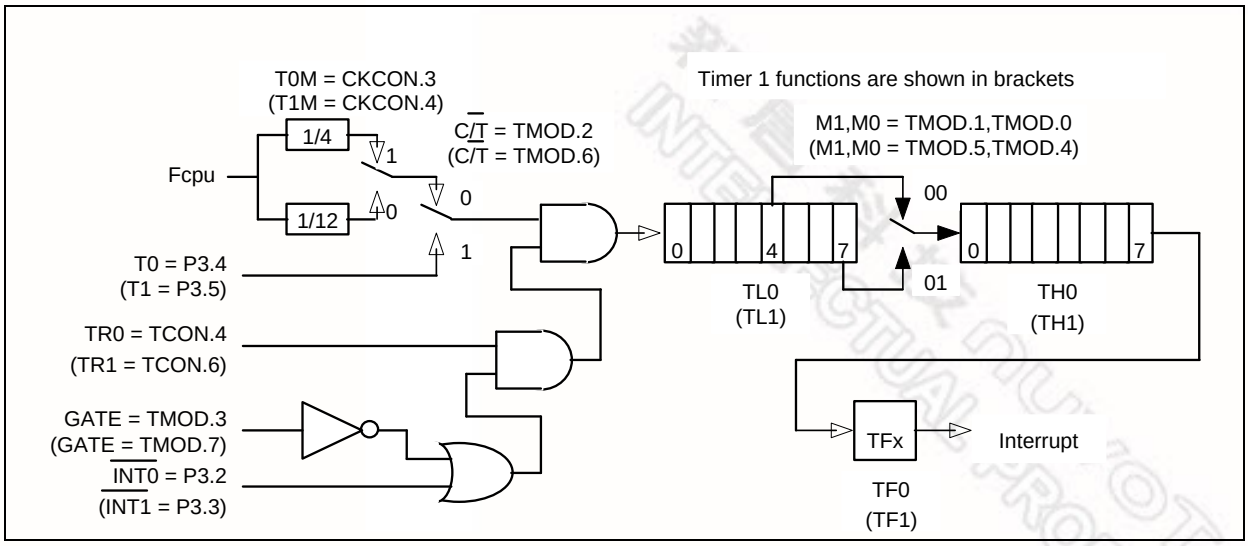


Figure 12-1: Timer/Counter Mode 0 & Mode 1

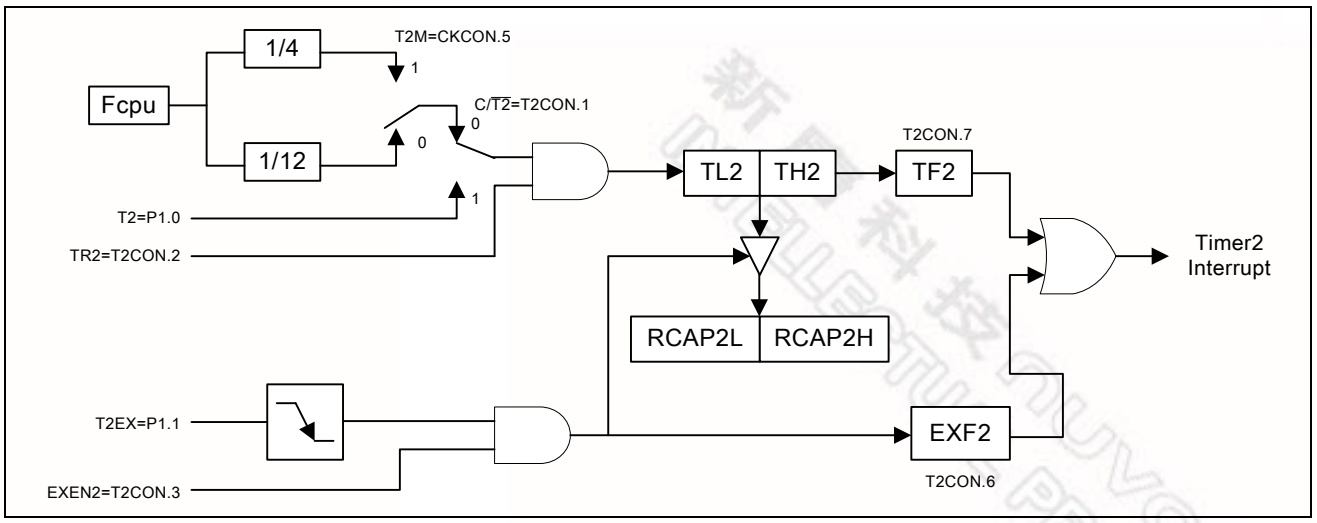


Figure 12-4: Timer 2 16-Bit Capture Mode

12.3.2 Auto-Reload Mode, Counting up

The auto-reload mode as an up counter is enabled by clearing the CP / $\overline{RL2}$ bit in the T2CON register and clearing the DCEN bit in T2MOD register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

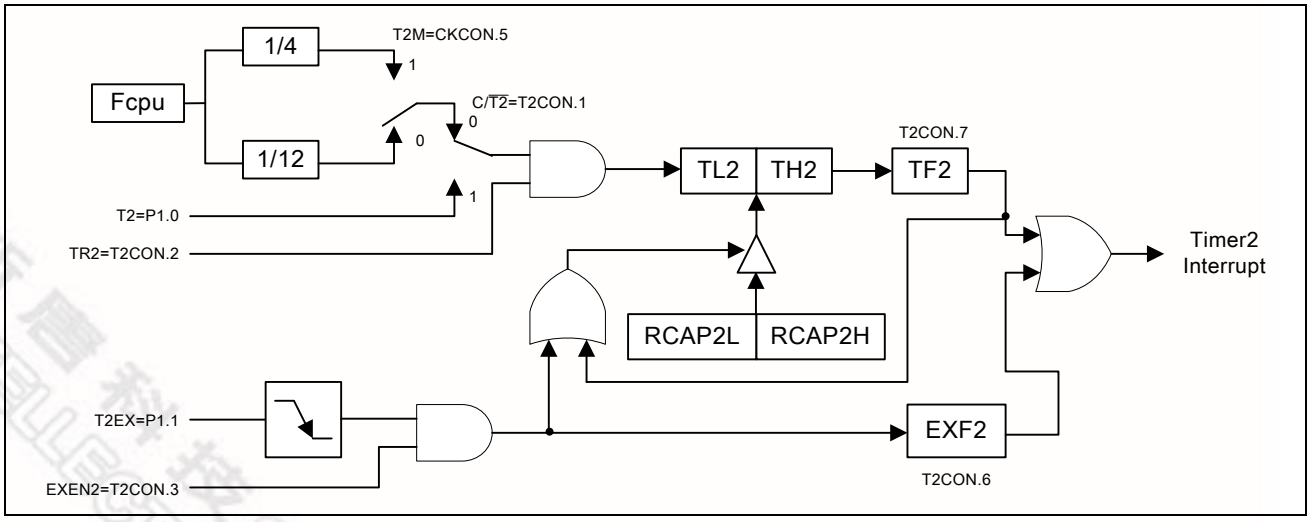


Figure 12-5: Timer 2 16-Bit Auto-reload Mode, Counting Up

12.3.3 Auto-Reload Mode, Counting Up/Down

Timer/Counter 2 will be in auto-reload mode as an up/down counter if CP / $\overline{RL2}$ bit in T2CON is cleared and the DCEN bit in T2MOD is set. In this mode, Timer/Counter 2 is an up/down counter whose direction is controlled by the T2EX pin. A 1 on this pin cause the counter to count up. An overflow while counting up will cause the counter to be reloaded with the contents of the capture

15. UART SERIAL PORT

Serial port in the N79E352(R) is a full duplex port. The N79E352(R) provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the N79E352(R) generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receive buffer register. The serial port can operate in four different modes as described below.

15.1 Mode 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the N79E352(R) whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This baud rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the N79E352(R).

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the N79E352(R) and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

15.4 Mode 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

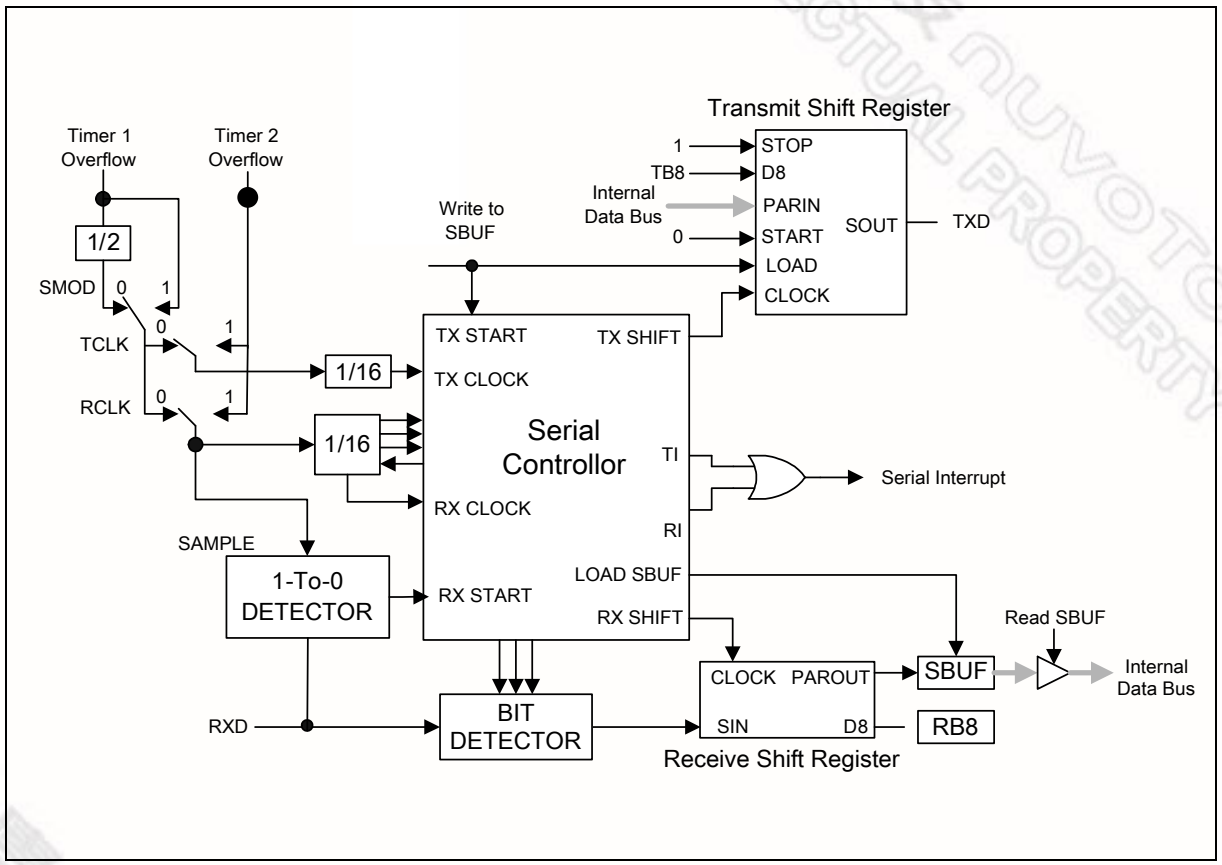


Figure 15-4: Uart Serial Port Mode 3

SM1	SM0	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit Function
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

Table 15-1: Uart Serial Port Modes

16.2.6 I2C Time-out Counter, I2Timerx

The I2C logic block provides a 14-bit timer-out counter that helps user to deal with bus pending problem. When SI is cleared user can set ENTI=1 to start the time-out counter. If I2C bus is pended too long to get any valid signal from devices on bus, the time-out counter overflows cause TIF=1 to request an I2C interrupt. The I2C interrupt is requested in the condition of either SI=1 or TIF=1. Flags SI and TIF must be cleared by software.

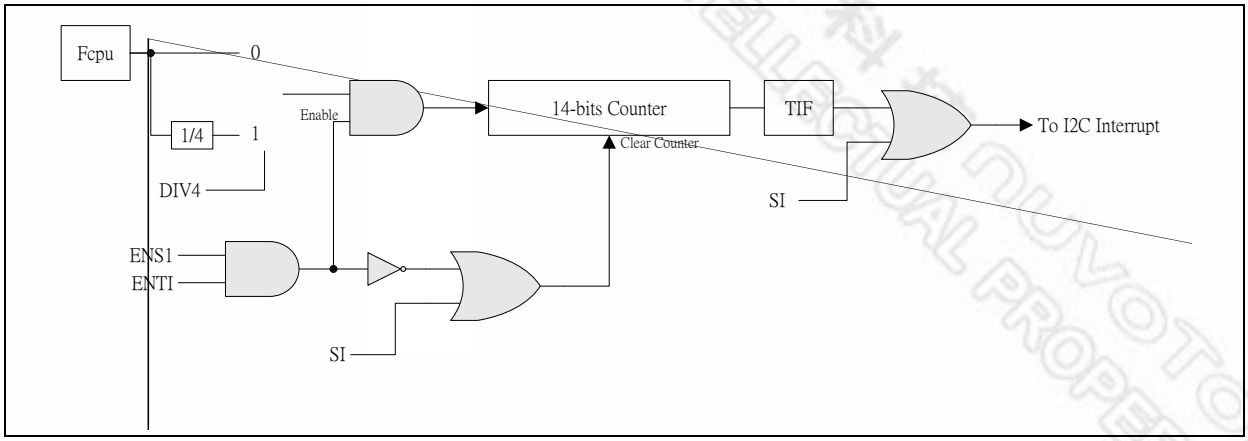


Figure 16-2: I2C Timer Count Block Diagram

16.3 Modes of Operation

The on-chip I2C ports support five operation modes, Master transmitter, Master receiver, Slave transmitter, Slave receiver, and GC call.

In a given application, I2C port may operate as a master or as a slave. In the slave mode, the I2C port hardware looks for its own slave address and the general call address. If one of these addresses is detected, and if the slave is willing to receive or transmit data from/to master(by setting the AA bit), acknowledge pulse will be transmitted out on the 9th clock, hence an interrupt is requested on both master and slave devices if interrupt is enabled. When the microcontroller wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the master mode, I2C port switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

16.3.1 Master Transmitter Mode

Serial data output through SDA while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case the data direction bit (R/W) will be logic 0, and it is represented by “W” in the flow diagrams. Thus the first byte transmitted is SLA+W. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

16.3.2 Master Receiver Mode

In this case the data direction bit (R/W) will be logic 1, and it is represented by “R” in the flow diagrams. Thus the first byte transmitted is SLA+R. Serial data is received via SDA while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

27.2 D.C. Characteristics

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4		5.5	V	V_{DD}=4.5V ~ 5.5V @ 24MHz V_{DD}=2.7V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 4MHz
Operating Current	I_{DD1}			5	mA	No load, RST = V_{DD}, V_{DD}= 3.0V @ 11.0592MHz
	I_{DD2}			15	mA	No load, RST = V_{DD}, V_{DD}= 5.0V @ 22.1184MHz
Idle Current	I_{IDLE}			4	mA	No load, V_{DD} = 3.0V @ 11.0592MHz
Power Down Current	I_{PWDN}		1	5	µA	No load, V_{DD} = 5.5V @ Disable BOV function
			1	5	uA	No load, V_{DD} = 3.0V @ Disable BOV function
Input / Output						
Input Current P0, P1, P2, P3, P4, P5	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current P1.5(RST pin)[1]	I_{IN2}	-48	-32	-24	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2, P3, P5 (Open Drain)	I_{LK}	-10	-	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4, P5	I_{TL} [*3]	-450	-	-246	µA	V_{DD} = 5.5V, V_{IN}<2.0V
		-93	-	-56		V_{DD}=2.4 Vin = 1.3v
Input Low Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6 1.0		V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4, P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 2.4V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		0.2V_{DD}		V	
Input Low Voltage RST [*1]	V_{IL21}	-	1.0	1.6	V	V_{DD}=4.5V

Output Data Hold to Clock Rising Edge SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XHQX}		 2 t_{CLCL} t_{CLCL}		ns	
Input Data Hold after Clock Rising SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XHDX}		 t_{CLCL} t_{CLCL}		ns	
Clock Rising Edge to Input Data Valid SM2=0 12 clocks per cycle SM2=1 4 clocks per cycle	t_{XHDV}		 11 t_{CLCL} 3 t_{CLCL}		ns	

27.3.5 Program Memory Read Cycle

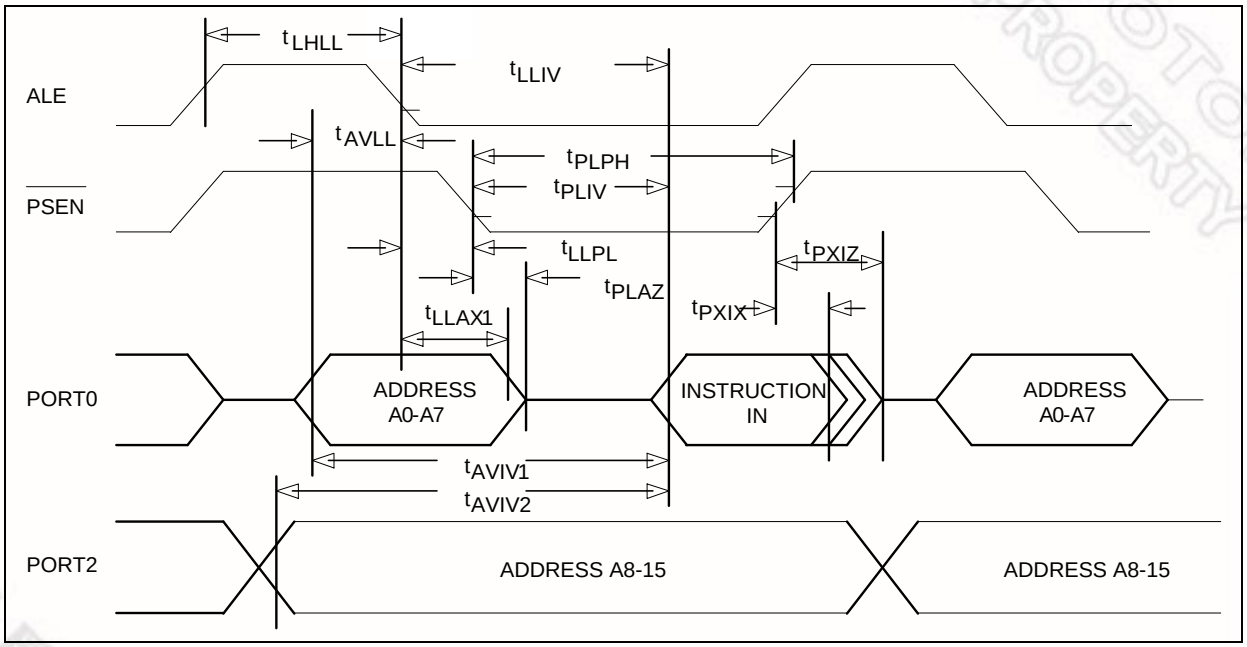


Figure 26-2 Program Memory Read Cycle

27.4 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
Frequency accuracy of On-chip RC oscillator (for N79E352)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
Frequency accuracy of On-chip RC oscillator with calibration[1] (for N79E352R)	-2		2	%	V_{DD}=4.5V~5.5V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		9	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

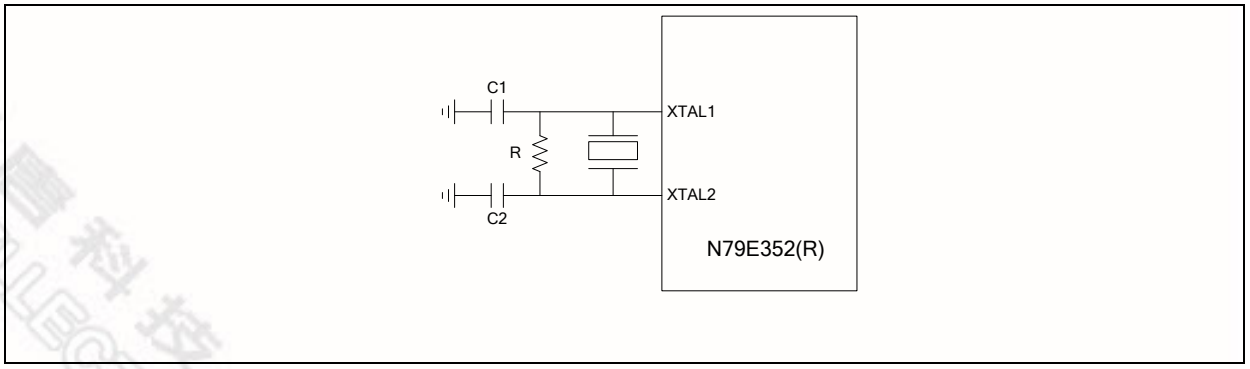
Note:

1. These values are for design guidance only and are not tested.

27.5 Typical Application Circuit

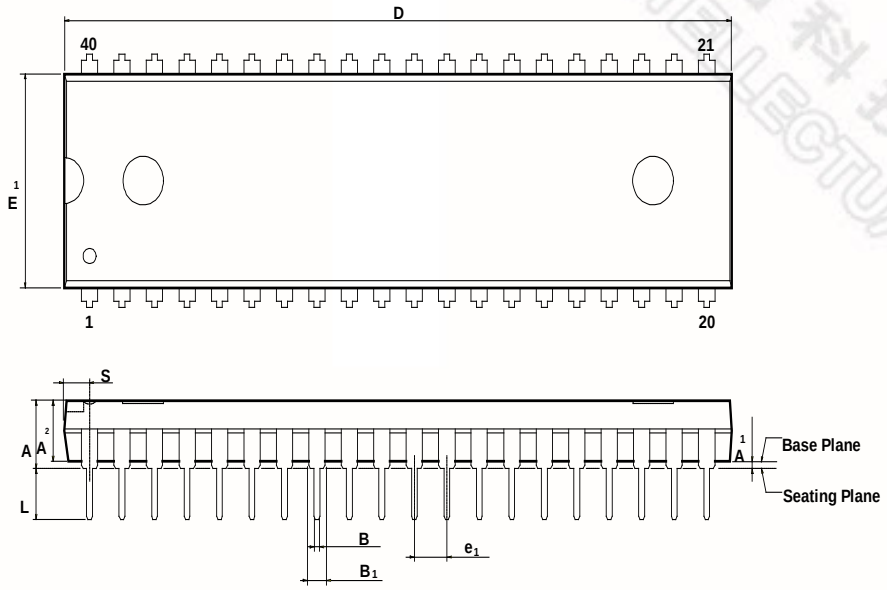
CRYSTAL	C1	C2	R
4MHz ~ 24MHz	without	without	without

The above table shows the reference values for crystal applications.



28. PACKAGE DIMENSIONS

28.1 40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29