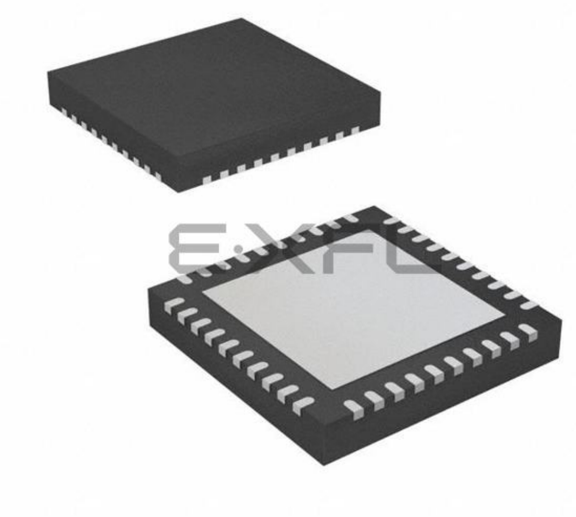

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c144-b-gmr

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{RESET}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{RESET}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{RESET}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{RESET}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C
Note: All voltages with respect to V_{SS}.						

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Oscillator (EXTOSC0)[8]	I_{EXTOSC}	FREQCN = 111	—	3.8	4.7	mA
		FREQCN = 110	—	840	950	µA
		FREQCN = 101	—	185	220	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	15	µA
		FREQCN = 001	—	5	10	µA
		FREQCN = 000	—	3	8	µA
SARADC0, SARADC1	I_{SARADC}	Sampling at 1 Msps, highest power mode settings.	—	1.2	1.5	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	510	µA
Temperature Sensor	I_{TSENSE}		—	75	105	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	750	µA
		Low Power Mode	—	160	190	µA
VREF0	I_{REFP}		—	75	100	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	—	µA
		CMPMD = 10	—	3	—	µA
		CMPMD = 01	—	10	—	µA
		CMPMD = 00	—	25	—	µA
Capacitive Sensing (CAPSENSE0)	I_{CS}	Continuous Conversions	—	55	80	µA
IDAC0[7], IDAC1[7]	I_{IDAC}		—	75	90	µA
IVC0[7]	I_{IVC}	$I_{IN} = 0$	—	1.5	2.5	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	25	µA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.14. Voltage Reference Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{DD} = 1.8–3.6 V	1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-Chip Precision Reference (VREF0)						
Valid Supply Range	V_{DD}	VREF2X = 0	1.8	—	3.6	V
		VREF2X = 1	2.7	—	3.6	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.195	1.2	1.205	V
		25 °C ambient, VREF2X = 1	2.39	2.4	2.41	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	25	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 3.16. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.4	—	mV
		CMPHYP = 01	—	4	—	mV
		CMPHYP = 10	—	8	—	mV
		CMPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.4	—	mV
		CMPHYN = 01	—	–4	—	mV
		CMPHYN = 10	—	–8	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}	PB2 Pins	—	7.5	—	pF
		PB3 Pins	—	10.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}		–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}		6			bits

3.2. Thermal Conditions

Table 3.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	LGA-92 Packages	—	35	—	°C/W
		TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		V_{SS}–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	V_{SS}–0.3	6.0	V
		EXTVREG0 Used	V_{SS}–0.3	3.6	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIOHD	V_{IOHD}		V_{SS}–0.3	6.5	V
Voltage on I/O pins, non Port Bank 3 I/O	V_{IN}	$\overline{\text{RESET}}$, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$\overline{\text{RESET}}$, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		Port Bank 0, 1, and 2 I/O	V_{SS}–0.3	V_{IO}+0.3	V
		Port Bank 4 I/O	V_{SSHD}–0.3	V_{IOHD}+0.3	V
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

4.1.5. Device Power Modes

The SiM3C1xx devices feature four low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low-Power Timer (LPT0), RTC0 (alarms and oscillator failure notification), Comparator 0, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0)

Normal Mode is the default mode of the device. The core and peripherals are fully operational, and instructions are executed from flash memory.

4.1.5.2. Power Mode 1

In Power Mode 1 the core and peripherals are fully operational, with instructions executing from RAM. Compared with Normal Mode, the active power consumption of the device in PM1 is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAM does not require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2

In Power Mode 2 the core halts and any enabled peripherals continue to run at the selected clock speed. The power consumption in PM2 corresponds to the AHB and APB clocks left enabled, thus the power can be tuned to the optimal level for the needs of the application. To place the device in PM2, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0 with the DMACTRL0 AHB clock disabled, PM2 can achieve similar power consumption to PM3, but with the ability to wake on APB-clocked interrupts. For example, enabling only the APB clock to the Ports will allow the firmware to wake on a PMATCH0, PBEXT0 or PBEXT1 interrupt with minimal impact on the supply current.

4.1.5.4. Power Mode 3

In Power Mode 3, the AHB and APB clocks are halted. The device may only wake from enabled interrupt sources which do not require the APB clock (RTC0ALRM, RTC0FAIL, LPTIMER0, VDDLOW and VREGLOW). A special fast wake option allows the device to operate at a very low level from the RTC0TCLK or LFOSC0 oscillator while in PM3, but quickly switch to the faster LPOSC0 when the wake event occurs. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

The device will enter PM3 on a WFI or WFE instruction. Because all AHB master clocks are disabled, the LPOSC will automatically halt and go into a low-power suspended state. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 9

In Power Mode 9, the core and all peripherals are halted, all clocks are stopped, and the pins and peripherals are set to a lower power mode. In addition, standard RAM contents are not preserved, though retention RAM contents are still available after exiting the power mode. This mode provides the lowest power consumption for the device, but requires an appropriate reset to exit. The available reset sources to wake from PM9 are controlled by the Power Management Unit (PMU).

Before entering PM9, the desired reset source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the RSTSRC0_CONFIG register must be set to indicate that PM9 is the desired power mode.

The device will enter PM9 on a WFI or WFE instruction, and remain in PM9 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.2. I/O

4.2.1. General Features

The SiM3C1xx ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB2 only) to generate simple square waves.
- A subset of pins can also serve as inputs to the Port Mapped Level Shifters available on the High Drive Pins.

4.2.2. High Drive Pins (PB4)

The High Drive pins have the following additional features:

- Programmable safe state: high, low, or high impedance.
- Programmable drive strength and slew rates.
- Programmable hardware current limiting.
- Powered from a separate source (VIOHD, which can be up to 6 V) from the rest of the device.
- Supports various functions, including GPIO, UART1 pins, EPCA0 pins, or Port Mapped Level Shifting.

4.2.3. 5 V Tolerant Pins (PB3)

The 5 V tolerant pins can be connected to external circuitry operating at voltages above the device supply without needing extra components to shift the voltage level.

4.2.4. Crossbars

The SiM3C1xx devices have two Crossbars with the following features:

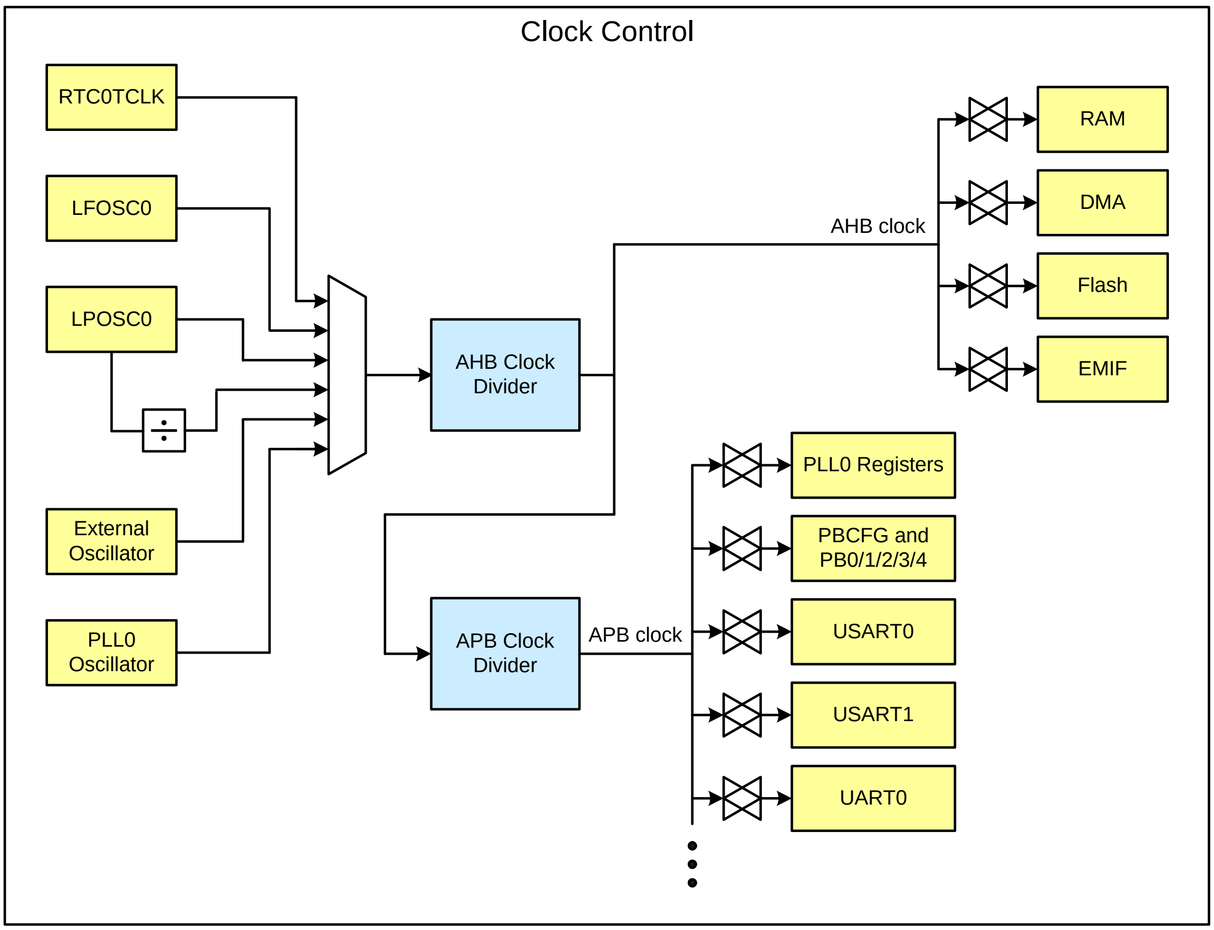
- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The Crossbars have a fixed priority for each I/O function and assign these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the Crossbars skip that pin when assigning the next selected resource. Additionally, the Crossbars will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.



4.6. Communications Peripherals

4.6.1. External Memory Interface (EMIF0)

The External Memory Interface (EMIF0) allows external parallel asynchronous devices, like SRAMs and LCD controllers, to appear as part of the system memory map. The EMIF0 module includes the following features:

- Provides a memory mapped view of multiple external devices.
- Support for byte, half-word and word accesses regardless of external device data-width.
- Error indicator for certain invalid transfers.
- Minimum external timing allows for 3 clocks per write or 4 clocks per read.
- Output bus can be shared between non-muxed and muxed devices.
- Available extended address output allows for up to 24-bit address with 8-bit parallel devices.
- Support for 8-bit and 16-bit (muxed-mode only) devices with up to two chip-select signals.
- Support for internally muxed devices with dynamic address shifting.
- Fully programmable control signal waveforms.

4.6.2. USART (USART0, USART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device. In addition to these signals, the USART0 module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.6.3. UART (UART0, UART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device.

The UART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud-rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX) or 1 Mbaud Smartcard (TX or RX).

- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation.
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.

4.6.4. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI module includes the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Programmable FIFO threshold level to request data service for DMA transfers.
- Support for multiple masters on the same data lines.

4.6.5. I2C (I2C0, I2C1)

The I2C interface is a two-wire, bi-directional serial bus. The two clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

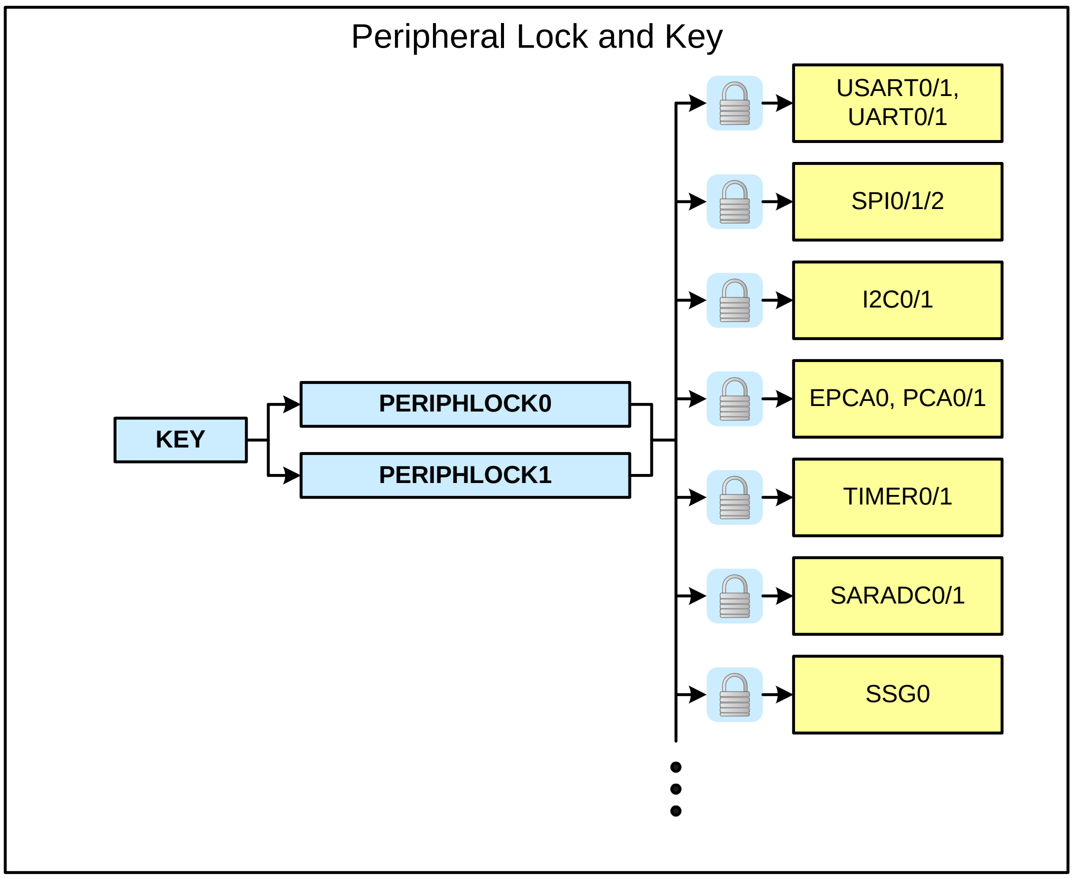
The I2C module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.

4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.



4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabiites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.

6. Pin Definitions and Packaging Information

6.1. SiM3C1x7 Pin Definitions

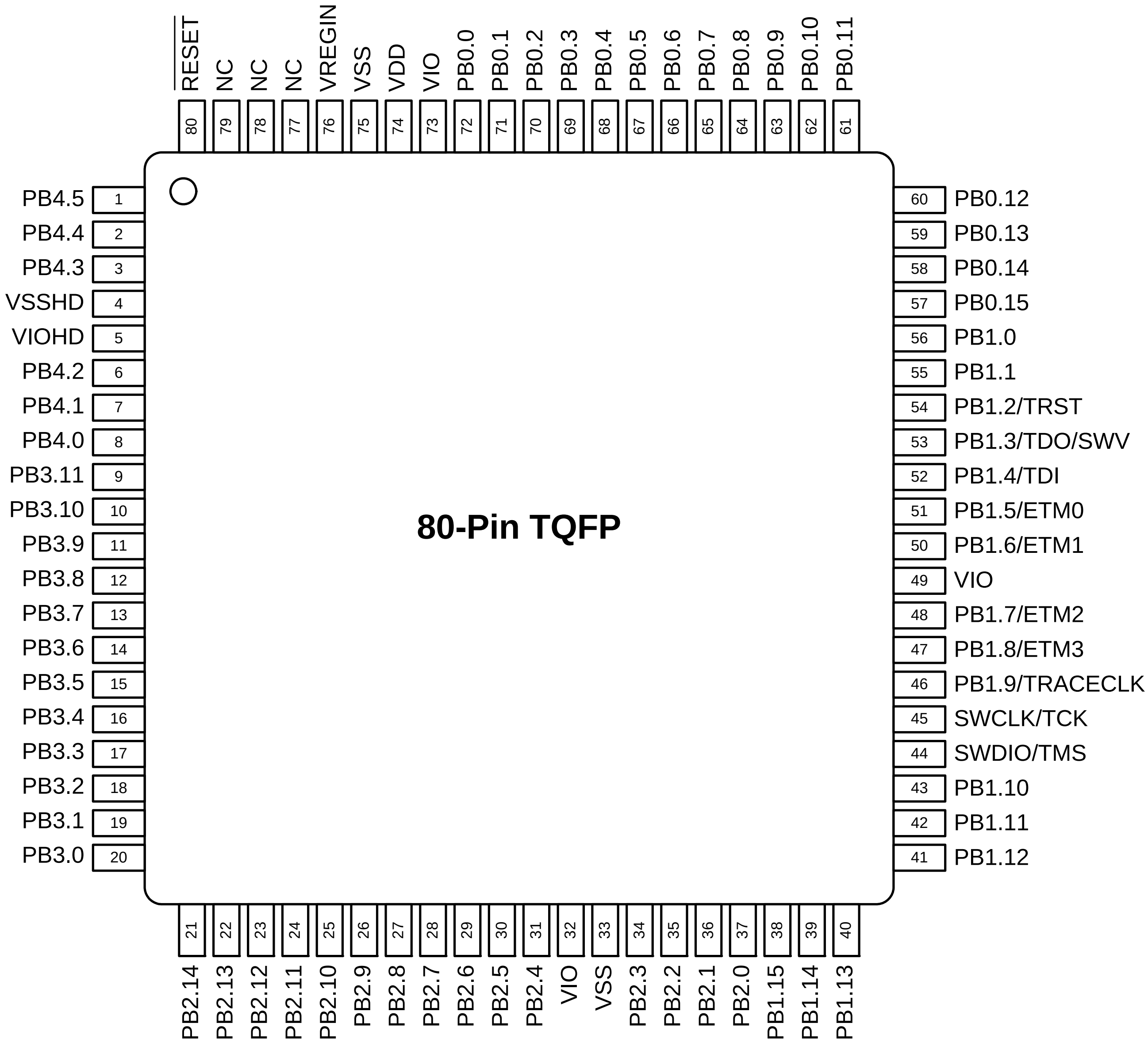


Figure 6.1. SiM3C1x7-GQ Pinout

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	33 75	B15 B34							
VDD	Power (Core)	74	A44							
VIO	Power (I/O)	32 49 73	A19 A29 A43							
VREGIN	Power (Regulator)	76	A45							
VSSHD	Ground (High Drive)	4	B2							
VIOHD	Power (High Drive)	5	A3							
$\overline{\text{RESET}}$	Active-low Reset	80	A48							
SWCLK/TCK	Serial Wire/JTAG	45	B20							
SWDIO/TMS	Serial Wire/JTAG	44	A27							
PB0.0	Standard I/O	72	B33	XBR0	✓					ADC0.0
PB0.1	Standard I/O	71	B32	XBR0	✓					ADC0.1 CS0.0
PB0.2	Standard I/O	70	A42	XBR0	✓					ADC0.2 CS0.1
PB0.3	Standard I/O	69	B31	XBR0	✓					ADC0.3 CS0.2
PB0.4	Standard I/O	68	A41	XBR0	✓					ADC0.4 CS0.3
PB0.5	Standard I/O	67	B30	XBR0	✓					ADC0.5 CS0.4
PB0.6	Standard I/O	66	A40	XBR0	✓					CS0.5
PB0.7	Standard I/O	65	B29	XBR0	✓					ADC0.6 CS0.6 IVC0.0

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	64	A39	XBR0	✓					ADC0.7 CS0.7 IVC0.1
PB0.9	Standard I/O	63	A38	XBR0	✓					ADC0.8 RTC1
PB0.10	Standard I/O	62	A37	XBR0	✓					RTC2
PB0.11	Standard I/O	61	D4	XBR0	✓					ADC0.9 VREFGND
PB0.12	Standard I/O	60	A36	XBR0	✓					ADC0.10 VREF
PB0.13	Standard I/O	59	A35	XBR0	✓					IDAC0
PB0.14	Standard I/O	58	B27	XBR0	✓					IDAC1
PB0.15	Standard I/O	57	A34	XBR0	✓					XTAL1
PB1.0	Standard I/O	56	A33	XBR0	✓					XTAL2
PB1.1	Standard I/O	55	B25	XBR0	✓					ADC0.11
PB1.2/TRST	Standard I/O /JTAG	54	A32	XBR0	✓					
PB1.3/TDO/ SWV	Standard I/O /JTAG/ Serial Wire Viewer	53	B24	XBR0	✓					ADC0.12 ADC1.12
PB1.4/TDI	Standard I/O /JTAG	52	A31	XBR0	✓					ADC0.13 ADC1.13
PB1.5/ETM0	Standard I/O /ETM	51	B23	XBR0	✓					ADC0.14 ADC1.14
PB1.6/ETM1	Standard I/O /ETM	50	A30	XBR0	✓					ADC0.15 ADC1.15
PB1.7/ETM2	Standard I/O /ETM	48	B22	XBR0	✓					ADC1.11 CS0.8
PB1.8/ETM3	Standard I/O /ETM	47	B21	XBR0	✓					ADC1.10 CS0.9

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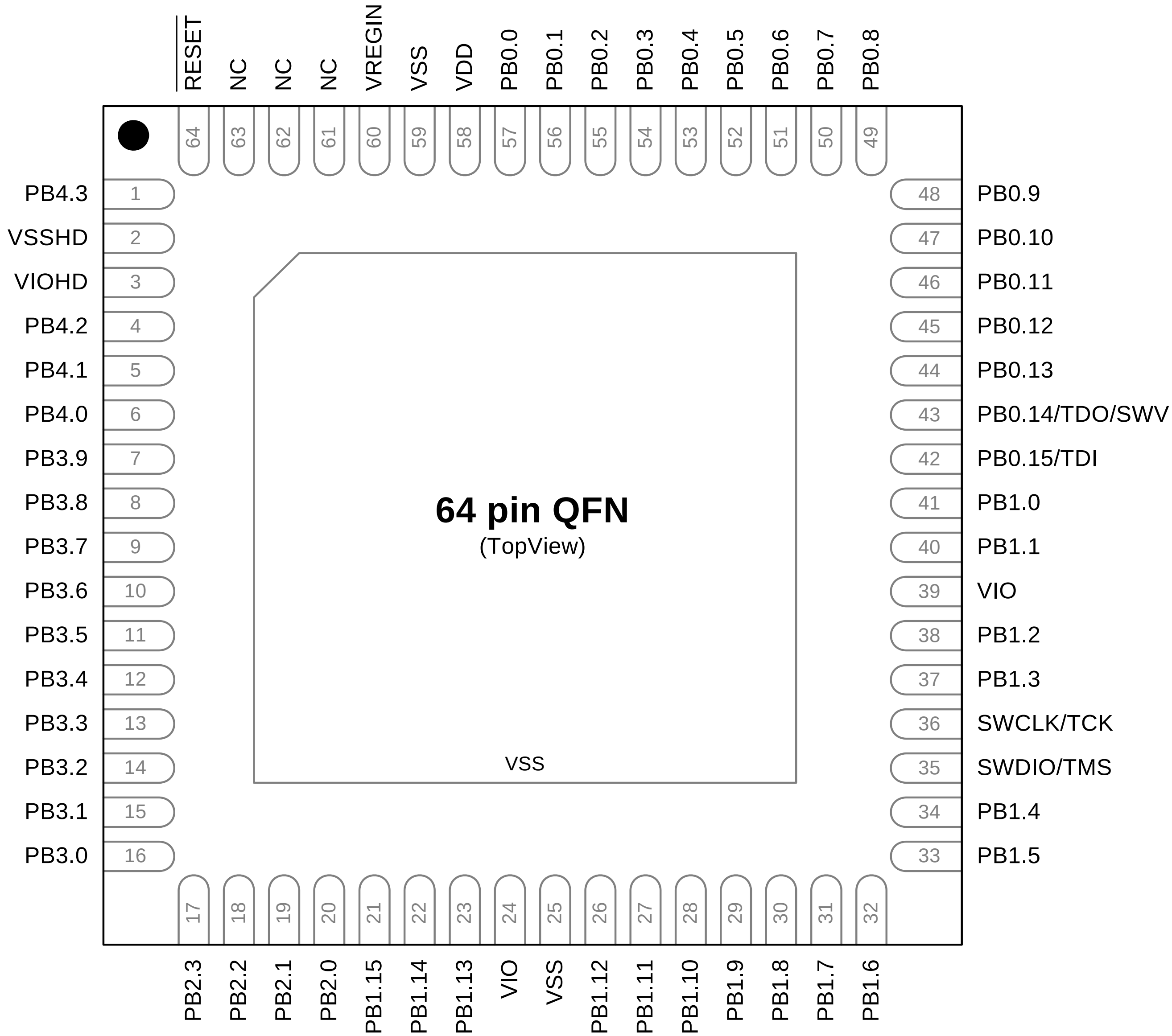

Figure 6.4. SiM3C1x6-GM Pinout

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	25 59							
VDD	Power (Core)	58							
VIO	Power (I/O)	24 39							
VREGIN	Power (Regulator)	60							
VSSHD	Ground (High Drive)	2							
VIOHD	Power (High Drive)	3							
$\overline{\text{RESET}}$	Active-low Reset	64							
SWCLK/TCK	Serial Wire / JTAG	36							
SWDIO/TMS	Serial Wire / JTAG	35							
PB0.0	Standard I/O	57	XBR0	✓					ADC0.2 CS0.1
PB0.1	Standard I/O	56	XBR0	✓					ADC0.3 CS0.2
PB0.2	Standard I/O	55	XBR0	✓					ADC0.4 CS0.3
PB0.3	Standard I/O	54	XBR0	✓					ADC0.5 CS0.4
PB0.4	Standard I/O	53	XBR0	✓					ADC0.6 CS0.5 IVC0.0
PB0.5	Standard I/O	52	XBR0	✓					ADC0.7 CS0.6 IVC0.1
PB0.6	Standard I/O	51	XBR0	✓					ADC0.8 CS0.7 RTC1

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.8	Standard I/O	30	XBR0	✓	AD14m/ A6			WAKE.2	ADC1.3 CS0.12
PB1.9	Standard I/O	29	XBR0	✓	AD13m/ A5			WAKE.3	ADC1.2 CS0.13
PB1.10	Standard I/O	28	XBR0	✓	AD12m/ A4			DMA0T1 WAKE.4	ADC1.1 CS0.14
PB1.11	Standard I/O	27	XBR0	✓	AD11m/ A3			DMA0T0 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.12	Standard I/O	26	XBR0	✓	AD10m/ A2			WAKE.6	
PB1.13	Standard I/O	23	XBR0	✓	AD9m/ A1				
PB1.14	Standard I/O	22	XBR0	✓	AD8m/ A0				
PB1.15	Standard I/O	21	XBR0	✓	AD7m/ D7				
PB2.0	Standard I/O	20	XBR1	✓	AD6m/ D6	LSI0	Yes	INT0.0 INT1.0	
PB2.1	Standard I/O	19	XBR1	✓	AD5m/ D5	LSI1	Yes	INT0.1 INT1.1	
PB2.2	Standard I/O	18	XBR1	✓	AD4m/ D4	LSI2	Yes	INT0.2 INT1.2	CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.3	Standard I/O	17	XBR1	✓	AD3m/ D3	LSI3	Yes	INT0.3 INT1.3	CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	16	XBR1	✓	AD2m/ D2				CMP0P.1 CMP1P.1
PB3.1	5 V Tolerant I/O	15	XBR1	✓	AD1m/ D1				CMP0N.1 CMP1N.1

6.4. LGA-92 Package Specifications

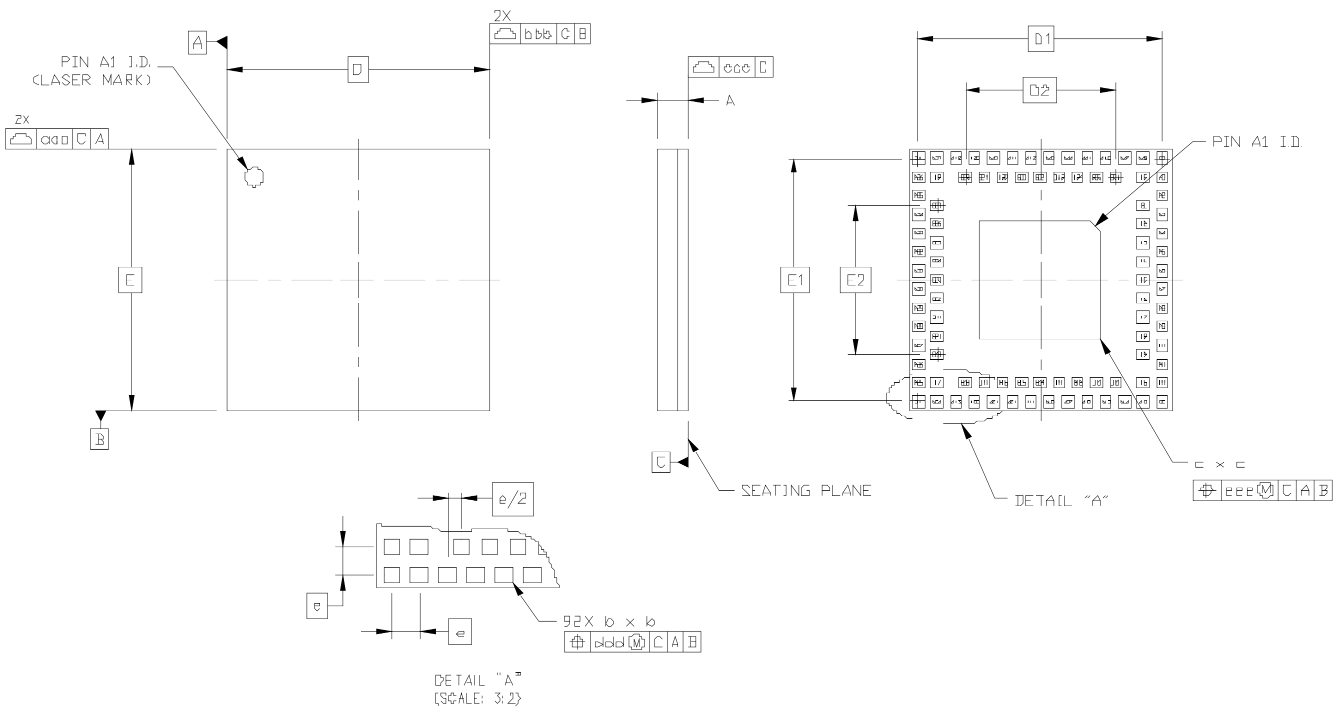

Figure 6.6. LGA-92 Package Drawing

Table 6.4. LGA-92 Package Dimensions

Dimension	Min	Nominal	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
c	3.15	3.20	3.25
D		7.00 BSC	
D1		6.50 BSC	
D2		4.00 BSC	
e		0.50 BSC	
E		7.00 BSC	
E1		6.50 BSC	
E2		4.00 BSC	
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 6.10. TQFP-64 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.