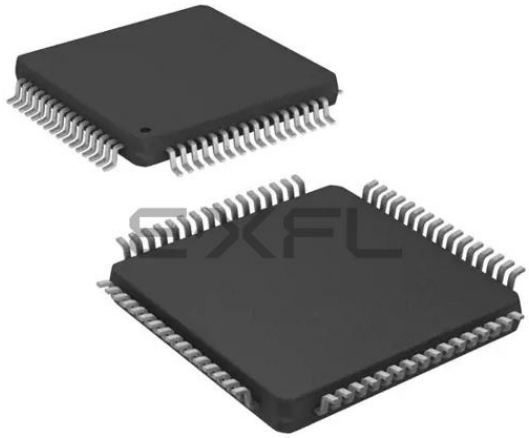

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Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c146-b-gqr

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Oscillator (EXTOSC0)[8]	I_{EXTOSC}	FREQCN = 111	—	3.8	4.7	mA
		FREQCN = 110	—	840	950	µA
		FREQCN = 101	—	185	220	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	15	µA
		FREQCN = 001	—	5	10	µA
		FREQCN = 000	—	3	8	µA
SARADC0, SARADC1	I_{SARADC}	Sampling at 1 Msps, highest power mode settings.	—	1.2	1.5	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	510	µA
Temperature Sensor	I_{TSENSE}		—	75	105	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	750	µA
		Low Power Mode	—	160	190	µA
VREF0	I_{REFP}		—	75	100	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	—	µA
		CMPMD = 10	—	3	—	µA
		CMPMD = 01	—	10	—	µA
		CMPMD = 00	—	25	—	µA
Capacitive Sensing (CAPSENSE0)	I_{CS}	Continuous Conversions	—	55	80	µA
IDAC0[7], IDAC1[7]	I_{IDAC}		—	75	90	µA
IVC0[7]	I_{IVC}	I_{IN} = 0	—	1.5	2.5	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	25	µA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} High Supply Monitor Threshold (VDDHITHEN = 1)	V_{VDDMH}	Early Warning	2.10	2.20	2.30	V
		Reset	1.95	2.05	2.1	V
V_{DD} Low Supply Monitor Threshold (VDDHITHEN = 0)	V_{VDDML}	Early Warning	1.81	1.85	1.88	V
		Reset	1.70	1.74	1.77	V
V_{REGIN} Supply Monitor Threshold	V_{VREGM}	Early Warning	4.2	4.4	4.6	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.4	—	V
		Falling Voltage on V_{DD}	0.8	1	1.3	V
V_{DD} Ramp Time	t_{RMP}	Time to $V_{DD} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.4	1	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13	kHz
V_{DD} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.7. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
V_{DD} Voltage During Programming	V_{PROG}		1.8	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During a sequential write operation, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 3.8. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency*	$f_{PLL0OSC}$	Full Temperature and Supply Range	77	79	80	MHz
Power Supply Sensitivity*	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 79 MHz	—	430	—	ppm/V
Temperature Sensitivity*	$TS_{PLL0OSC}$	V_{DD} = 3.3 V, Fout = 79 MHz	—	95	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	80	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 80 MHz, M=24, N=99, LOCKTH = 0	—	1.7	—	µs
		f_{REF} = 32 kHz, $f_{PLL0OSC}$ = 80 MHz, M=0, N=2440, LOCKTH = 0	—	91	—	µs

***Note:** PLL0OSC in free-running oscillator mode.

Table 3.12. Capacitive Sense

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single Conversion Time (Default Configuration)	t_{single}	12-bit Mode	—	25	—	µs
		13-bit Mode	—	27	—	µs
		14-bit Mode	—	29	—	µs
		16-bit Mode	—	33	—	µs
Maximum External Capacitive Load	C_L	Highest Gain Setting (default)	—	45	—	pF
		Lowest Gain Setting	—	500	—	pF
Maximum External Series Impedance	C_L	Highest Gain Setting (default)	—	50	—	kΩ

Table 3.13. Current-to-Voltage Converter (IVC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (VDD)	V_{DDIVC}		2.2	—	3.6	V
Input Pin Voltage	V_{IN}		2.2	—	VDD	V
Minimum Input Current (source)	I_{IN}		100	—	—	µA
Integral Nonlinearity	INL_{IVC}		–0.6	—	0.6	%
Full Scale Output	V_{IVCOUT}		—	1.65	—	V
Slope	M_{IVC}	Input Range 1 mA (INxRANGE = 101)	1.55	1.65	1.75	V/mA
		Input Range 2 mA (INxRANGE = 100)	795	830	860	mV/mA
		Input Range 3 mA (INxRANGE = 011)	525	550	570	mV/mA
		Input Range 4 mA (INxRANGE = 010)	390	415	430	mV/mA
		Input Range 5 mA (INxRANGE = 001)	315	330	340	mV/mA
		Input Range 6 mA (INxRANGE = 000)	260	275	285	mV/mA
Settling Time to 0.1%	V_{IVCOUT}		—	—	500	ns

Table 3.14. Voltage Reference Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{DD} = 1.8–3.6 V	1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-Chip Precision Reference (VREF0)						
Valid Supply Range	V_{DD}	VREF2X = 0	1.8	—	3.6	V
		VREF2X = 1	2.7	—	3.6	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.195	1.2	1.205	V
		25 °C ambient, VREF2X = 1	2.39	2.4	2.41	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	25	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 3.17. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard I/O (PB0, PB1, and PB2), 5 V Tolerant I/O (PB3), and $\overline{\text{RESET}}$						
Output High Voltage*	V_{OH}	Low Drive, I_{OH} = –2 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –5 mA	V_{IO} – 0.7	—	—	V
Output Low Voltage*	V_{OL}	Low Drive, I_{OL} = 3 mA	—	—	0.6	V
		High Drive, I_{OL} = 12.5 mA	—	—	0.6	V
Input High Voltage	V_{IH}	1.8 ≤ V_{IO} ≤ 2.0	0.7 x V_{IO}	—	—	V
		2.0 ≤ V_{IO} ≤ 3.6	V_{IO} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}	PB0, PB1 and PB2 Pins	—	4	—	pF
		PB3 Pins	—	7	—	pF
Weak Pull-Up Current (Input Voltage = 0 V)	I_{PU}	V_{IO} = 1.8	–6	–3.5	–2	µA
		V_{IO} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	0 ≤ V_{IN} ≤ V_{IO}	–1	—	1	µA
Input Leakage Current of Port Bank 3 I/O, V_{IN} above V_{IO}	I_L	V_{IO} < V_{IN} < V_{IO}+2.0 V (pins without EXREG functions)	0	5	150	µA
		V_{IO} < V_{IN} < V_{REGIN} (pins with EXREG functions)	0	5	150	µA
High Drive I/O (PB4)						
Output High Voltage	V_{OH}	Standard Mode, Low Drive, I_{OH} = –3 mA	V_{IOHD} – 0.7	—	—	V
		Standard Mode, High Drive, I_{OH} = –10 mA	V_{IOHD} – 0.7	—	—	V
Output Low Voltage	V_{OL}	Standard Mode, Low Drive, I_{OH} = 3 mA	—	—	0.6	V
		Standard Mode, High Drive, I_{OH} = 12.5 mA	—	—	0.6	V
Output Rise Time	t_R	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

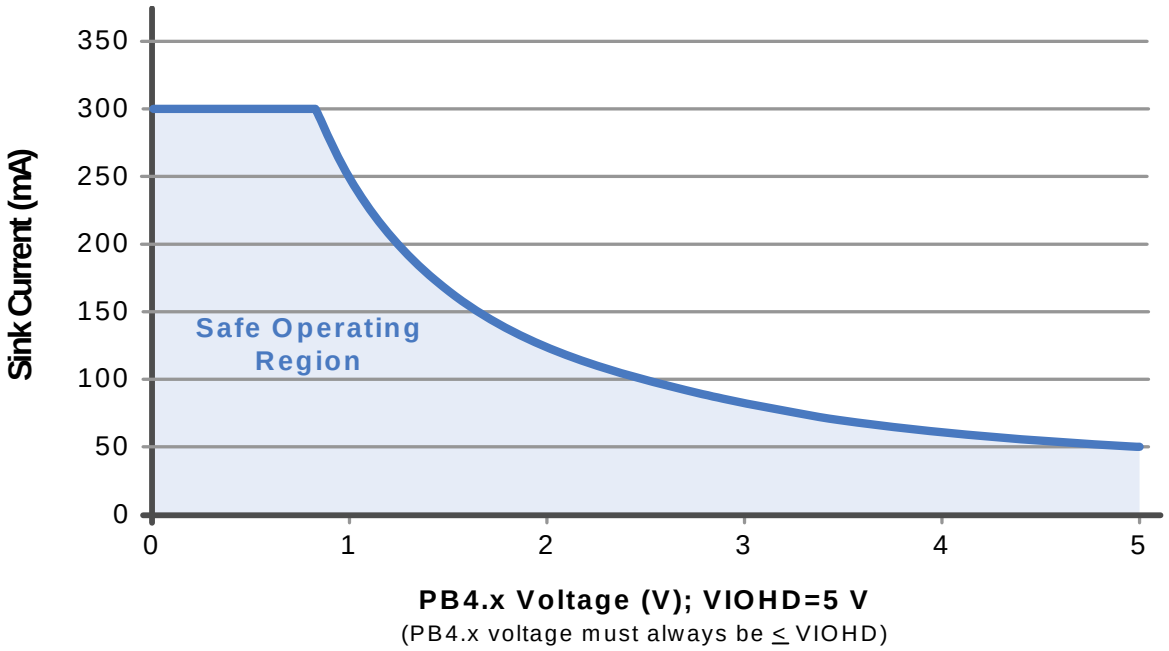

Figure 3.1. Maximum Sink Current vs. PB4.x Pin Voltage

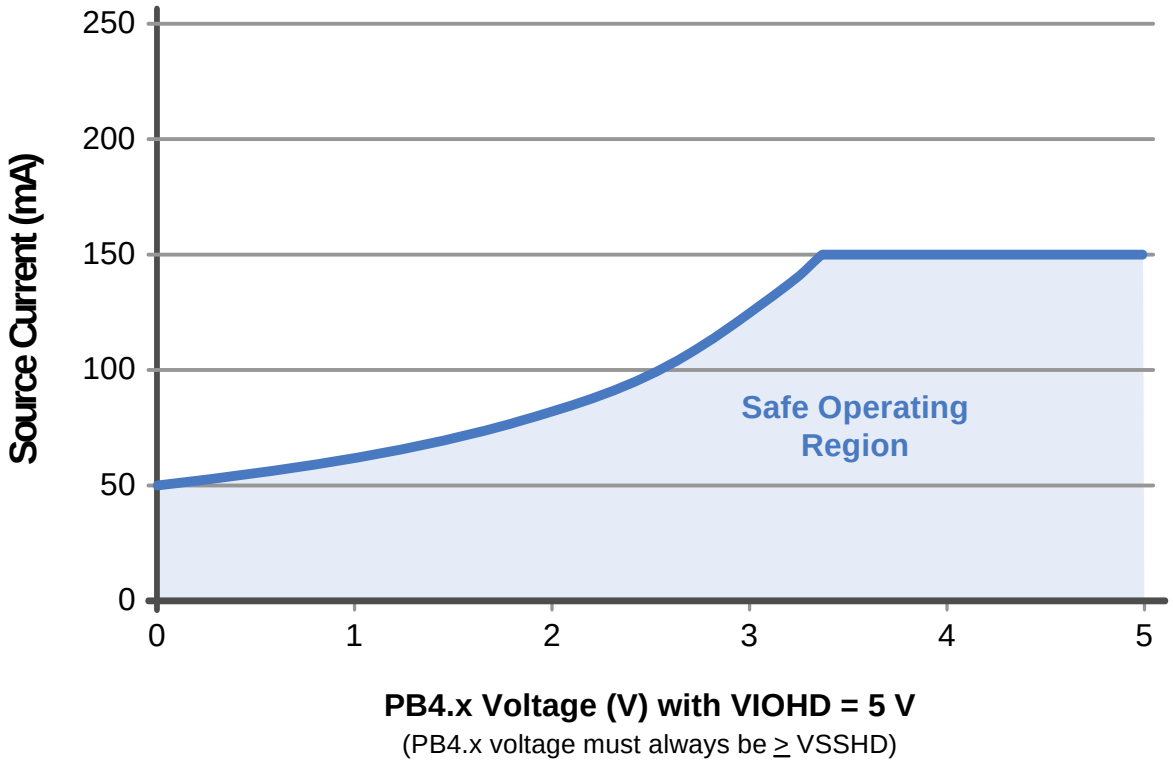

Figure 3.2. Maximum Source Current vs. PB4.x Pin Voltage

3.2. Thermal Conditions

Table 3.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	LGA-92 Packages	—	35	—	°C/W
		TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		V_{SS}–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	V_{SS}–0.3	6.0	V
		EXTVREG0 Used	V_{SS}–0.3	3.6	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIOHD	V_{IOHD}		V_{SS}–0.3	6.5	V
Voltage on I/O pins, non Port Bank 3 I/O	V_{IN}	$\overline{\text{RESET}}$, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$\overline{\text{RESET}}$, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		Port Bank 0, 1, and 2 I/O	V_{SS}–0.3	V_{IO}+0.3	V
		Port Bank 4 I/O	V_{SSHD}–0.3	V_{IOHD}+0.3	V
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

4. Precision32™ SiM3C1xx System Overview

The SiM3C1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 80 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB Flash; in-system programmable, 8–32 kB SRAM (including 4 kB retention SRAM, which preserves state in PM9 mode).
- **Power:**
  - Low drop-out (LDO) regulator for CPU core voltage.
  - Power-on reset circuit and brownout detectors.
  - 3.3 V output LDO for direct power from 5 V supplies.
  - External transistor regulator.
  - Power Management Unit (PMU).
- **I/O: Up to 65 total multifunction I/O pins:**
  - Up to six programmable high-power capable (5–300 mA with programmable current limiting, 1.8–5 V).
  - Up to twelve 5 V tolerant general purpose pins.
  - Two flexible peripheral crossbars for peripheral routing.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–80 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz and 2.5 MHz modes.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock modes.
  - Programmable clock divider allows any oscillator source to be divided by binary factor from 1-128.
- **Data Peripherals:**
  - 16-Channel DMA Controller.
  - 128/192/256-bit Hardware AES Encryption.
  - 16/32-bit CRC.
- **Timers/Counters and PWM:**
  - 6-channel Enhanced Programmable Counter Array (EPCAn) supporting advanced PWM and capture/compare.
  - 2 x 2-channel Standard Programmable Counter Array (PCAn) supporting PWM and capture/compare.
  - 2 x 32-bit Timers - can be split into 4 x 16-bit Timers, support PWM and capture/compare.
  - Real Time Clock (RTCn).
  - Low Power Timer.
  - Watchdog Timer.
- **Communications Peripherals:**
  - External Memory Interface.
  - 2 x USARTs and 2 x UARTs with IrDA and ISO7816 SmartCard support.
  - 3 x SPIs.
  - 2 x I2C.
  - I^2S (receive and transmit).
- **Analog:**
  - 2 x 12-Bit Analog-to-Digital Converters (SARADC).
  - 2 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 16-Channel Capacitance-to-Digital Converter (CAPSENSE).
  - 2 x Low-Current Comparators (CMP).
  - 1 x Current-to-Voltage Converter (IVC) module with two channels.
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the SiM3C1xx devices are truly standalone system-on-a-chip solutions. The Flash memory is reprogrammable in-circuit, providing non-

4.1. Power

4.1.1. LDO and Voltage Regulator (VREG0)

The SiM3C1xx devices include two internal regulators: the core LDO Regulator and the Voltage Regulator (VREG0).

The LDO Regulator converts a 1.8–3.6 V supply to the core operating voltage of 1.8 V. This LDO consumes little power and provides flexibility in choosing a power supply for the system.

The Voltage Regulator regulates from 5.5 to 2.7 V and can serve as an input to the LDO. This allows the device to be powered from up to a 5.5 V supply without any external components other than bypass capacitors.

4.1.2. Voltage Supply Monitor (VMON0)

The SiM3C1xx devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware. The supply monitor includes additional circuitry that can monitor the main supply voltage and the VREGIN input voltage divided by 4 (VREGIN / 4).

The supply monitor module includes the following features:

- Main supply “VDD Low” (VDD below the early warning threshold) notification.
- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.
- VREGIN divided by 4 (VREGIN / 4) supply “VREGIN Low” notification.

4.1.3. External Regulator (EXTVREG0)

The External Regulator provides all the circuitry needed for a high-power regulator except the power transistor (NPN or PNP) and current sensing resistor (if current limiting is enabled).

The External Regulator module has the following features:

- Interfaces with either an NPN or PNP external transistor that serves as the pass device for the high current regulator.
- Automatic current limiting.
- Automatic foldback limiting.
- Sources up to 1 A for use by external circuitry.
- Variable output voltage from 1.8–3.6 V in 100 mV steps.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3C1xx manages the power systems of the device. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins. It also recognizes and manages the various wake sources for low-power modes of the device.

The PMU module includes the following features:

- Up to 16 pin wake inputs can wake the device from Power Mode 9.
- The Low Power Timer, RTC0 (alarms and oscillator fail), Comparator 0, and the $\overline{\text{RESET}}$ pin can also serve as wake sources for Power Mode 9.
- All PM9 wake sources (except for the $\overline{\text{RESET}}$ pin) can also reset the Low Power Timer or RTC0 modules.
- Disables the level shifters to pins and peripherals to further reduce power usage in PM9. These level shifters must be re-enabed by firmware after exiting PM9.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM9.

4.1.5. Device Power Modes

The SiM3C1xx devices feature four low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low-Power Timer (LPT0), RTC0 (alarms and oscillator failure notification), Comparator 0, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0)

Normal Mode is the default mode of the device. The core and peripherals are fully operational, and instructions are executed from flash memory.

4.1.5.2. Power Mode 1

In Power Mode 1 the core and peripherals are fully operational, with instructions executing from RAM. Compared with Normal Mode, the active power consumption of the device in PM1 is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAM does not require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2

In Power Mode 2 the core halts and any enabled peripherals continue to run at the selected clock speed. The power consumption in PM2 corresponds to the AHB and APB clocks left enabled, thus the power can be tuned to the optimal level for the needs of the application. To place the device in PM2, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0 with the DMACTRL0 AHB clock disabled, PM2 can achieve similar power consumption to PM3, but with the ability to wake on APB-clocked interrupts. For example, enabling only the APB clock to the Ports will allow the firmware to wake on a PMATCH0, PBEXT0 or PBEXT1 interrupt with minimal impact on the supply current.

4.1.5.4. Power Mode 3

In Power Mode 3, the AHB and APB clocks are halted. The device may only wake from enabled interrupt sources which do not require the APB clock (RTC0ALRM, RTC0FAIL, LPTIMER0, VDDLOW and VREGLOW). A special fast wake option allows the device to operate at a very low level from the RTC0TCLK or LFOSC0 oscillator while in PM3, but quickly switch to the faster LPOSC0 when the wake event occurs. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

The device will enter PM3 on a WFI or WFE instruction. Because all AHB master clocks are disabled, the LPOSC will automatically halt and go into a low-power suspended state. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 9

In Power Mode 9, the core and all peripherals are halted, all clocks are stopped, and the pins and peripherals are set to a lower power mode. In addition, standard RAM contents are not preserved, though retention RAM contents are still available after exiting the power mode. This mode provides the lowest power consumption for the device, but requires an appropriate reset to exit. The available reset sources to wake from PM9 are controlled by the Power Management Unit (PMU).

Before entering PM9, the desired reset source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the RSTSRC0_CONFIG register must be set to indicate that PM9 is the desired power mode.

The device will enter PM9 on a WFI or WFE instruction, and remain in PM9 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.2. I/O

4.2.1. General Features

The SiM3C1xx ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB2 only) to generate simple square waves.
- A subset of pins can also serve as inputs to the Port Mapped Level Shifters available on the High Drive Pins.

4.2.2. High Drive Pins (PB4)

The High Drive pins have the following additional features:

- Programmable safe state: high, low, or high impedance.
- Programmable drive strength and slew rates.
- Programmable hardware current limiting.
- Powered from a separate source (VIOHD, which can be up to 6 V) from the rest of the device.
- Supports various functions, including GPIO, UART1 pins, EPCA0 pins, or Port Mapped Level Shifting.

4.2.3. 5 V Tolerant Pins (PB3)

The 5 V tolerant pins can be connected to external circuitry operating at voltages above the device supply without needing extra components to shift the voltage level.

4.2.4. Crossbars

The SiM3C1xx devices have two Crossbars with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The Crossbars have a fixed priority for each I/O function and assign these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the Crossbars skip that pin when assigning the next selected resource. Additionally, the Crossbars will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	33 75	B15 B34							
VDD	Power (Core)	74	A44							
VIO	Power (I/O)	32 49 73	A19 A29 A43							
VREGIN	Power (Regulator)	76	A45							
VSSHD	Ground (High Drive)	4	B2							
VIOHD	Power (High Drive)	5	A3							
$\overline{\text{RESET}}$	Active-low Reset	80	A48							
SWCLK/TCK	Serial Wire/JTAG	45	B20							
SWDIO/TMS	Serial Wire/JTAG	44	A27							
PB0.0	Standard I/O	72	B33	XBR0	✓					ADC0.0
PB0.1	Standard I/O	71	B32	XBR0	✓					ADC0.1 CS0.0
PB0.2	Standard I/O	70	A42	XBR0	✓					ADC0.2 CS0.1
PB0.3	Standard I/O	69	B31	XBR0	✓					ADC0.3 CS0.2
PB0.4	Standard I/O	68	A41	XBR0	✓					ADC0.4 CS0.3
PB0.5	Standard I/O	67	B30	XBR0	✓					ADC0.5 CS0.4
PB0.6	Standard I/O	66	A40	XBR0	✓					CS0.5
PB0.7	Standard I/O	65	B29	XBR0	✓					ADC0.6 CS0.6 IVC0.0

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.4	5 V Tolerant I/O	16	A9	XBR1	✓	$\overline{OE}$			INT0.9 INT1.9 WAKE.8	CMP0P.4 CMP1P.4
PB3.5	5 V Tolerant I/O	15	B7	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.10 INT1.10 WAKE.9	CMP0N.4 CMP1N.4
PB3.6	5 V Tolerant I/O	14	A8	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.11 INT1.11 WAKE.10	CMP0P.5 CMP1P.5
PB3.7	5 V Tolerant I/O	13	B6	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 LPT0T1 INT0.12 INT1.12 WAKE.11	CMP0N.5 CMP1N.5
PB3.8	5 V Tolerant I/O	12	A7	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T2 INT0.13 INT1.13 WAKE.12	CMP0P.6 CMP1P.6 EXREGSP
PB3.9	5 V Tolerant I/O	11	B5	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 INT0.14 INT1.14 WAKE.13	CMP0N.6 CMP1N.6 EXREGSN
PB3.10	5 V Tolerant I/O	10	B4	XBR1	✓				INT0.15 INT1.15 WAKE.14	CMP0P.7 CMP1P.7 EXREGOUT
PB3.11	5 V Tolerant I/O	9	B3	XBR1	✓				WAKE.15	CMP0N.7 CMP1N.7 EXREGBD

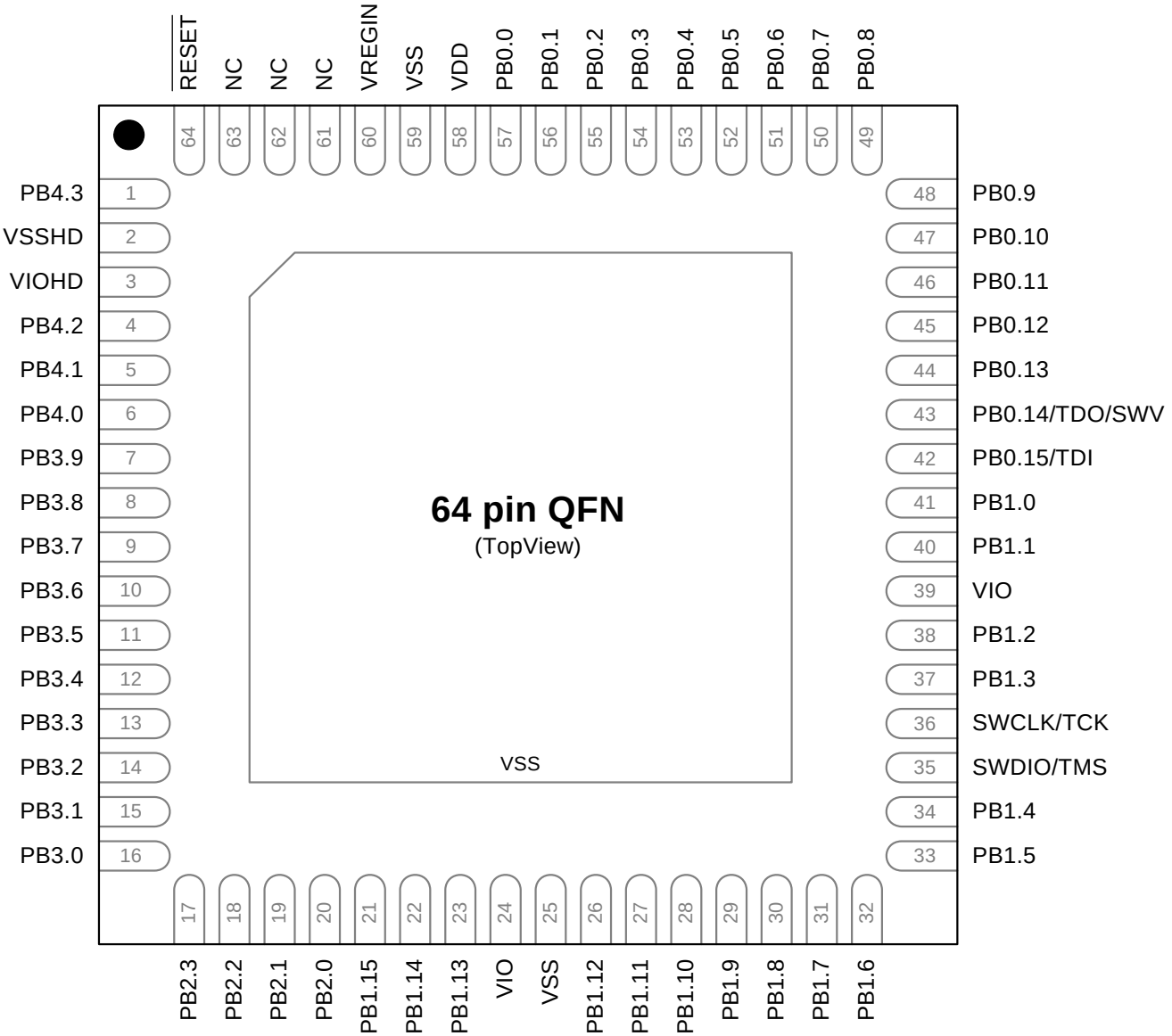

Figure 6.4. SiM3C1x6-GM Pinout

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	26	XBR0	✓			ADC0.14 ADC1.14
PB0.9	Standard I/O	25	XBR0	✓			ADC0.15 ADC1.15
PB0.10	Standard I/O	22	XBR0	✓		DMA0T1	ADC1.8
PB0.11	Standard I/O	21	XBR0	✓		DMA0T0	ADC1.7
PB0.12	Standard I/O	20	XBR0	✓		ADC0T15 WAKE.0	ADC1.5 CS0.10
PB0.13	Standard I/O	19	XBR0	✓		ADC1T15 WAKE.1	ADC1.4 CS0.11
PB0.14	Standard I/O	18	XBR0	✓		WAKE.2	ADC1.3 CS0.12
PB0.15	Standard I/O	17	XBR0	✓		WAKE.3	ADC1.2 CS0.13
PB1.0	Standard I/O	16	XBR0	✓		WAKE.4	ADC1.1 CS0.14
PB1.1	Standard I/O	15	XBR0	✓		WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.2	Standard I/O	12	XBR0	✓			CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB1.3	Standard I/O	11	XBR0	✓			CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	10	XBR1	✓		DAC0T0 DAC1T0 LPT0T0 INT0.0 INT1.0 WAKE.12	CMP0P.1 CMP1P.1 EXREGSP

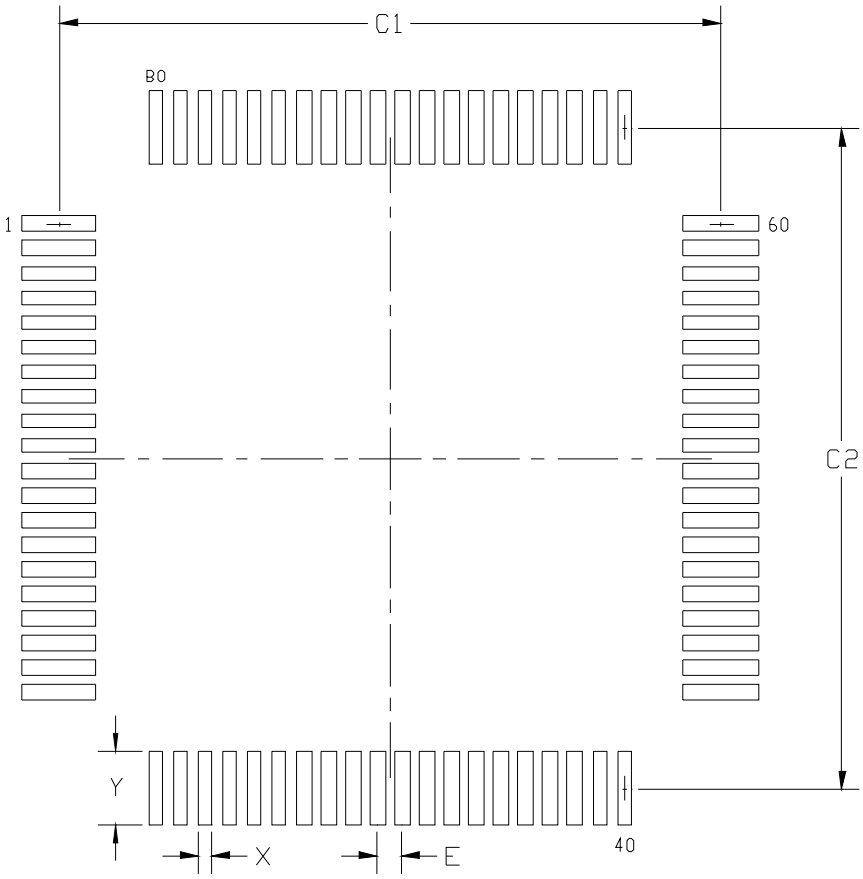

Figure 6.9. TQFP-80 Landing Diagram

Table 6.7. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.6. QFN-64 Package Specifications

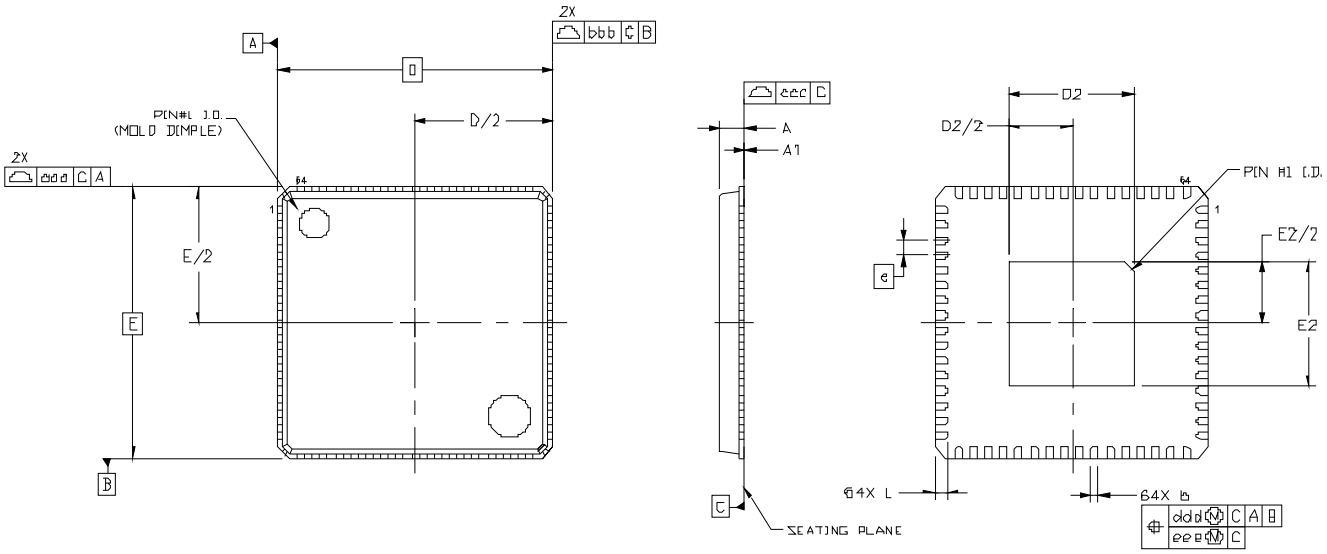

Figure 6.10. QFN-64 Package Drawing

Table 6.8. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.6.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

6.6.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.7.1. TQFP-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

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1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
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6.7.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
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