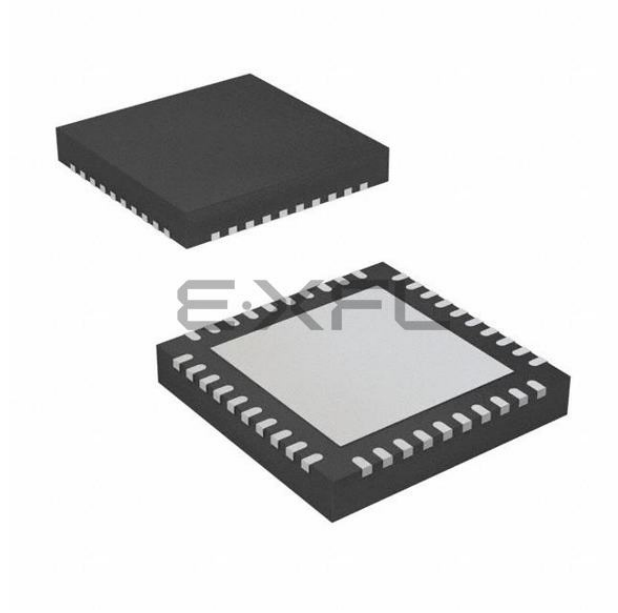

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c154-b-gm

1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3C1xx device family.

1.1.1. SiM3U1xx/SiM3C1xx Reference Manual

The Silicon Laboratories SiM3U1xx/SiM3C1xx Reference Manual provides detailed functional descriptions for the SiM3C1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3C1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vector Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm.m3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

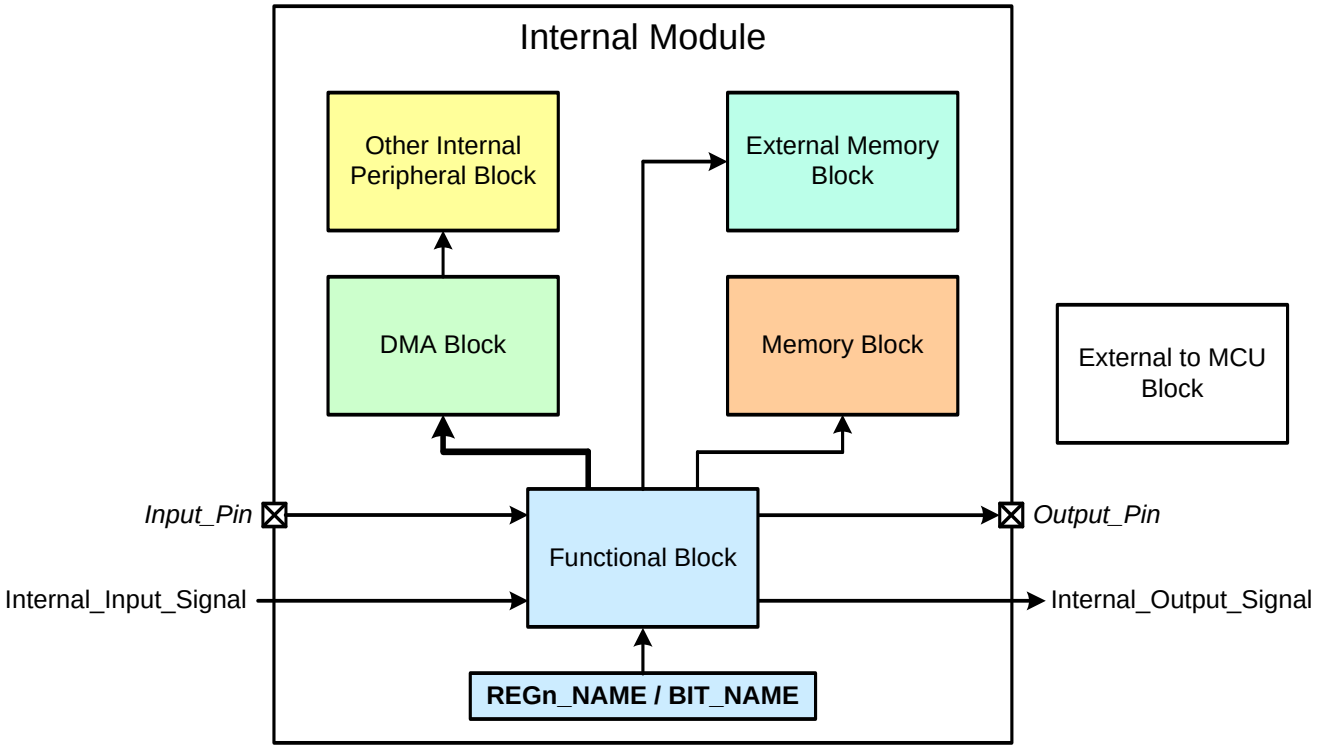


Figure 1.1. Block Diagram Conventions

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.10. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VDD)	V_{ADC}	High Speed Mode	2.2	—	3.6	V
		Low Power Mode	1.8	—	3.6	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode[2]	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

Table 3.10. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode[2]	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF =2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF =2.4 V	–1	0	1	LSB
Offset Temperatue Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error[3]	E_M	12 Bit Mode	–0.07	–0.02	0.02	%
Dynamic Performance with 10 kHz Sine Wave Input 1 dB below full scale, Max throughput						
Signal-to-Noise	SNR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	78	—	dB
		10 Bit Mode	—	77	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

Table 3.12. Capacitive Sense

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single Conversion Time (Default Configuration)	t_{single}	12-bit Mode	—	25	—	µs
		13-bit Mode	—	27	—	µs
		14-bit Mode	—	29	—	µs
		16-bit Mode	—	33	—	µs
Maximum External Capacitive Load	C_L	Highest Gain Setting (default)	—	45	—	pF
		Lowest Gain Setting	—	500	—	pF
Maximum External Series Impedance	C_L	Highest Gain Setting (default)	—	50	—	kΩ

Table 3.13. Current-to-Voltage Converter (IVC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (VDD)	V_{DDIVC}		2.2	—	3.6	V
Input Pin Voltage	V_{IN}		2.2	—	VDD	V
Minimum Input Current (source)	I_{IN}		100	—	—	µA
Integral Nonlinearity	INL_{IVC}		–0.6	—	0.6	%
Full Scale Output	V_{IVCOUT}		—	1.65	—	V
Slope	M_{IVC}	Input Range 1 mA (INxRANGE = 101)	1.55	1.65	1.75	V/mA
		Input Range 2 mA (INxRANGE = 100)	795	830	860	mV/mA
		Input Range 3 mA (INxRANGE = 011)	525	550	570	mV/mA
		Input Range 4 mA (INxRANGE = 010)	390	415	430	mV/mA
		Input Range 5 mA (INxRANGE = 001)	315	330	340	mV/mA
		Input Range 6 mA (INxRANGE = 000)	260	275	285	mV/mA
Settling Time to 0.1%	V_{IVCOUT}		—	—	500	ns

Table 3.16. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.4	—	mV
		CMPHYP = 01	—	4	—	mV
		CMPHYP = 10	—	8	—	mV
		CMPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.4	—	mV
		CMPHYN = 01	—	–4	—	mV
		CMPHYN = 10	—	–8	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}	PB2 Pins	—	7.5	—	pF
		PB3 Pins	—	10.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}		–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.19. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Voltage on I/O pins, Port Bank 3 I/O	V_{IN}	SiM3C1x7, PB3.0–PB3.7, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		SiM3C1x7, PB3.0–PB3.7, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		SiM3C1x7, PB3.8 - PB3.11	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
		SiM3C1x6, PB3.0–PB3.5, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		SiM3C1x6, PB3.0–PB3.5, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		SiM3C1x6, PB3.6–PB3.9	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
		SiM3C1x4, PB3.0–PB3.3	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
Total Current Sunk into Supply Pins	I_{SUPP}	V_{DD}, V_{REGIN}, V_{IO}, V_{IOHD}	—	400	mA
Total Current Sourced out of Ground Pins	I_{VSS}	V_{SS}, V_{SSHD}	400	—	mA
Current Sourced or Sunk by Any I/O Pin	I_{PIO}	PB0, PB1, PB2, PB3, and $\overline{\text{RESET}}$	–100	100	mA
		PB4	–300	300	mA
Current Injected on Any I/O Pin	I_{INJ}	PB0, PB1, PB2, PB3, and $\overline{\text{RESET}}$	–100	100	mA
		PB4	–300	300	mA
Total Injected Current on I/O Pins	ΣI_{INJ}	Sum of all I/O and $\overline{\text{RESET}}$	–400	400	mA

***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.

4. Precision32™ SiM3C1xx System Overview

The SiM3C1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 80 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB Flash; in-system programmable, 8–32 kB SRAM (including 4 kB retention SRAM, which preserves state in PM9 mode).
- **Power:**
  - Low drop-out (LDO) regulator for CPU core voltage.
  - Power-on reset circuit and brownout detectors.
  - 3.3 V output LDO for direct power from 5 V supplies.
  - External transistor regulator.
  - Power Management Unit (PMU).
- **I/O: Up to 65 total multifunction I/O pins:**
  - Up to six programmable high-power capable (5–300 mA with programmable current limiting, 1.8–5 V).
  - Up to twelve 5 V tolerant general purpose pins.
  - Two flexible peripheral crossbars for peripheral routing.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–80 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz and 2.5 MHz modes.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock modes.
  - Programmable clock divider allows any oscillator source to be divided by binary factor from 1-128.
- **Data Peripherals:**
  - 16-Channel DMA Controller.
  - 128/192/256-bit Hardware AES Encryption.
  - 16/32-bit CRC.
- **Timers/Counters and PWM:**
  - 6-channel Enhanced Programmable Counter Array (EPCAn) supporting advanced PWM and capture/compare.
  - 2 x 2-channel Standard Programmable Counter Array (PCAn) supporting PWM and capture/compare.
  - 2 x 32-bit Timers - can be split into 4 x 16-bit Timers, support PWM and capture/compare.
  - Real Time Clock (RTCn).
  - Low Power Timer.
  - Watchdog Timer.
- **Communications Peripherals:**
  - External Memory Interface.
  - 2 x USARTs and 2 x UARTs with IrDA and ISO7816 SmartCard support.
  - 3 x SPIs.
  - 2 x I2C.
  - I^2S (receive and transmit).
- **Analog:**
  - 2 x 12-Bit Analog-to-Digital Converters (SARADC).
  - 2 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 16-Channel Capacitance-to-Digital Converter (CAPSENSE).
  - 2 x Low-Current Comparators (CMP).
  - 1 x Current-to-Voltage Converter (IVC) module with two channels.
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the SiM3C1xx devices are truly standalone system-on-a-chip solutions. The Flash memory is reprogrammable in-circuit, providing non-

4.2. I/O

4.2.1. General Features

The SiM3C1xx ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB2 only) to generate simple square waves.
- A subset of pins can also serve as inputs to the Port Mapped Level Shifters available on the High Drive Pins.

4.2.2. High Drive Pins (PB4)

The High Drive pins have the following additional features:

- Programmable safe state: high, low, or high impedance.
- Programmable drive strength and slew rates.
- Programmable hardware current limiting.
- Powered from a separate source (VIOHD, which can be up to 6 V) from the rest of the device.
- Supports various functions, including GPIO, UART1 pins, EPCA0 pins, or Port Mapped Level Shifting.

4.2.3. 5 V Tolerant Pins (PB3)

The 5 V tolerant pins can be connected to external circuitry operating at voltages above the device supply without needing extra components to shift the voltage level.

4.2.4. Crossbars

The SiM3C1xx devices have two Crossbars with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The Crossbars have a fixed priority for each I/O function and assign these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the Crossbars skip that pin when assigning the next selected resource. Additionally, the Crossbars will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

5. Ordering Information

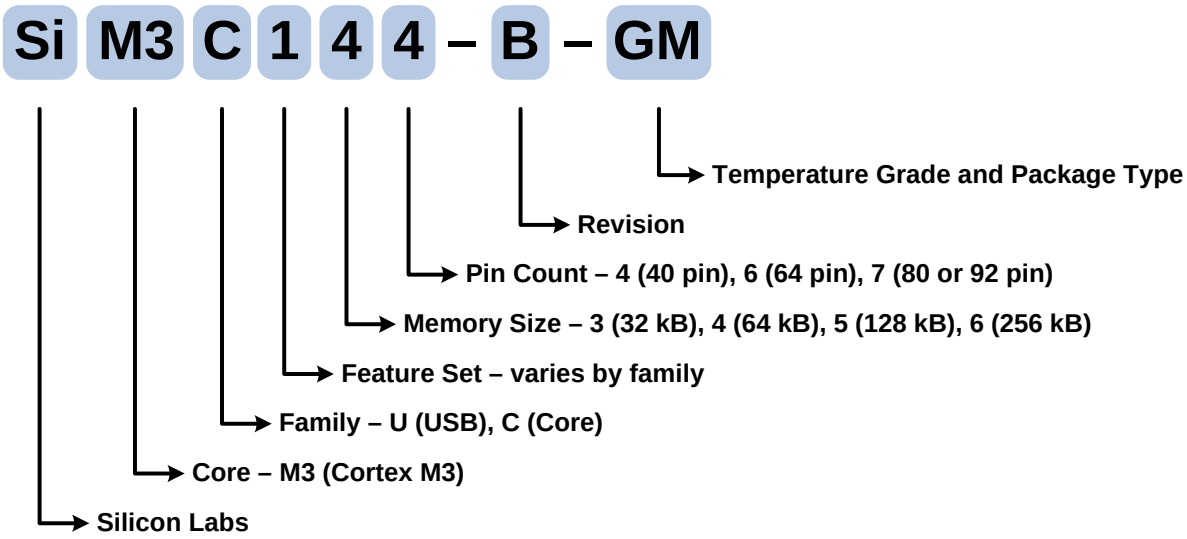


Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I^2S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	33 75	B15 B34							
VDD	Power (Core)	74	A44							
VIO	Power (I/O)	32 49 73	A19 A29 A43							
VREGIN	Power (Regulator)	76	A45							
VSSHD	Ground (High Drive)	4	B2							
VIOHD	Power (High Drive)	5	A3							
$\overline{\text{RESET}}$	Active-low Reset	80	A48							
SWCLK/TCK	Serial Wire/JTAG	45	B20							
SWDIO/TMS	Serial Wire/JTAG	44	A27							
PB0.0	Standard I/O	72	B33	XBR0	✓					ADC0.0
PB0.1	Standard I/O	71	B32	XBR0	✓					ADC0.1 CS0.0
PB0.2	Standard I/O	70	A42	XBR0	✓					ADC0.2 CS0.1
PB0.3	Standard I/O	69	B31	XBR0	✓					ADC0.3 CS0.2
PB0.4	Standard I/O	68	A41	XBR0	✓					ADC0.4 CS0.3
PB0.5	Standard I/O	67	B30	XBR0	✓					ADC0.5 CS0.4
PB0.6	Standard I/O	66	A40	XBR0	✓					CS0.5
PB0.7	Standard I/O	65	B29	XBR0	✓					ADC0.6 CS0.6 IVC0.0

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.9/ TRACECLK	Standard I/O /ETM	46	A28	XBR0	✓					ADC1.9
PB1.10	Standard I/O	43	A26	XBR0	✓	A23m/ A15			DMA0T1	ADC1.8
PB1.11	Standard I/O	42	A25	XBR0	✓	A22m/ A14			DMA0T0	ADC1.7
PB1.12	Standard I/O	41	D3	XBR0	✓	A21m/ A13				ADC1.6
PB1.13	Standard I/O	40	A24	XBR0	✓	A20m/ A12			ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.14	Standard I/O	39	A23	XBR0	✓	A19m/ A11			ADC1T15 WAKE.1	ADC1.4 CS0.11
PB1.15	Standard I/O	38	A22	XBR0	✓	A18m/ A10			WAKE.2	ADC1.3 CS0.12
PB2.0	Standard I/O	37	B17	XBR1	✓	A17m/ A9	LSI0	Yes	INT0.0 INT1.0 WAKE.3	ADC1.2 CS0.13
PB2.1	Standard I/O	36	A21	XBR1	✓	A16m/ A8	LSI1	Yes	INT0.1 INT1.1 WAKE.4	ADC1.1 CS0.14
PB2.2	Standard I/O	35	B16	XBR1	✓	AD15m/ A7	LSI2	Yes	INT0.2 INT1.2 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB2.3	Standard I/O	34	A20	XBR1	✓	AD14m/ A6	LSI3	Yes	INT0.3 INT1.3 WAKE.6	
PB2.4	Standard I/O	31	B14	XBR1	✓	AD13m/ A5	LSI4	Yes	INT0.4 INT1.4 WAKE.7	
PB2.5	Standard I/O	30	A18	XBR1	✓	AD12m / A4	LSI5	Yes	INT0.5 INT1.5	

6.2. SiM3C1x6 Pin Definitions

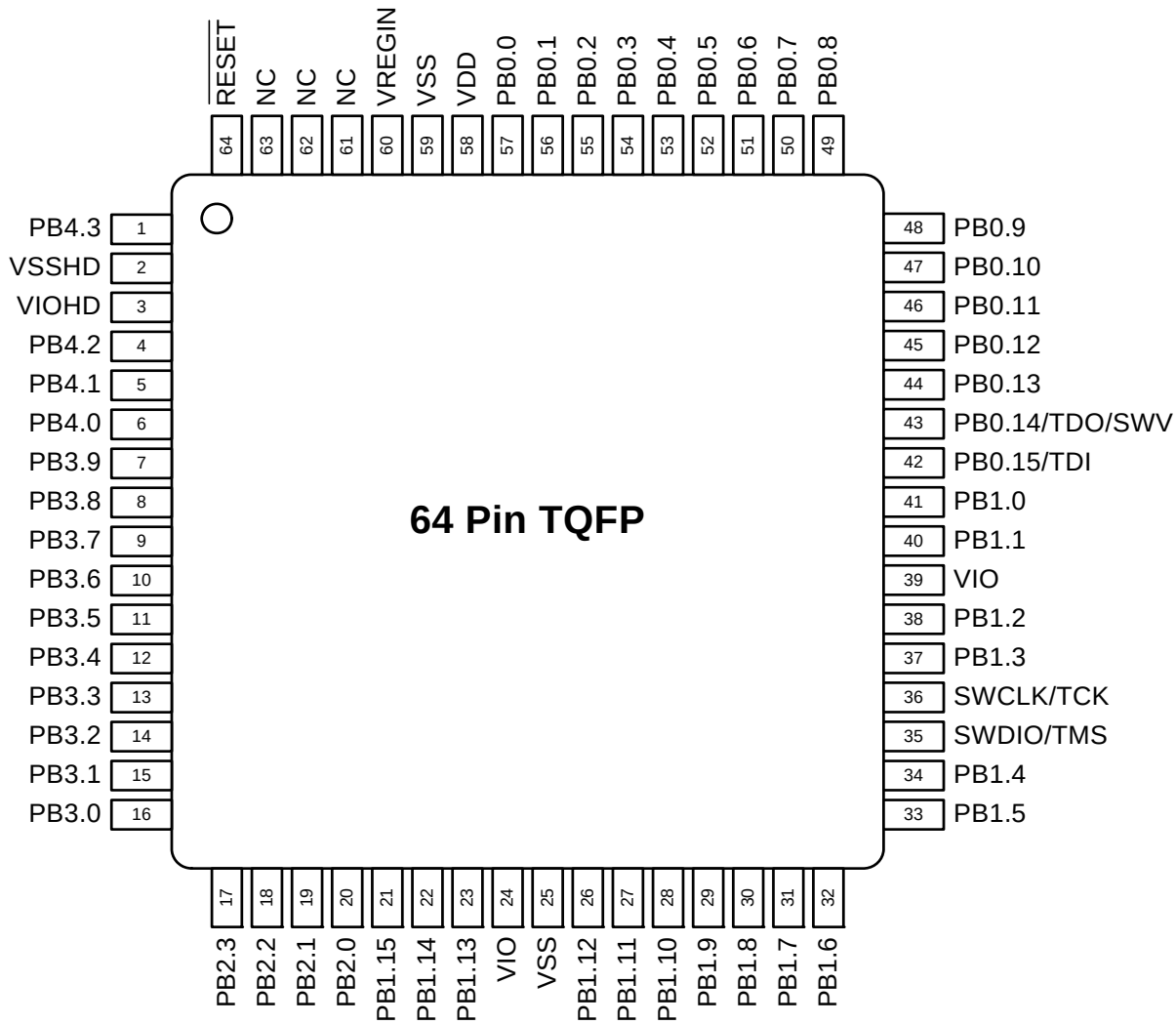


Figure 6.3. SiM3C1x6-GQ Pinout

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	25 59							
VDD	Power (Core)	58							
VIO	Power (I/O)	24 39							
VREGIN	Power (Regulator)	60							
VSSHD	Ground (High Drive)	2							
VIOHD	Power (High Drive)	3							
$\overline{\text{RESET}}$	Active-low Reset	64							
SWCLK/TCK	Serial Wire / JTAG	36							
SWDIO/TMS	Serial Wire / JTAG	35							
PB0.0	Standard I/O	57	XBR0	✓					ADC0.2 CS0.1
PB0.1	Standard I/O	56	XBR0	✓					ADC0.3 CS0.2
PB0.2	Standard I/O	55	XBR0	✓					ADC0.4 CS0.3
PB0.3	Standard I/O	54	XBR0	✓					ADC0.5 CS0.4
PB0.4	Standard I/O	53	XBR0	✓					ADC0.6 CS0.5 IVC0.0
PB0.5	Standard I/O	52	XBR0	✓					ADC0.7 CS0.6 IVC0.1
PB0.6	Standard I/O	51	XBR0	✓					ADC0.8 CS0.7 RTC1

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.7	Standard I/O	50	XBR0	✓					RTC2
PB0.8	Standard I/O	49	XBR0	✓					ADC0.9 VREFGND
PB0.9	Standard I/O	48	XBR0	✓					ADC0.10 VREF
PB0.10	Standard I/O	47	XBR0	✓					ADC1.6 IDAC0
PB0.11	Standard I/O	46	XBR0	✓					IDAC1
PB0.12	Standard I/O	45	XBR0	✓					XTAL1
PB0.13	Standard I/O	44	XBR0	✓					XTAL2
PB0.14/TDO/ SWV	Standard I/O / JTAG / Serial Wire Viewer	43	XBR0	✓					ADC0.12 ADC1.12
PB0.15/TDI	Standard I/O / JTAG	42	XBR0	✓					ADC0.13 ADC1.13
PB1.0	Standard I/O	41	XBR0	✓					ADC0.14 ADC1.14
PB1.1	Standard I/O	40	XBR0	✓					ADC0.15 ADC1.15
PB1.2	Standard I/O	38	XBR0	✓					ADC1.11 CS0.8
PB1.3	Standard I/O	37	XBR0	✓					ADC1.10 CS0.9
PB1.4	Standard I/O	34	XBR0	✓					ADC1.8
PB1.5	Standard I/O	33	XBR0	✓					ADC1.7
PB1.6	Standard I/O	32	XBR0	✓				ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.7	Standard I/O	31	XBR0	✓	AD15m/ A7			ADC1T15 WAKE.1	ADC1.4 CS0.11

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	14					
VDD	Power (Core)	35					
VIO	Power (I/O)	13					
VREGIN	Power (Regulator)	36					
VSSHD	Ground (High Drive)	2					
VIOHD	Power (High Drive)	3					
$\overline{\text{RESET}}$	Active-low Reset	40					
SWCLK	Serial Wire	24					
SWDIO	Serial Wire	23					
PB0.0	Standard I/O	34	XBR0	✓			ADC0.8 CS0.7 RTC1
PB0.1	Standard I/O	33	XBR0	✓			RTC2
PB0.2	Standard I/O	32	XBR0	✓			ADC0.9 CS0.0 VREFGND
PB0.3	Standard I/O	31	XBR0	✓			ADC0.10 CS0.1 VREF
PB0.4	Standard I/O	30	XBR0	✓			ADC1.6 CS0.2 IDAC0
PB0.5	Standard I/O	29					IDAC1
PB0.6	Standard I/O	28	XBR0	✓			ADC0.0 CS0.3 XTAL1
PB0.7	Standard I/O	27	XBR0	✓			ADC0.1 CS0.4 XTAL2

Table 6.10. TQFP-64 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

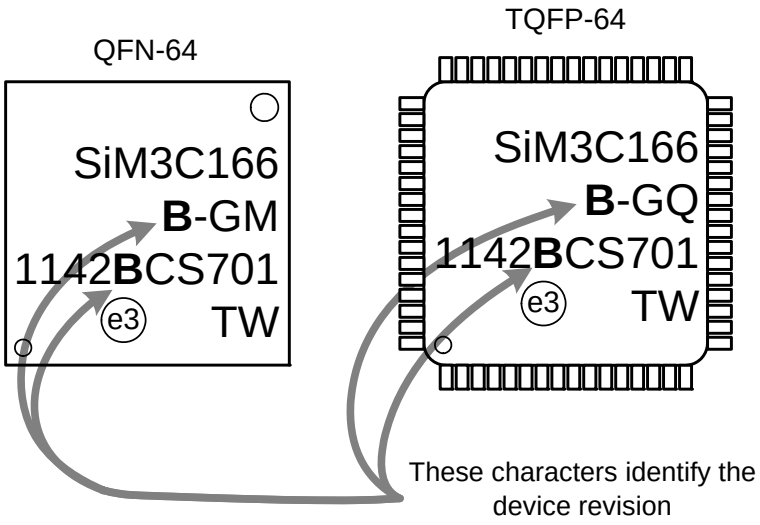


Figure 7.3. SiM3C1x6 Revision Information

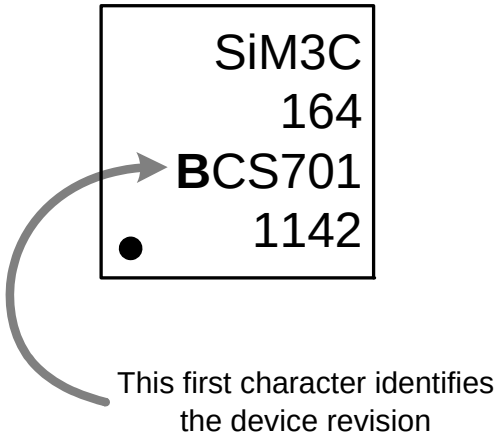


Figure 7.4. SiM3C1x4 Revision Information

7.2. Comparator Rising/Falling Edge Flags in Debug Mode (CMP0, CMP1)

7.2.1. Problem

On Revision A and Revision B devices, if the comparator output is high, the comparator rising and falling edge flags will both be set to 1 upon single-step or exit from debug mode.

7.2.2. Impacts

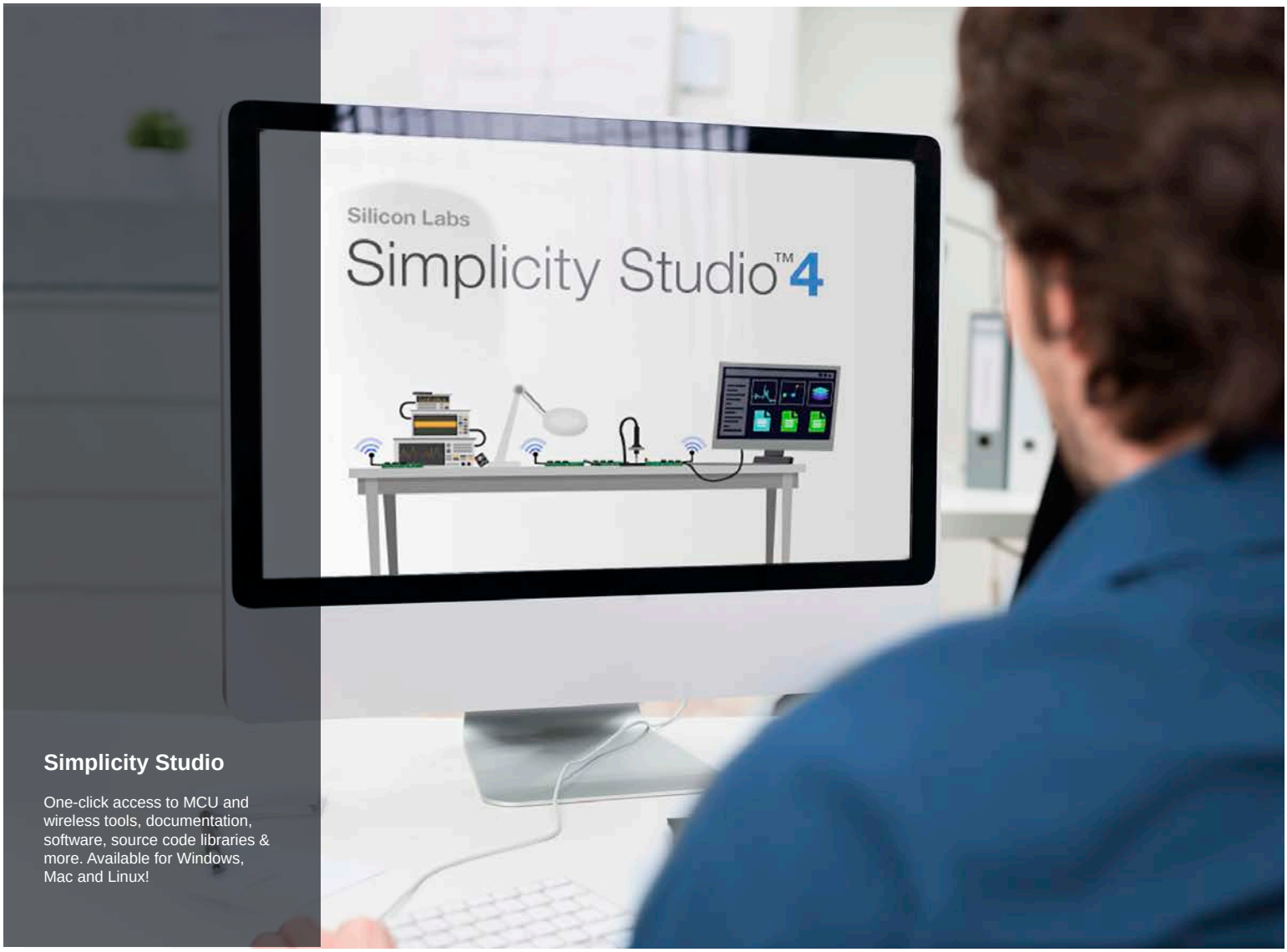
Firmware using the rising and falling edge flags to make decisions may see a false trigger of the comparator if the output of the comparator is high during a debug session. This does not impact the non-debug operation of the device.

7.2.3. Workaround

There is not a system-agnostic workaround for this issue.

7.2.4. Resolution

This issue exists on Revision A and Revision B devices. It may be corrected in a future device revision.



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