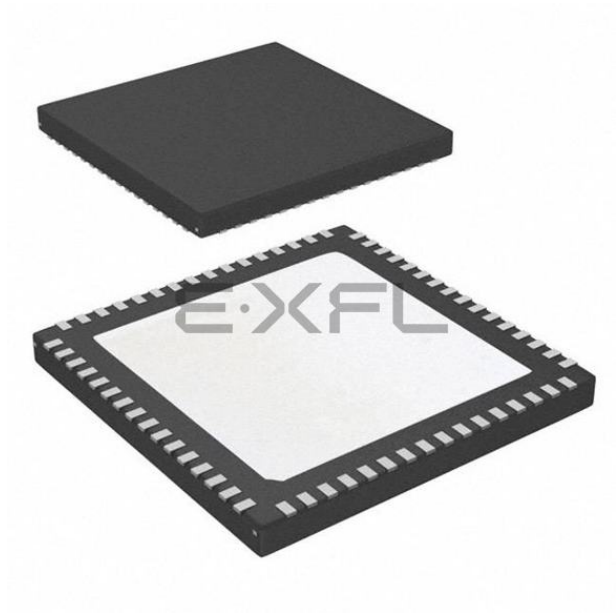

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Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c156-b-gmr

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 9[2,3]—Low Power Shutdown with VREG0 disabled, powered through VDD and VIO	I_{DD}	RTC Disabled, V_{DD} = 1.8 V, T_A = 25 °C	—	85	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 1.8 V, T_A = 25 °C	—	350	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 1.8 V, T_A = 25 °C	—	620	—	nA
		RTC Disabled, V_{DD} = 3.0 V, T_A = 25 °C	—	145	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 3.0 V, T_A = 25 °C	—	500	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 3.0 V, T_A = 25 °C	—	800	—	nA
Power Mode 9[2,3]—Low Power Shutdown with VREG0 in low-power mode, VDD and VIO powered through VREG0 (Includes VREG0 current)	I_{VREGIN}	RTC Disabled, VREGIN = 5 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, VREGIN = 5 V, T_A = 25 °C	—	650	—	nA
		RTC w/ 32.768 kHz Crystal, VREGIN = 5 V, T_A = 25 °C	—	950	—	nA
VIOHD Current (High-drive I/O disabled)	I_{VIOHD}	HV Mode (default)	—	2.5	5	µA
		LV Mode	—	2	—	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Peripheral Supply Currents						
Voltage Regulator (VREG0)	I_{VREGIN}	Normal Mode, T_A = 25 °C BGDIS = 0, SUSEN = 0	—	300	—	µA
		Normal Mode, T_A = 85 °C BGDIS = 0, SUSEN = 0	—	—	650	µA
		Suspend Mode, T_A = 25 °C BGDIS = 0, SUSEN = 1	—	75	—	µA
		Suspend Mode, T_A = 85 °C BGDIS = 0, SUSEN = 1	—	—	115	µA
		Sleep Mode, T_A = 25 °C BGDIS = 1, SUSEN = X	—	90	—	nA
		Sleep Mode, T_A = 85 °C BGDIS = 1, SUSEN = X	—	—	500	nA
Voltage Regulator (VREG0) Sense	$I_{VRSENSE}$	SENSEEN = 1	—	3	—	µA
External Regulator (EXTVREG0)	$I_{EXTVREG}$	Regulator	—	215	250	µA
		Current Sensor	—	7	—	µA
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 80 MHz	—	1.75	1.86	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	190	—	µA
		Operating at 2.5 MHz	—	40	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz, T_A = 25 °C	—	215	—	nA
		Operating at 16.4 kHz, T_A = 85 °C	—	—	500	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} High Supply Monitor Threshold (VDDHITHEN = 1)	V_{VDDMH}	Early Warning	2.10	2.20	2.30	V
		Reset	1.95	2.05	2.1	V
V_{DD} Low Supply Monitor Threshold (VDDHITHEN = 0)	V_{VDDML}	Early Warning	1.81	1.85	1.88	V
		Reset	1.70	1.74	1.77	V
V_{REGIN} Supply Monitor Threshold	V_{VREGM}	Early Warning	4.2	4.4	4.6	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.4	—	V
		Falling Voltage on V_{DD}	0.8	1	1.3	V
V_{DD} Ramp Time	t_{RMP}	Time to $V_{DD} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.4	1	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13	kHz
V_{DD} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.8. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Low Power Oscillator (LPOSC0)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz
		T_A = 25 °C, V_{DD} = 3.3 V	19.5	20	20.5	MHz
Divided Oscillator Frequency	f_{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz
Power Supply Sensitivity	PSS_{LPOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{LPOSC}	V_{DD} = 3.3 V	—	55	—	ppm/°C
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		T_A = 25 °C, V_{DD} = 3.3 V	15.8	16.4	17.3	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	2.4	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.3 V	—	0.2	—	%/°C
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%
***Note:** PLL0OSC in free-running oscillator mode.						

Table 3.9. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency*	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
External Crystal Clock Frequency	f_{XTAL}		0.01	—	30	MHz
***Note:** Minimum of 10 kHz during debug operations.						

Table 3.10. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VDD)	V_{ADC}	High Speed Mode	2.2	—	3.6	V
		Low Power Mode	1.8	—	3.6	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode[2]	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

Table 3.14. Voltage Reference Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{DD} = 1.8–3.6 V	1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-Chip Precision Reference (VREF0)						
Valid Supply Range	V_{DD}	VREF2X = 0	1.8	—	3.6	V
		VREF2X = 1	2.7	—	3.6	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.195	1.2	1.205	V
		25 °C ambient, VREF2X = 1	2.39	2.4	2.41	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	25	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 3.15. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	760	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	±14	—	mV
Slope	M		—	2.8	—	mV/°C
Slope Error*	E_M		—	±120	—	µV/°C
Linearity			—	1	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

Table 3.17. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard I/O (PB0, PB1, and PB2), 5 V Tolerant I/O (PB3), and $\overline{\text{RESET}}$						
Output High Voltage*	V_{OH}	Low Drive, I_{OH} = –2 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –5 mA	V_{IO} – 0.7	—	—	V
Output Low Voltage*	V_{OL}	Low Drive, I_{OL} = 3 mA	—	—	0.6	V
		High Drive, I_{OL} = 12.5 mA	—	—	0.6	V
Input High Voltage	V_{IH}	1.8 ≤ V_{IO} ≤ 2.0	0.7 x V_{IO}	—	—	V
		2.0 ≤ V_{IO} ≤ 3.6	V_{IO} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}	PB0, PB1 and PB2 Pins	—	4	—	pF
		PB3 Pins	—	7	—	pF
Weak Pull-Up Current (Input Voltage = 0 V)	I_{PU}	V_{IO} = 1.8	–6	–3.5	–2	µA
		V_{IO} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	0 ≤ V_{IN} ≤ V_{IO}	–1	—	1	µA
Input Leakage Current of Port Bank 3 I/O, V_{IN} above V_{IO}	I_L	V_{IO} < V_{IN} < V_{IO}+2.0 V (pins without EXREG functions)	0	5	150	µA
		V_{IO} < V_{IN} < V_{REGIN} (pins with EXREG functions)	0	5	150	µA
High Drive I/O (PB4)						
Output High Voltage	V_{OH}	Standard Mode, Low Drive, I_{OH} = –3 mA	V_{IOHD} – 0.7	—	—	V
		Standard Mode, High Drive, I_{OH} = –10 mA	V_{IOHD} – 0.7	—	—	V
Output Low Voltage	V_{OL}	Standard Mode, Low Drive, I_{OH} = 3 mA	—	—	0.6	V
		Standard Mode, High Drive, I_{OH} = 12.5 mA	—	—	0.6	V
Output Rise Time	t_R	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Fall Time	t_F	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs
Input High Voltage	V_{IH}	1.8 V≤ V_{IOHD} ≤ 2.0 V	0.7 x V_{IOHD}	—	—	V
		2.0 V≤ V_{IOHD} ≤ 6 V	V_{IOHD} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
N-Channel Sink Current Limit (2.7 V ≤ V_{IOHD} ≤ 6 V, V_{OL} = 0.8 V) See Figure 3.1	I_{SINKL}	Mode 0	—	1.75	—	mA
		Mode 1	—	2.5	—	
		Mode 2	—	3.5	—	
		Mode 3	—	4.75	—	
		Mode 4	—	7	—	
		Mode 5	—	9.5	—	
		Mode 6	—	14	—	
		Mode 7	—	18.75	—	
		Mode 8	—	28.25	—	
		Mode 9	—	37.5	—	
		Mode 10	—	56.25	—	
		Mode 11	—	75	—	
		Mode 12	—	112.5	—	
		Mode 13	—	150	—	
		Mode 14	—	225	—	
		Mode 15	—	300	—	
Total N-Channel Sink Current on P4.0-P4.5 (DC)	I_{SINKLT}		—	—	400	mA

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

4.1. Power

4.1.1. LDO and Voltage Regulator (VREG0)

The SiM3C1xx devices include two internal regulators: the core LDO Regulator and the Voltage Regulator (VREG0).

The LDO Regulator converts a 1.8–3.6 V supply to the core operating voltage of 1.8 V. This LDO consumes little power and provides flexibility in choosing a power supply for the system.

The Voltage Regulator regulates from 5.5 to 2.7 V and can serve as an input to the LDO. This allows the device to be powered from up to a 5.5 V supply without any external components other than bypass capacitors.

4.1.2. Voltage Supply Monitor (VMON0)

The SiM3C1xx devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware. The supply monitor includes additional circuitry that can monitor the main supply voltage and the VREGIN input voltage divided by 4 (VREGIN / 4).

The supply monitor module includes the following features:

- Main supply “VDD Low” (VDD below the early warning threshold) notification.
- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.
- VREGIN divided by 4 (VREGIN / 4) supply “VREGIN Low” notification.

4.1.3. External Regulator (EXTVREG0)

The External Regulator provides all the circuitry needed for a high-power regulator except the power transistor (NPN or PNP) and current sensing resistor (if current limiting is enabled).

The External Regulator module has the following features:

- Interfaces with either an NPN or PNP external transistor that serves as the pass device for the high current regulator.
- Automatic current limiting.
- Automatic foldback limiting.
- Sources up to 1 A for use by external circuitry.
- Variable output voltage from 1.8–3.6 V in 100 mV steps.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3C1xx manages the power systems of the device. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins. It also recognizes and manages the various wake sources for low-power modes of the device.

The PMU module includes the following features:

- Up to 16 pin wake inputs can wake the device from Power Mode 9.
- The Low Power Timer, RTC0 (alarms and oscillator fail), Comparator 0, and the $\overline{\text{RESET}}$ pin can also serve as wake sources for Power Mode 9.
- All PM9 wake sources (except for the $\overline{\text{RESET}}$ pin) can also reset the Low Power Timer or RTC0 modules.
- Disables the level shifters to pins and peripherals to further reduce power usage in PM9. These level shifters must be re-enabed by firmware after exiting PM9.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM9.

4.5. Counters/Timers and PWM

4.5.1. Programmable Counter Array (EPCA0, PCA0, PCA1)

The SiM3C1xx devices include two types of PCA module: Enhanced and Standard.

The Enhanced Programmable Counter Array (EPCA0) and Standard Programmable Counter Array (PCA0, PCA1) modules are timer/counter systems allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

The Enhanced PCA module is multi-purpose, but is optimized for motor control applications. The EPCA module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never both active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers and outputs.
- Pulse-Width Modulation (PWM) waveform generation.
- High-speed square wave generation.
- Input capture mode.
- DMA capability for both input capture and waveform generation.
- PWM generation halt input.

The Standard PCA module (PCA) includes the following features:

- Two independent channels.
- Center- and edge-aligned waveform generation.
- Programmable clock divisor and multiple options for clock source selection.
- Pulse-Width Modulation waveform generation.

4.5.2. 32-bit Timer (TIMER0, TIMER1)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.
- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

5. Ordering Information

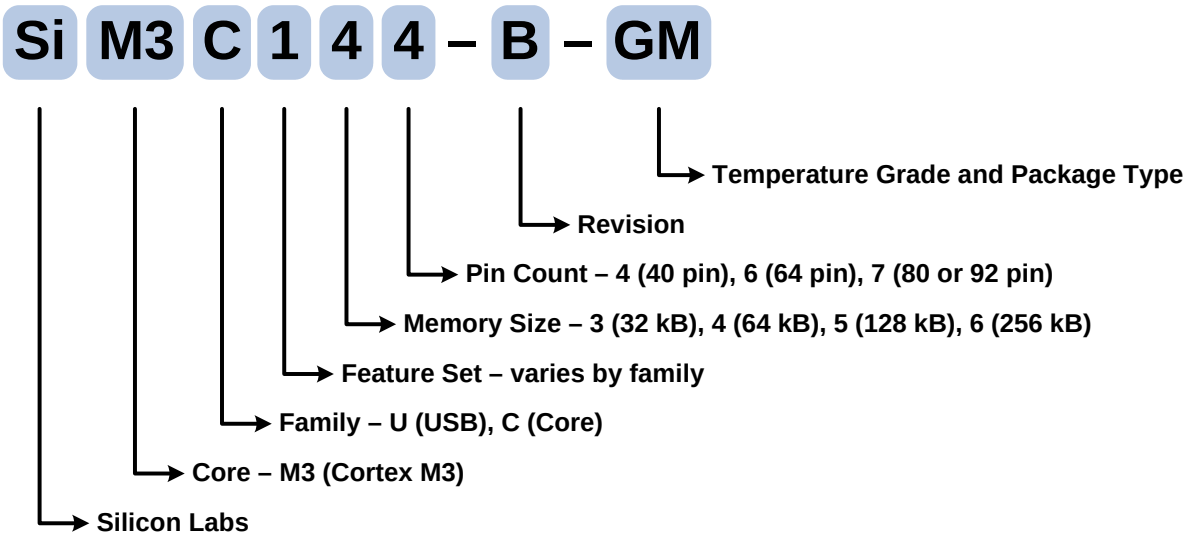


Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I^2S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	64	A39	XBR0	✓					ADC0.7 CS0.7 IVC0.1
PB0.9	Standard I/O	63	A38	XBR0	✓					ADC0.8 RTC1
PB0.10	Standard I/O	62	A37	XBR0	✓					RTC2
PB0.11	Standard I/O	61	D4	XBR0	✓					ADC0.9 VREFGND
PB0.12	Standard I/O	60	A36	XBR0	✓					ADC0.10 VREF
PB0.13	Standard I/O	59	A35	XBR0	✓					IDAC0
PB0.14	Standard I/O	58	B27	XBR0	✓					IDAC1
PB0.15	Standard I/O	57	A34	XBR0	✓					XTAL1
PB1.0	Standard I/O	56	A33	XBR0	✓					XTAL2
PB1.1	Standard I/O	55	B25	XBR0	✓					ADC0.11
PB1.2/TRST	Standard I/O /JTAG	54	A32	XBR0	✓					
PB1.3/TDO/ SWV	Standard I/O /JTAG/ Serial Wire Viewer	53	B24	XBR0	✓					ADC0.12 ADC1.12
PB1.4/TDI	Standard I/O /JTAG	52	A31	XBR0	✓					ADC0.13 ADC1.13
PB1.5/ETM0	Standard I/O /ETM	51	B23	XBR0	✓					ADC0.14 ADC1.14
PB1.6/ETM1	Standard I/O /ETM	50	A30	XBR0	✓					ADC0.15 ADC1.15
PB1.7/ETM2	Standard I/O /ETM	48	B22	XBR0	✓					ADC1.11 CS0.8
PB1.8/ETM3	Standard I/O /ETM	47	B21	XBR0	✓					ADC1.10 CS0.9

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.8	Standard I/O	30	XBR0	✓	AD14m/ A6			WAKE.2	ADC1.3 CS0.12
PB1.9	Standard I/O	29	XBR0	✓	AD13m/ A5			WAKE.3	ADC1.2 CS0.13
PB1.10	Standard I/O	28	XBR0	✓	AD12m/ A4			DMA0T1 WAKE.4	ADC1.1 CS0.14
PB1.11	Standard I/O	27	XBR0	✓	AD11m/ A3			DMA0T0 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.12	Standard I/O	26	XBR0	✓	AD10m/ A2			WAKE.6	
PB1.13	Standard I/O	23	XBR0	✓	AD9m/ A1				
PB1.14	Standard I/O	22	XBR0	✓	AD8m/ A0				
PB1.15	Standard I/O	21	XBR0	✓	AD7m/ D7				
PB2.0	Standard I/O	20	XBR1	✓	AD6m/ D6	LSI0	Yes	INT0.0 INT1.0	
PB2.1	Standard I/O	19	XBR1	✓	AD5m/ D5	LSI1	Yes	INT0.1 INT1.1	
PB2.2	Standard I/O	18	XBR1	✓	AD4m/ D4	LSI2	Yes	INT0.2 INT1.2	CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.3	Standard I/O	17	XBR1	✓	AD3m/ D3	LSI3	Yes	INT0.3 INT1.3	CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	16	XBR1	✓	AD2m/ D2				CMP0P.1 CMP1P.1
PB3.1	5 V Tolerant I/O	15	XBR1	✓	AD1m/ D1				CMP0N.1 CMP1N.1

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	14					
VDD	Power (Core)	35					
VIO	Power (I/O)	13					
VREGIN	Power (Regulator)	36					
VSSHD	Ground (High Drive)	2					
VIOHD	Power (High Drive)	3					
$\overline{\text{RESET}}$	Active-low Reset	40					
SWCLK	Serial Wire	24					
SWDIO	Serial Wire	23					
PB0.0	Standard I/O	34	XBR0	✓			ADC0.8 CS0.7 RTC1
PB0.1	Standard I/O	33	XBR0	✓			RTC2
PB0.2	Standard I/O	32	XBR0	✓			ADC0.9 CS0.0 VREFGND
PB0.3	Standard I/O	31	XBR0	✓			ADC0.10 CS0.1 VREF
PB0.4	Standard I/O	30	XBR0	✓			ADC1.6 CS0.2 IDAC0
PB0.5	Standard I/O	29					IDAC1
PB0.6	Standard I/O	28	XBR0	✓			ADC0.0 CS0.3 XTAL1
PB0.7	Standard I/O	27	XBR0	✓			ADC0.1 CS0.4 XTAL2

6.7. TQFP-64 Package Specifications

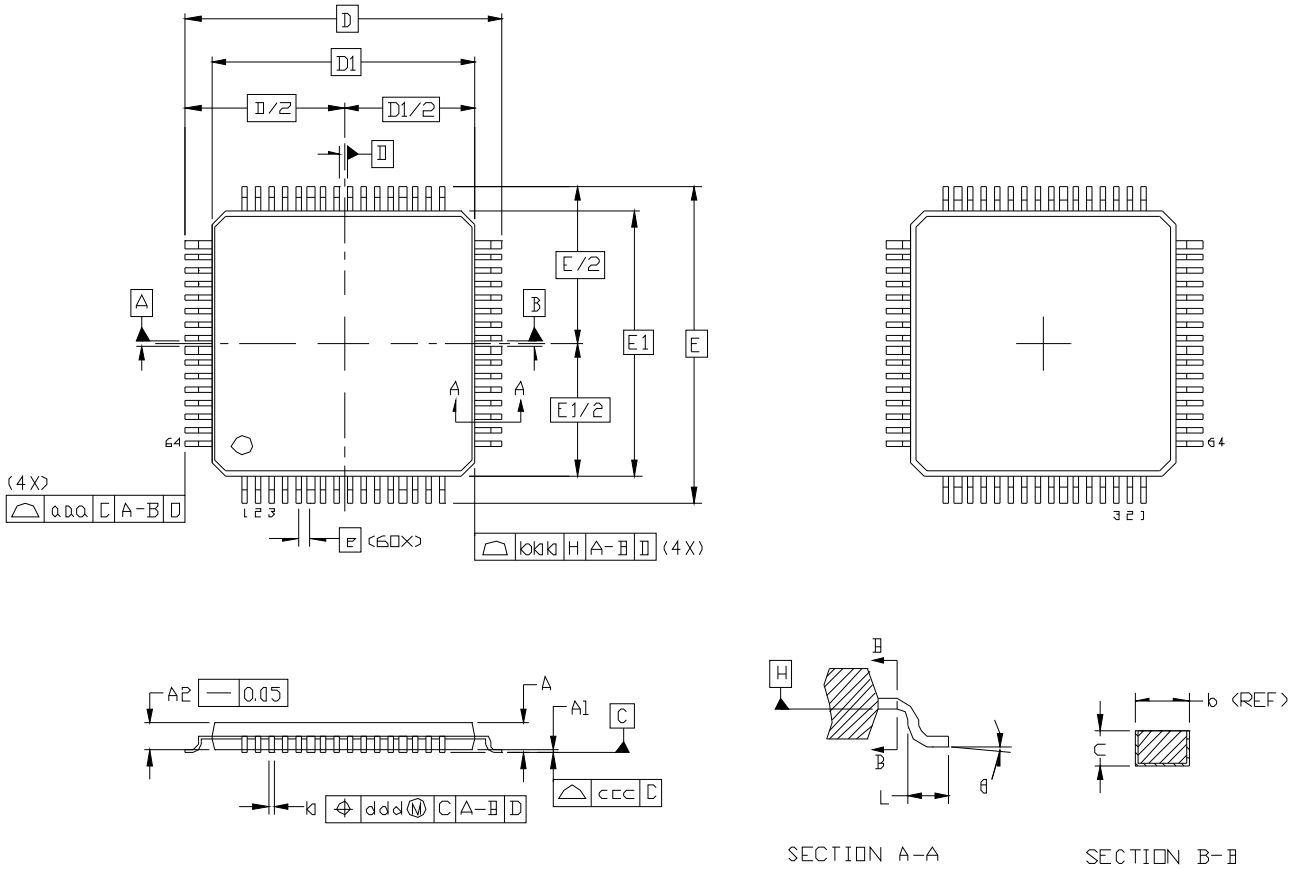


Figure 6.12. TQFP-64 Package Drawing

Table 6.10. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°

7. Revision Specific Behavior

This chapter details any known differences from behavior as stated in the device datasheet and reference manual. All known errata for the current silicon revision are rolled into this section at the time of publication. Any errata found after publication of this document will initially be detailed in a separate errata document until this datasheet is revised.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, 7.3, and 7.4 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

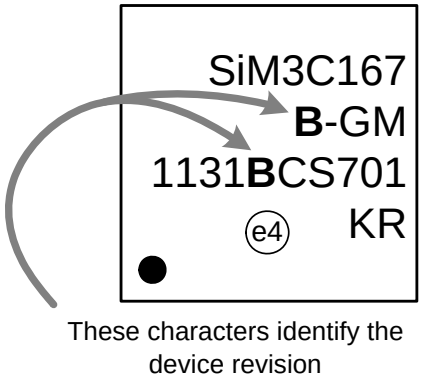


Figure 7.1. LGA-92 SiM3C1x7 Revision Information

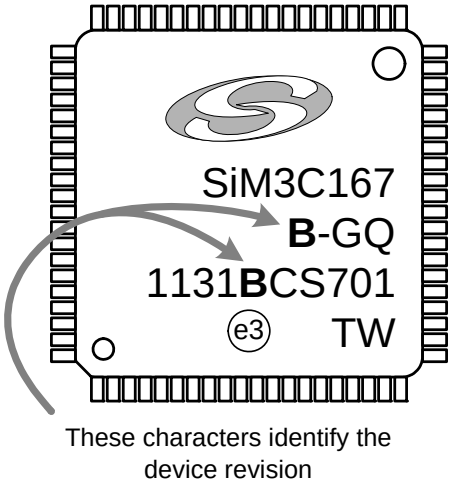


Figure 7.2. TQFP-80 SiM3C1x7 Revision Information

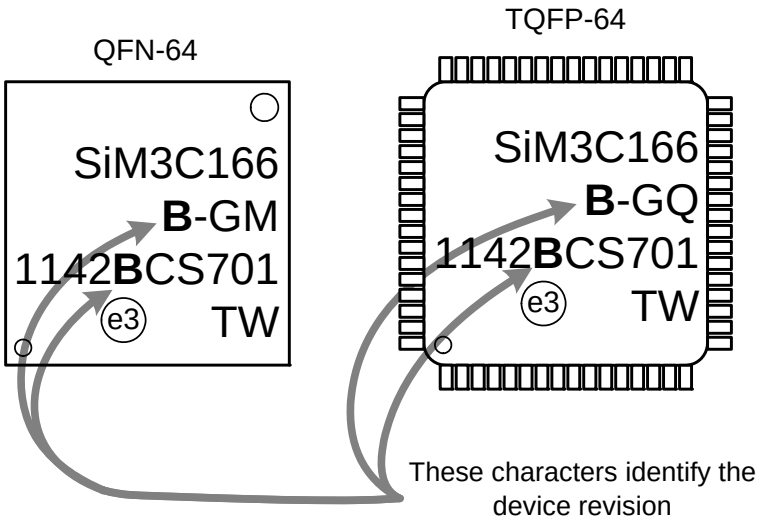


Figure 7.3. SiM3C1x6 Revision Information

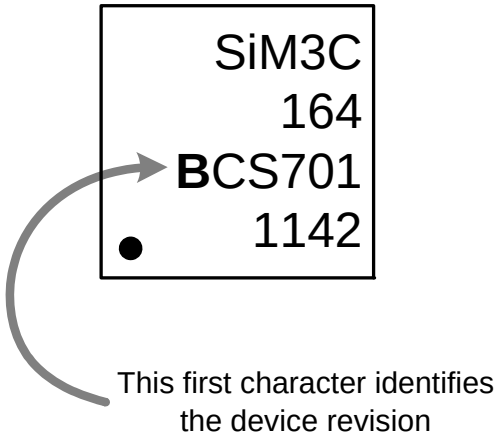


Figure 7.4. SiM3C1x4 Revision Information

7.2. Comparator Rising/Falling Edge Flags in Debug Mode (CMP0, CMP1)

7.2.1. Problem

On Revision A and Revision B devices, if the comparator output is high, the comparator rising and falling edge flags will both be set to 1 upon single-step or exit from debug mode.

7.2.2. Impacts

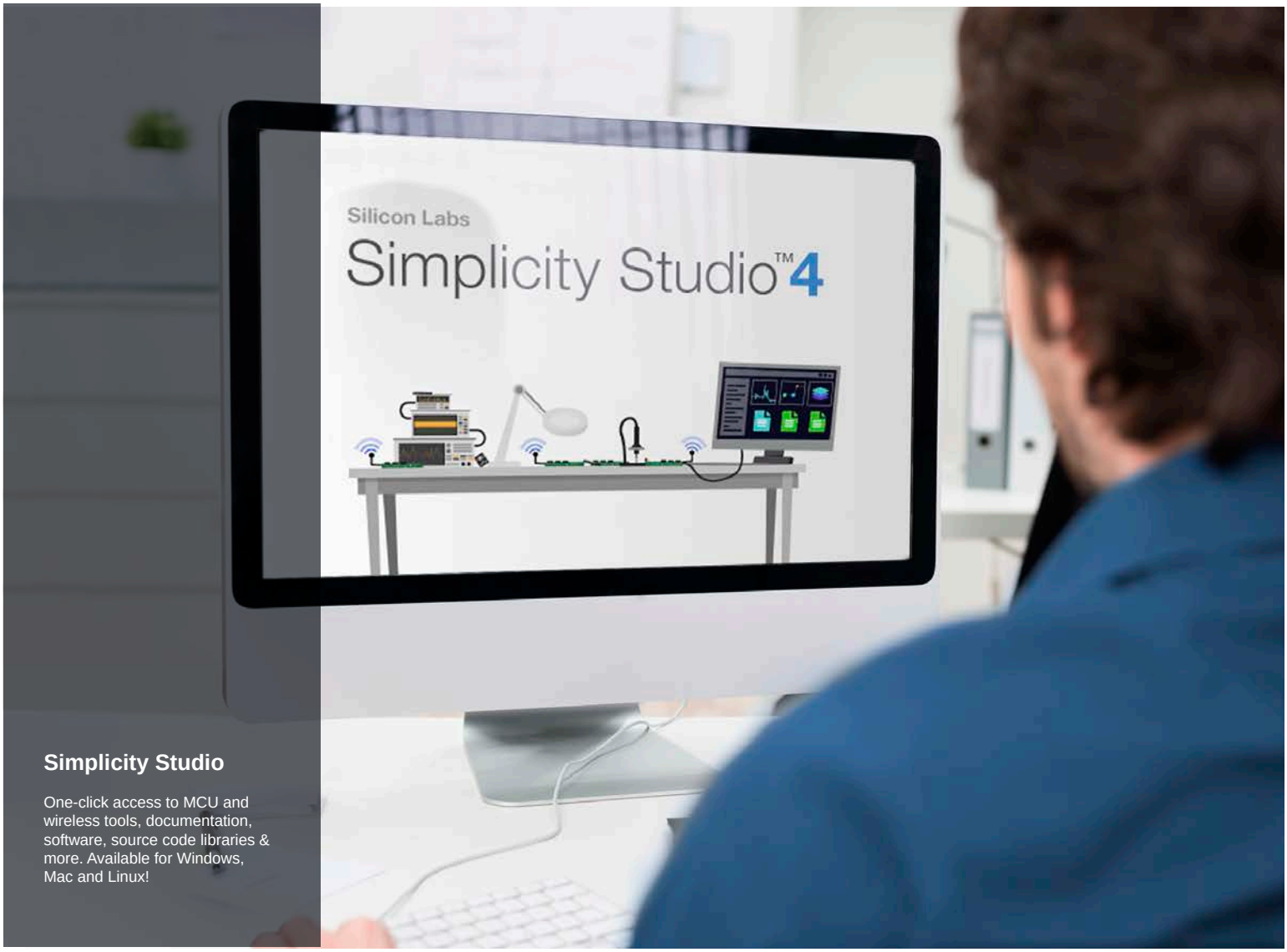
Firmware using the rising and falling edge flags to make decisions may see a false trigger of the comparator if the output of the comparator is high during a debug session. This does not impact the non-debug operation of the device.

7.2.3. Workaround

There is not a system-agnostic workaround for this issue.

7.2.4. Resolution

This issue exists on Revision A and Revision B devices. It may be corrected in a future device revision.



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