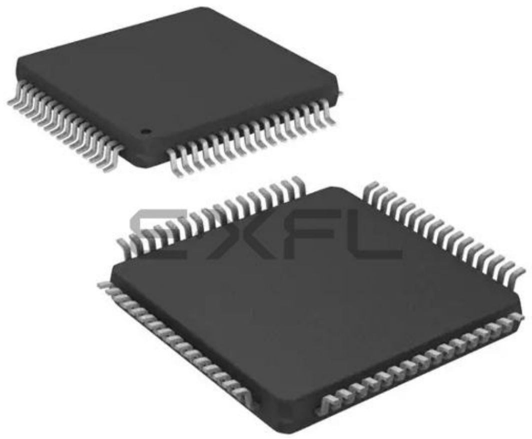


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c156-b-gq

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Oscillator (EXTOSC0)[8]	I_{EXTOSC}	FREQCN = 111	—	3.8	4.7	mA
		FREQCN = 110	—	840	950	µA
		FREQCN = 101	—	185	220	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	15	µA
		FREQCN = 001	—	5	10	µA
		FREQCN = 000	—	3	8	µA
SARADC0, SARADC1	I_{SARADC}	Sampling at 1 Msps, highest power mode settings.	—	1.2	1.5	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	510	µA
Temperature Sensor	I_{TSENSE}		—	75	105	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	750	µA
		Low Power Mode	—	160	190	µA
VREF0	I_{REFP}		—	75	100	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	—	µA
		CMPMD = 10	—	3	—	µA
		CMPMD = 01	—	10	—	µA
		CMPMD = 00	—	25	—	µA
Capacitive Sensing (CAPSENSE0)	I_{CS}	Continuous Conversions	—	55	80	µA
IDAC0[7], IDAC1[7]	I_{IDAC}		—	75	90	µA
IVC0[7]	I_{IVC}	$I_{IN} = 0$	—	1.5	2.5	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	25	µA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.7. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
V_{DD} Voltage During Programming	V_{PROG}		1.8	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During a sequential write operation, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 3.8. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency*	$f_{PLL0OSC}$	Full Temperature and Supply Range	77	79	80	MHz
Power Supply Sensitivity*	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 79 MHz	—	430	—	ppm/V
Temperature Sensitivity*	$TS_{PLL0OSC}$	V_{DD} = 3.3 V, Fout = 79 MHz	—	95	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	80	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 80 MHz, M=24, N=99, LOCKTH = 0	—	1.7	—	µs
		f_{REF} = 32 kHz, $f_{PLL0OSC}$ = 80 MHz, M=0, N=2440, LOCKTH = 0	—	91	—	µs

***Note:** PLL0OSC in free-running oscillator mode.

Table 3.12. Capacitive Sense

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single Conversion Time (Default Configuration)	t_{single}	12-bit Mode	—	25	—	µs
		13-bit Mode	—	27	—	µs
		14-bit Mode	—	29	—	µs
		16-bit Mode	—	33	—	µs
Maximum External Capacitive Load	C_L	Highest Gain Setting (default)	—	45	—	pF
		Lowest Gain Setting	—	500	—	pF
Maximum External Series Impedance	C_L	Highest Gain Setting (default)	—	50	—	kΩ

Table 3.13. Current-to-Voltage Converter (IVC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (VDD)	V_{DDIVC}		2.2	—	3.6	V
Input Pin Voltage	V_{IN}		2.2	—	VDD	V
Minimum Input Current (source)	I_{IN}		100	—	—	µA
Integral Nonlinearity	INL_{IVC}		–0.6	—	0.6	%
Full Scale Output	V_{IVCOUT}		—	1.65	—	V
Slope	M_{IVC}	Input Range 1 mA (INxRANGE = 101)	1.55	1.65	1.75	V/mA
		Input Range 2 mA (INxRANGE = 100)	795	830	860	mV/mA
		Input Range 3 mA (INxRANGE = 011)	525	550	570	mV/mA
		Input Range 4 mA (INxRANGE = 010)	390	415	430	mV/mA
		Input Range 5 mA (INxRANGE = 001)	315	330	340	mV/mA
		Input Range 6 mA (INxRANGE = 000)	260	275	285	mV/mA
Settling Time to 0.1%	V_{IVCOUT}		—	—	500	ns

Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Fall Time	t_F	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs
Input High Voltage	V_{IH}	1.8 V≤ V_{IOHD} ≤ 2.0 V	0.7 x V_{IOHD}	—	—	V
		2.0 V≤ V_{IOHD} ≤ 6 V	V_{IOHD} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
N-Channel Sink Current Limit (2.7 V ≤ V_{IOHD} ≤ 6 V, V_{OL} = 0.8 V) See Figure 3.1	I_{SINKL}	Mode 0	—	1.75	—	mA
		Mode 1	—	2.5	—	
		Mode 2	—	3.5	—	
		Mode 3	—	4.75	—	
		Mode 4	—	7	—	
		Mode 5	—	9.5	—	
		Mode 6	—	14	—	
		Mode 7	—	18.75	—	
		Mode 8	—	28.25	—	
		Mode 9	—	37.5	—	
		Mode 10	—	56.25	—	
		Mode 11	—	75	—	
		Mode 12	—	112.5	—	
		Mode 13	—	150	—	
		Mode 14	—	225	—	
		Mode 15	—	300	—	
Total N-Channel Sink Current on P4.0-P4.5 (DC)	I_{SINKLT}		—	—	400	mA

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
P-Channel Source Current Limit (2.7 V ≤ VIOHD ≤ 6 V, V_{OH} = VIOHD – 0.8 V) See Figure 3.2	I_{SRCL}	Mode 0	—	0.8	—	mA
		Mode 1	—	1.25	—	
		Mode 2	—	1.75	—	
		Mode 3	—	2.5	—	
		Mode 4	—	3.5	—	
		Mode 5	—	4.75	—	
		Mode 6	—	7	—	
		Mode 7	—	9.5	—	
		Mode 8	—	14	—	
		Mode 9	—	18.75	—	
		Mode 10	—	28.25	—	
		Mode 11	—	37.5	—	
		Mode 12	—	56.25	—	
		Mode 13	—	75	—	
		Mode 14	—	112.5	—	
		Mode 15	—	150	—	
Total P-Channel Source Current on P4.0-P4.5 (DC)	I_{SRCLT}		—	—	400	mA
Pin Capacitance	C_{IO}		—	30	—	pF
Weak Pull-Up Current in Low Voltage Mode	I_{PU}	V_{IOHD} = 1.8 V	–6	–3.5	–2	µA
		V_{IOHD} = 3.6 V	–30	–20	–10	µA
Weak Pull-Up Current in High Voltage Mode	I_{PU}	V_{IOHD} = 2.7 V	–15	–10	–5	µA
		V_{IOHD} = 6 V	–30	–20	–10	µA
Input Leakage (Pullups off)	I_{LK}		–1	—	1	µA
***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.						

4.1. Power

4.1.1. LDO and Voltage Regulator (VREG0)

The SiM3C1xx devices include two internal regulators: the core LDO Regulator and the Voltage Regulator (VREG0).

The LDO Regulator converts a 1.8–3.6 V supply to the core operating voltage of 1.8 V. This LDO consumes little power and provides flexibility in choosing a power supply for the system.

The Voltage Regulator regulates from 5.5 to 2.7 V and can serve as an input to the LDO. This allows the device to be powered from up to a 5.5 V supply without any external components other than bypass capacitors.

4.1.2. Voltage Supply Monitor (VMON0)

The SiM3C1xx devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware. The supply monitor includes additional circuitry that can monitor the main supply voltage and the VREGIN input voltage divided by 4 (VREGIN / 4).

The supply monitor module includes the following features:

- Main supply “VDD Low” (VDD below the early warning threshold) notification.
- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.
- VREGIN divided by 4 (VREGIN / 4) supply “VREGIN Low” notification.

4.1.3. External Regulator (EXTVREG0)

The External Regulator provides all the circuitry needed for a high-power regulator except the power transistor (NPN or PNP) and current sensing resistor (if current limiting is enabled).

The External Regulator module has the following features:

- Interfaces with either an NPN or PNP external transistor that serves as the pass device for the high current regulator.
- Automatic current limiting.
- Automatic foldback limiting.
- Sources up to 1 A for use by external circuitry.
- Variable output voltage from 1.8–3.6 V in 100 mV steps.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3C1xx manages the power systems of the device. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins. It also recognizes and manages the various wake sources for low-power modes of the device.

The PMU module includes the following features:

- Up to 16 pin wake inputs can wake the device from Power Mode 9.
- The Low Power Timer, RTC0 (alarms and oscillator fail), Comparator 0, and the $\overline{\text{RESET}}$ pin can also serve as wake sources for Power Mode 9.
- All PM9 wake sources (except for the $\overline{\text{RESET}}$ pin) can also reset the Low Power Timer or RTC0 modules.
- Disables the level shifters to pins and peripherals to further reduce power usage in PM9. These level shifters must be re-enabed by firmware after exiting PM9.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM9.

4.2. I/O

4.2.1. General Features

The SiM3C1xx ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB2 only) to generate simple square waves.
- A subset of pins can also serve as inputs to the Port Mapped Level Shifters available on the High Drive Pins.

4.2.2. High Drive Pins (PB4)

The High Drive pins have the following additional features:

- Programmable safe state: high, low, or high impedance.
- Programmable drive strength and slew rates.
- Programmable hardware current limiting.
- Powered from a separate source (VIOHD, which can be up to 6 V) from the rest of the device.
- Supports various functions, including GPIO, UART1 pins, EPCA0 pins, or Port Mapped Level Shifting.

4.2.3. 5 V Tolerant Pins (PB3)

The 5 V tolerant pins can be connected to external circuitry operating at voltages above the device supply without needing extra components to shift the voltage level.

4.2.4. Crossbars

The SiM3C1xx devices have two Crossbars with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The Crossbars have a fixed priority for each I/O function and assign these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the Crossbars skip that pin when assigning the next selected resource. Additionally, the Crossbars will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

4.7. Analog

4.7.1. 12-Bit Analog-to-Digital Converters (SARADC0, SARADC1)

The SARADC0 and SARADC1 modules on SiM3C1xx devices are Successive Approximation Register (SAR) Analog to Digital Converters (ADCs). The key features of the SARADC module are:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- Output data window comparator allows automatic range checking.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to 8 sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Multiple SARADC modules can work together synchronously or by interleaving samples.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.7.2. Sample Sync Generator (SSG0)

The SSG module includes a phase counter and a pulse generator. The phase counter is a 4-bit free-running counter clocked from the SARADC module clock. Counting-up from zero, the phase counter marks sixteen equally-spaced events for any number of SARADC modules. The ADCs can use this phase counter to start a conversion. The programmable pulse generator creates a 50% duty cycle pulse with a period of 16 phase counter ticks. Up to four programmable outputs available to external devices can be driven by the pulse generator with programmable polarity and a defined output setting when the pulse generator is stopped.

The Sample Sync Generator module has the following features:

- Connects multiple modules together to perform synchronized actions.
- Outputs a clock synchronized to the internal sampling clock used by any number of SARADC modules to pins for use by external devices.
- Includes a phase counter, pulse generator, and up to four programmable outputs.

4.7.3. 10-Bit Digital-to-Analog Converter (IDAC0, IDAC1)

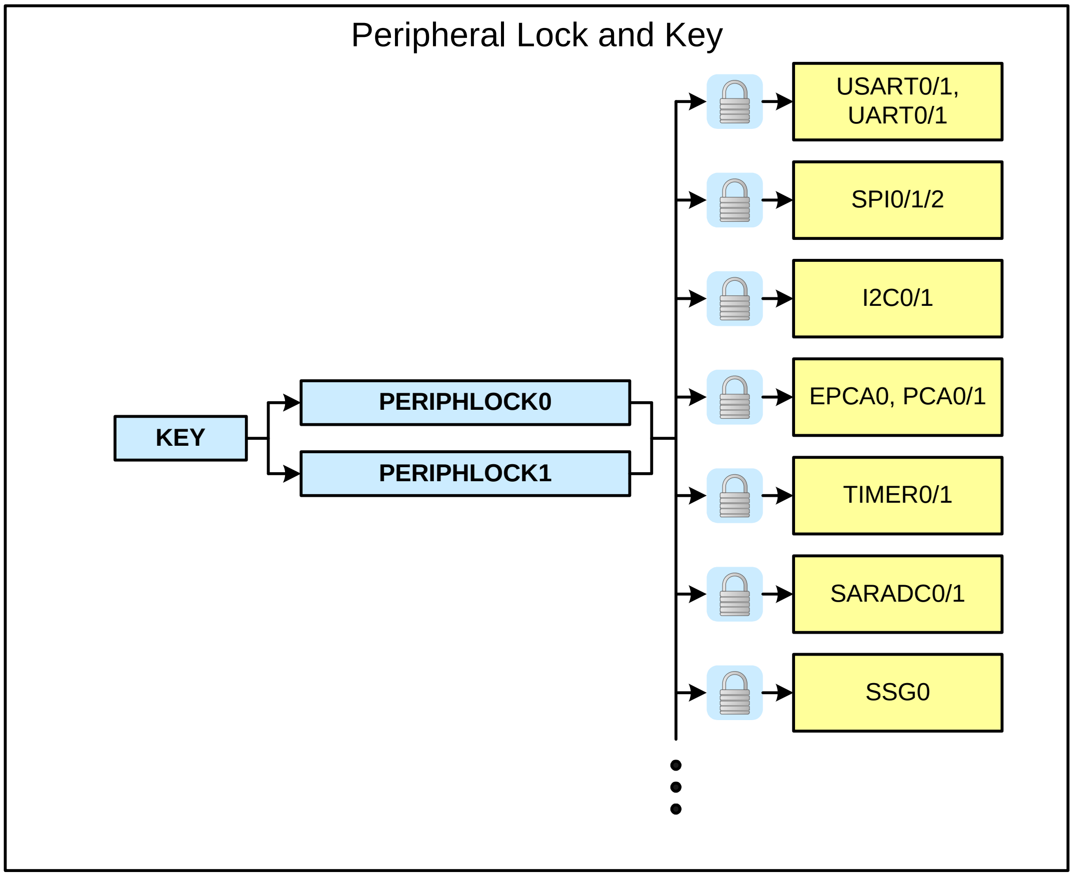
The IDAC takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O, on demand, and SSG0 output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources (DACnTx).
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.



4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabiites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.

5. Ordering Information

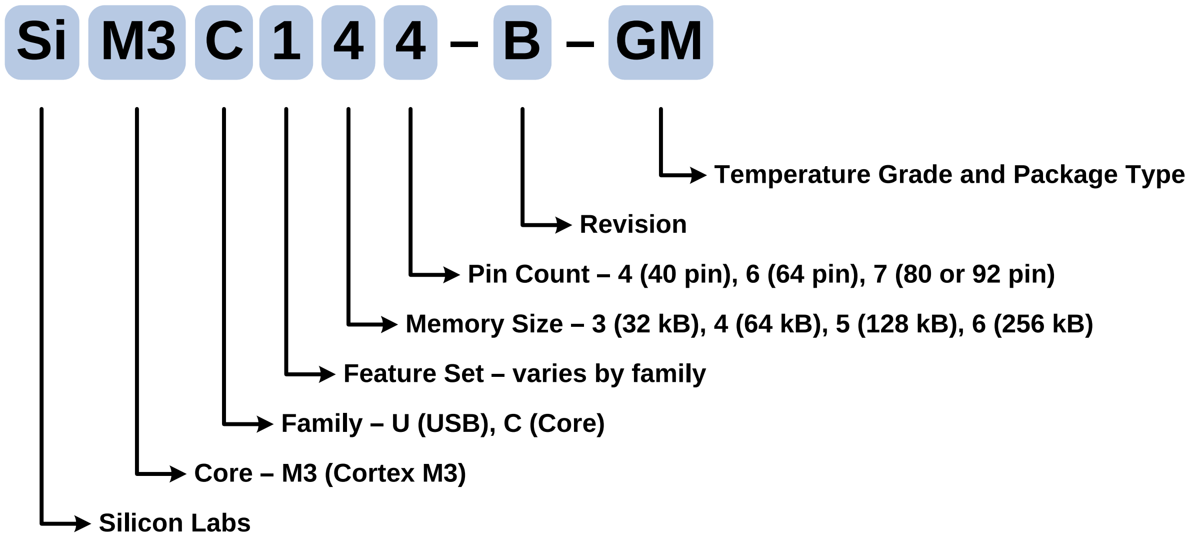


Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I^2S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

Table 5.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (kB)	External Memory Interface (EMIF)	Maximum Number of EMIF Address/Data Pins	Digital Port I/Os (Total)	Digital Port I/Os with High Drive Capability	Number of SARADC0 Channels	Number of SARADC1 Channels	Number of CAPSENSE0 Channels	Number of Comparator 0/1 Inputs (+/-)	Number of PMU Pin Wake Sources	JTAG Debugging Interface	ETM Debugging Interface	Serial Wire Debugging Interface	Lead-free (RoHS Compliant)	Package
SiM3C167-B-GM	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	LGA-92
SiM3C167-B-GQ	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	TQFP-80
SiM3C166-B-GM	256	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C166-B-GQ	256	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C164-B-GM	256	32			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C157-B-GM	128	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	LGA-92
SiM3C157-B-GQ	128	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	TQFP-80
SiM3C156-B-GM	128	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C156-B-GQ	128	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C154-B-GM	128	32			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C146-B-GM	64	16	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C146-B-GQ	64	16	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C144-B-GM	64	16			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C136-B-GM	32	8	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C136-B-GQ	32	8	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C134-B-GM	32	8			28	4	7	11	12	3/3	10			✓	✓	QFN-40

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	33 75	B15 B34							
VDD	Power (Core)	74	A44							
VIO	Power (I/O)	32 49 73	A19 A29 A43							
VREGIN	Power (Regulator)	76	A45							
VSSHD	Ground (High Drive)	4	B2							
VIOHD	Power (High Drive)	5	A3							
$\overline{\text{RESET}}$	Active-low Reset	80	A48							
SWCLK/TCK	Serial Wire/JTAG	45	B20							
SWDIO/TMS	Serial Wire/JTAG	44	A27							
PB0.0	Standard I/O	72	B33	XBR0	✓					ADC0.0
PB0.1	Standard I/O	71	B32	XBR0	✓					ADC0.1 CS0.0
PB0.2	Standard I/O	70	A42	XBR0	✓					ADC0.2 CS0.1
PB0.3	Standard I/O	69	B31	XBR0	✓					ADC0.3 CS0.2
PB0.4	Standard I/O	68	A41	XBR0	✓					ADC0.4 CS0.3
PB0.5	Standard I/O	67	B30	XBR0	✓					ADC0.5 CS0.4
PB0.6	Standard I/O	66	A40	XBR0	✓					CS0.5
PB0.7	Standard I/O	65	B29	XBR0	✓					ADC0.6 CS0.6 IVC0.0

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	64	A39	XBR0	✓					ADC0.7 CS0.7 IVC0.1
PB0.9	Standard I/O	63	A38	XBR0	✓					ADC0.8 RTC1
PB0.10	Standard I/O	62	A37	XBR0	✓					RTC2
PB0.11	Standard I/O	61	D4	XBR0	✓					ADC0.9 VREFGND
PB0.12	Standard I/O	60	A36	XBR0	✓					ADC0.10 VREF
PB0.13	Standard I/O	59	A35	XBR0	✓					IDAC0
PB0.14	Standard I/O	58	B27	XBR0	✓					IDAC1
PB0.15	Standard I/O	57	A34	XBR0	✓					XTAL1
PB1.0	Standard I/O	56	A33	XBR0	✓					XTAL2
PB1.1	Standard I/O	55	B25	XBR0	✓					ADC0.11
PB1.2/TRST	Standard I/O /JTAG	54	A32	XBR0	✓					
PB1.3/TDO/ SWV	Standard I/O /JTAG/ Serial Wire Viewer	53	B24	XBR0	✓					ADC0.12 ADC1.12
PB1.4/TDI	Standard I/O /JTAG	52	A31	XBR0	✓					ADC0.13 ADC1.13
PB1.5/ETM0	Standard I/O /ETM	51	B23	XBR0	✓					ADC0.14 ADC1.14
PB1.6/ETM1	Standard I/O /ETM	50	A30	XBR0	✓					ADC0.15 ADC1.15
PB1.7/ETM2	Standard I/O /ETM	48	B22	XBR0	✓					ADC1.11 CS0.8
PB1.8/ETM3	Standard I/O /ETM	47	B21	XBR0	✓					ADC1.10 CS0.9

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

6.3. SiM3C1x4 Pin Definitions

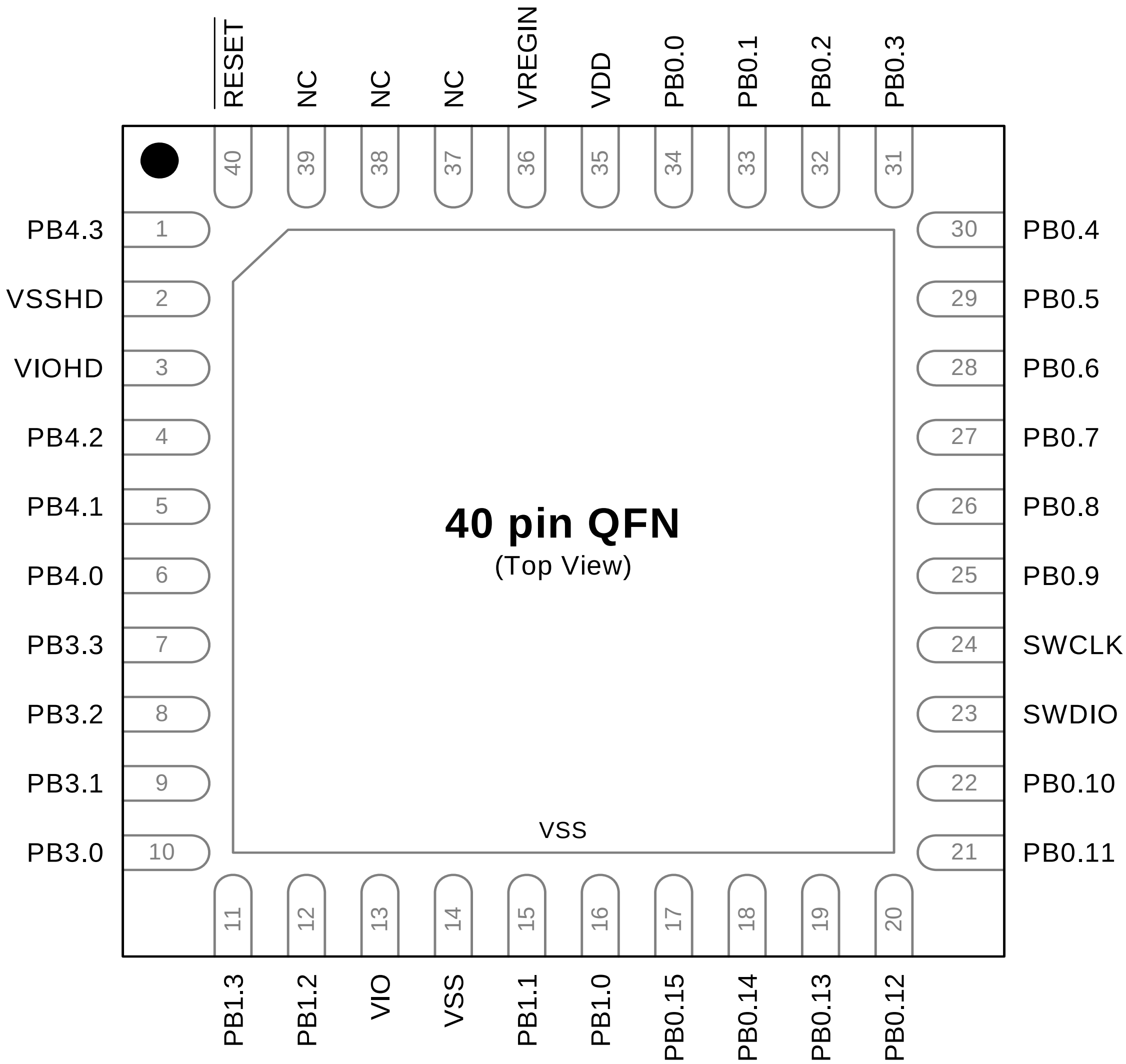


Figure 6.5. SiM3C1x4-GM Pinout

6.4. LGA-92 Package Specifications

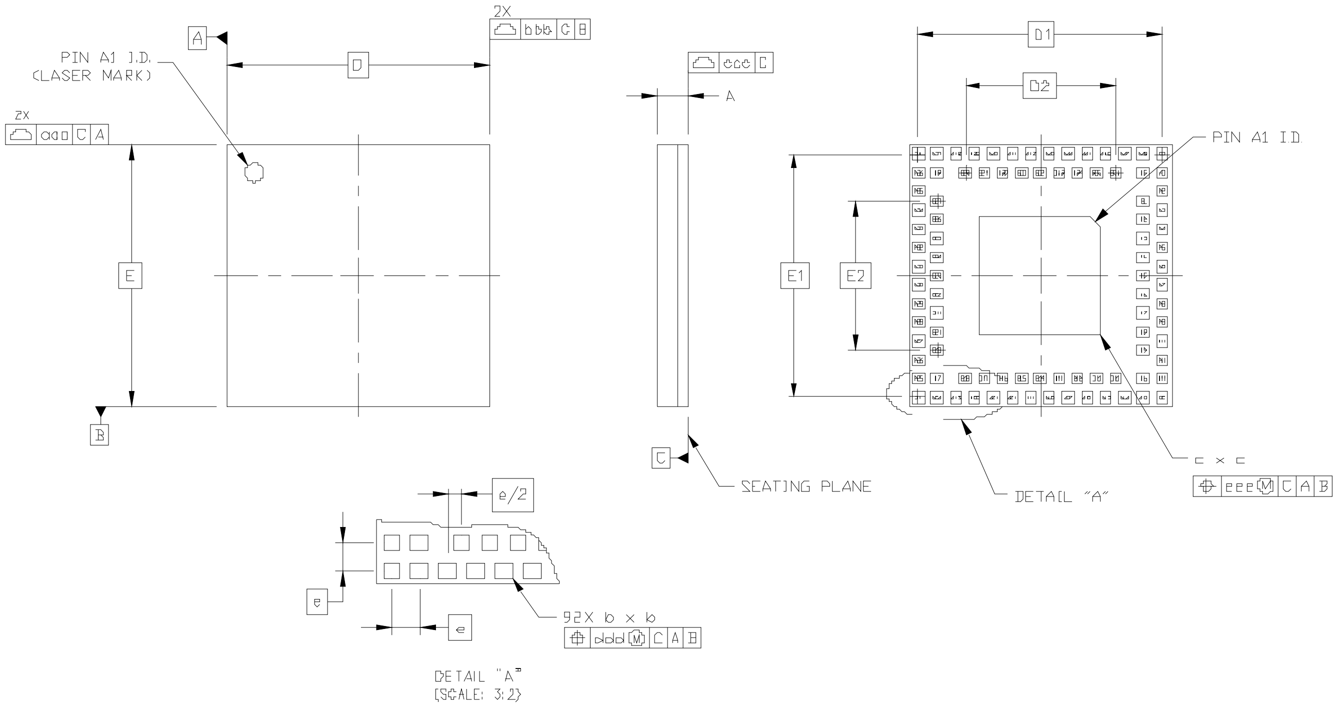


Figure 6.6. LGA-92 Package Drawing

Table 6.4. LGA-92 Package Dimensions

Dimension	Min	Nominal	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
c	3.15	3.20	3.25
D	7.00 BSC		
D1	6.50 BSC		
D2	4.00 BSC		
e	0.50 BSC		
E	7.00 BSC		
E1	6.50 BSC		
E2	4.00 BSC		
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

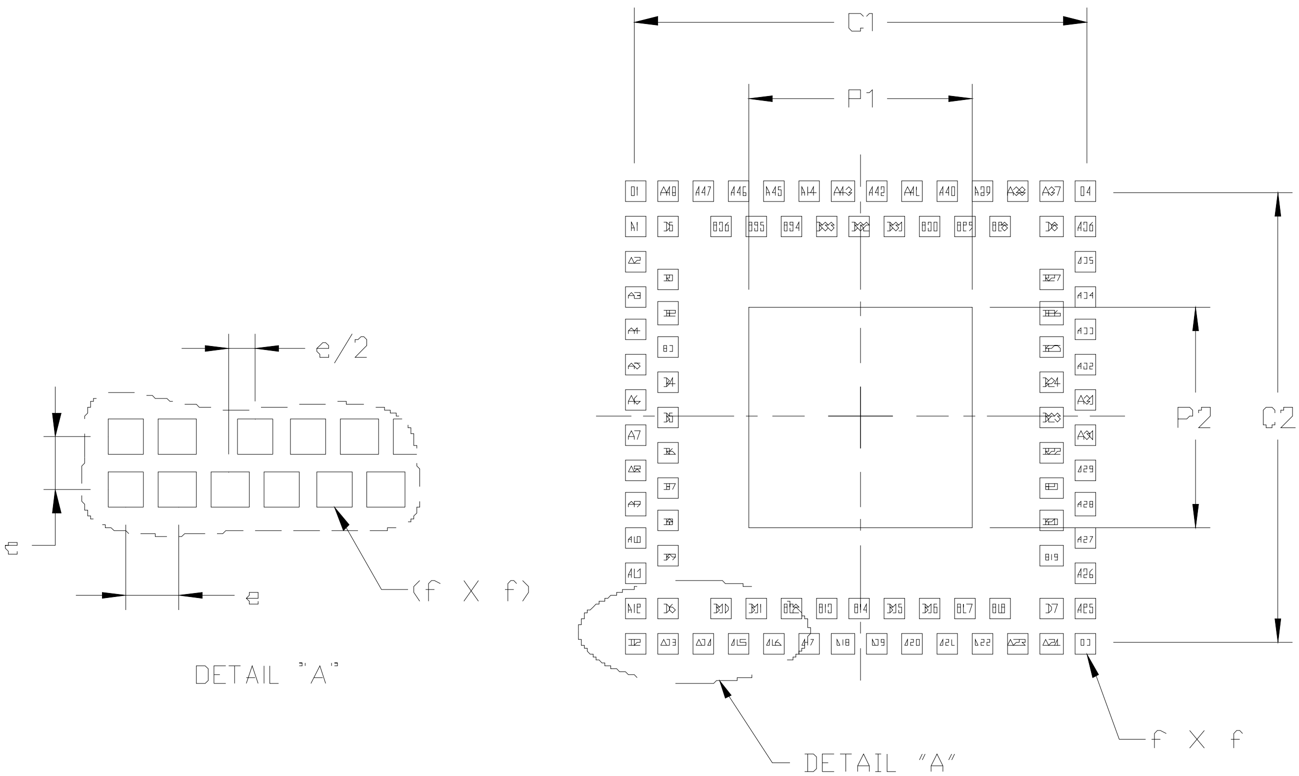


Figure 6.7. LGA-92 Landing Diagram

Table 6.5. LGA-92 Landing Diagram Dimensions

Dimension	Typical	Max
C1	6.50	—
C2	6.50	—
e	0.50	—
f	—	0.35
P1	—	3.20
P2	—	3.20

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
3. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
4. This land pattern design is based on the IPC-7351 guidelines.

6.6.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

6.6.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.7. TQFP-64 Package Specifications

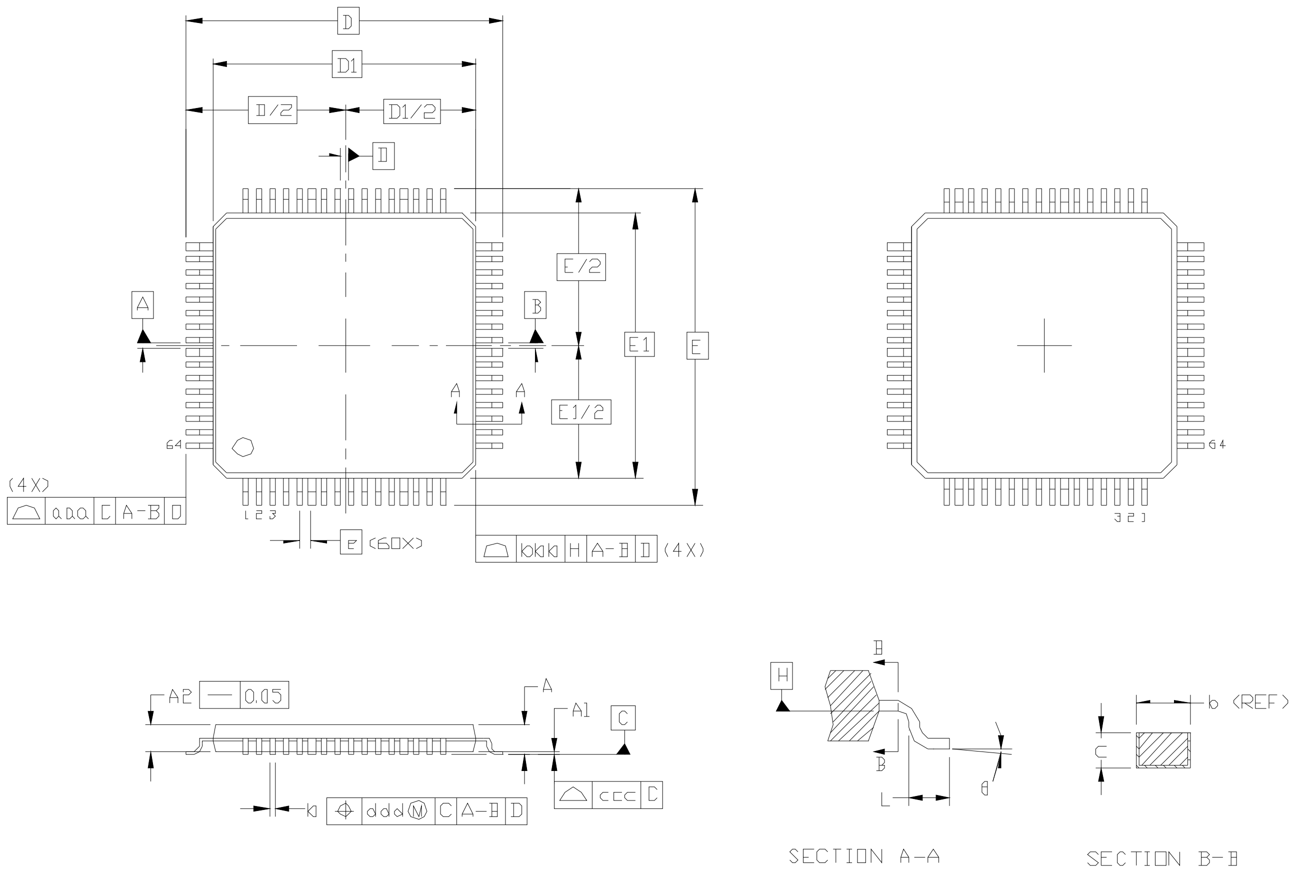


Figure 6.12. TQFP-64 Package Drawing

Table 6.10. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°

6.8.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.8.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

6.8.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.