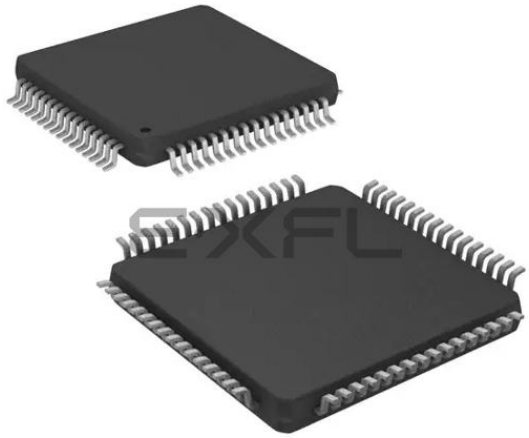

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c156-b-gqr

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Current on VDD						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time	t_{PM3FW}		—	425	—	µs
Power Mode 9 Wake Time	t_{PM9}		—	12	—	µs

Table 3.7. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
V_{DD} Voltage During Programming	V_{PROG}		1.8	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During a sequential write operation, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 3.8. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency*	$f_{PLL0OSC}$	Full Temperature and Supply Range	77	79	80	MHz
Power Supply Sensitivity*	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 79 MHz	—	430	—	ppm/V
Temperature Sensitivity*	$TS_{PLL0OSC}$	V_{DD} = 3.3 V, Fout = 79 MHz	—	95	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	80	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 80 MHz, M=24, N=99, LOCKTH = 0	—	1.7	—	µs
		f_{REF} = 32 kHz, $f_{PLL0OSC}$ = 80 MHz, M=0, N=2440, LOCKTH = 0	—	91	—	µs

***Note:** PLL0OSC in free-running oscillator mode.

Table 3.16. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.4	—	mV
		CMPHYP = 01	—	4	—	mV
		CMPHYP = 10	—	8	—	mV
		CMPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.4	—	mV
		CMPHYN = 01	—	–4	—	mV
		CMPHYN = 10	—	–8	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}	PB2 Pins	—	7.5	—	pF
		PB3 Pins	—	10.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}		–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

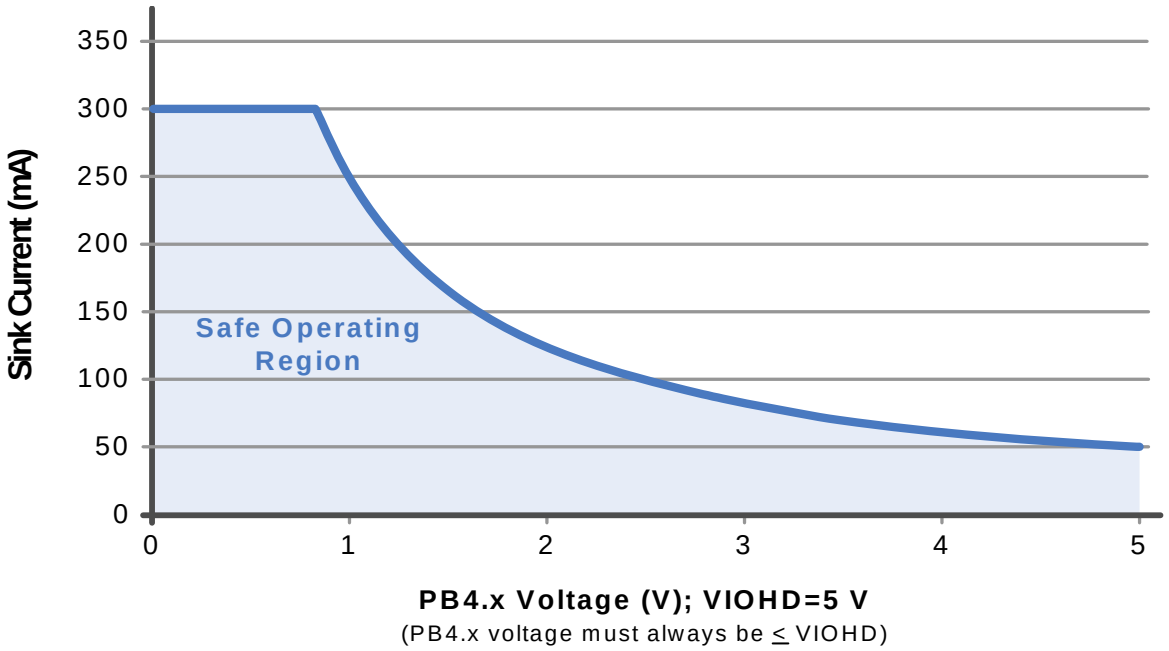


Figure 3.1. Maximum Sink Current vs. PB4.x Pin Voltage

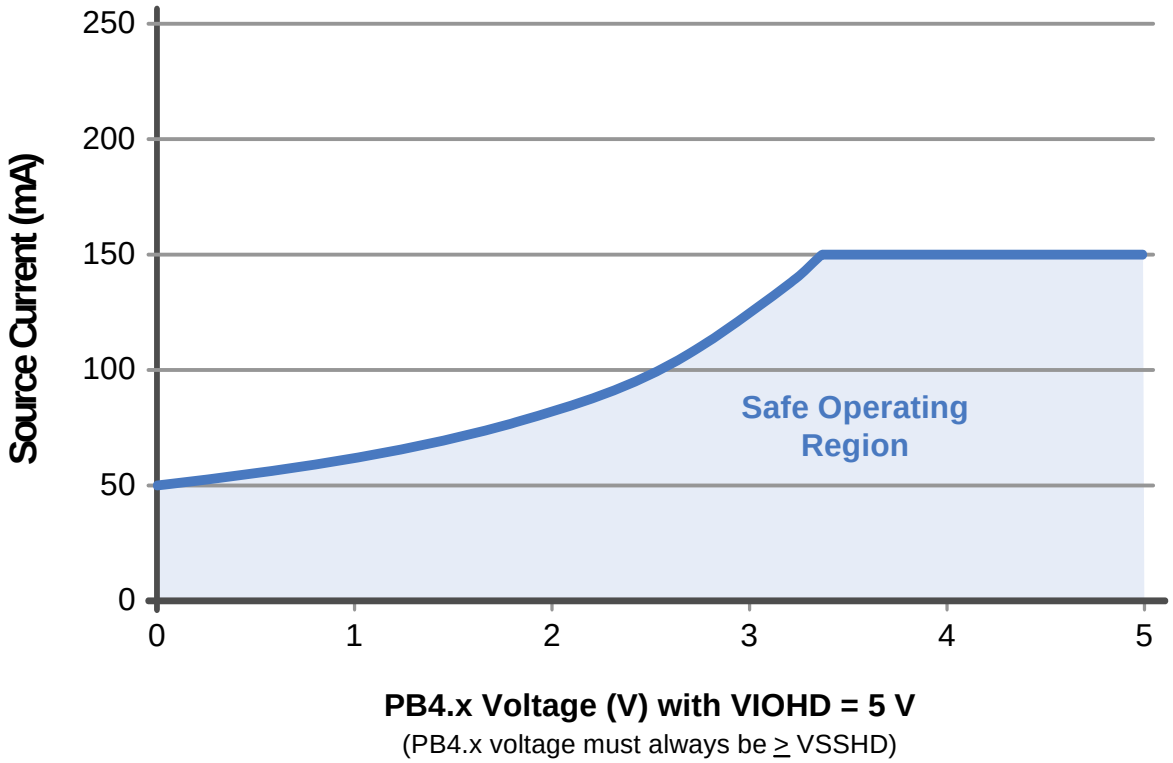


Figure 3.2. Maximum Source Current vs. PB4.x Pin Voltage

3.2. Thermal Conditions

Table 3.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	LGA-92 Packages	—	35	—	°C/W
		TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

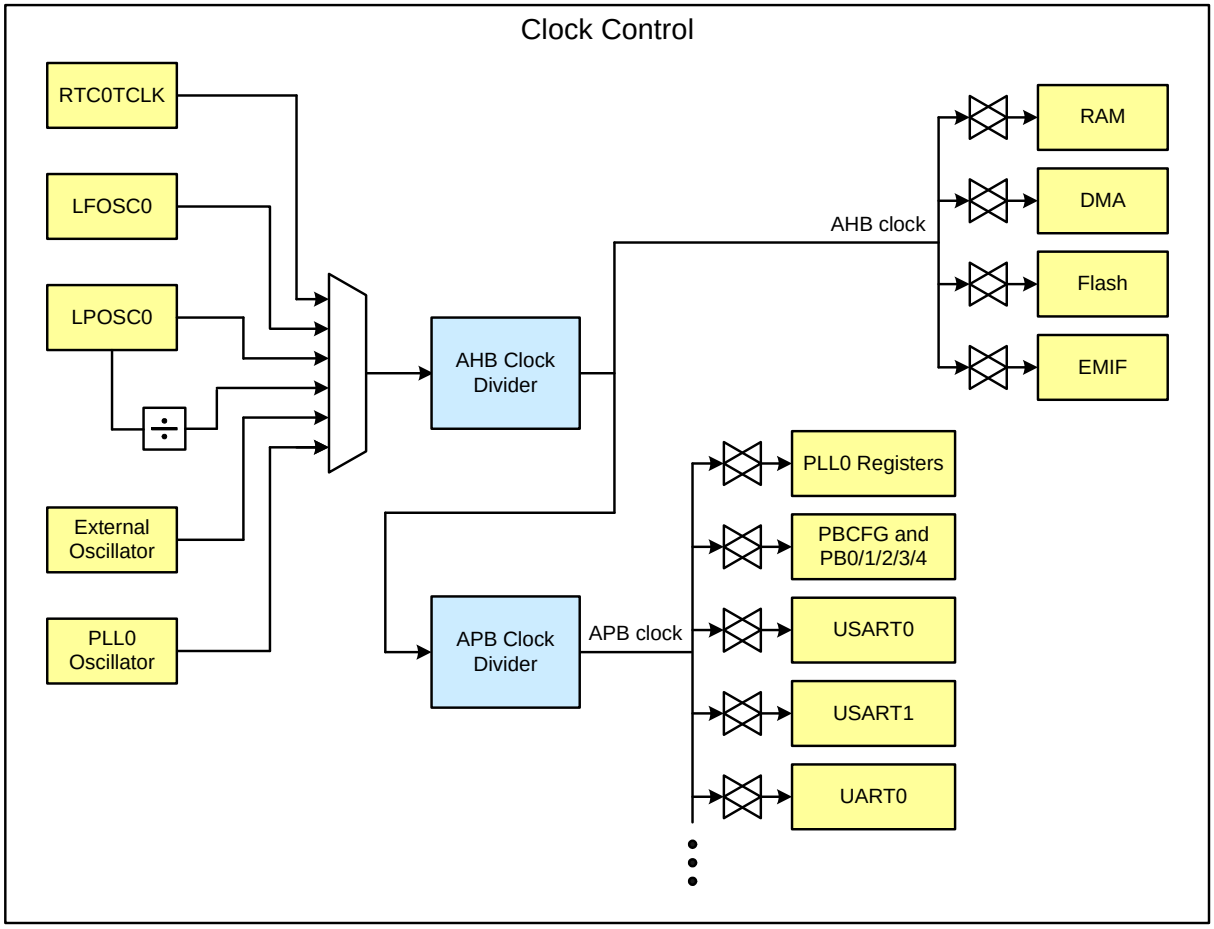
Table 3.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		V_{SS}–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	V_{SS}–0.3	6.0	V
		EXTVREG0 Used	V_{SS}–0.3	3.6	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIOHD	V_{IOHD}		V_{SS}–0.3	6.5	V
Voltage on I/O pins, non Port Bank 3 I/O	V_{IN}	$\overline{\text{RESET}}$, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$\overline{\text{RESET}}$, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		Port Bank 0, 1, and 2 I/O	V_{SS}–0.3	V_{IO}+0.3	V
		Port Bank 4 I/O	V_{SSHD}–0.3	V_{IOHD}+0.3	V
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.



4.5. Counters/Timers and PWM

4.5.1. Programmable Counter Array (EPCA0, PCA0, PCA1)

The SiM3C1xx devices include two types of PCA module: Enhanced and Standard.

The Enhanced Programmable Counter Array (EPCA0) and Standard Programmable Counter Array (PCA0, PCA1) modules are timer/counter systems allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

The Enhanced PCA module is multi-purpose, but is optimized for motor control applications. The EPCA module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never both active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers and outputs.
- Pulse-Width Modulation (PWM) waveform generation.
- High-speed square wave generation.
- Input capture mode.
- DMA capability for both input capture and waveform generation.
- PWM generation halt input.

The Standard PCA module (PCA) includes the following features:

- Two independent channels.
- Center- and edge-aligned waveform generation.
- Programmable clock divisor and multiple options for clock source selection.
- Pulse-Width Modulation waveform generation.

4.5.2. 32-bit Timer (TIMER0, TIMER1)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.
- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

4.5.3. Real-Time Clock (RTC0)

The RTC0 module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC0 provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3C1xx devices.

The RTC0 module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC0 output can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal low frequency oscillator (LFOSC0), an external 32.768 kHz crystal (no additional resistors or capacitors necessary), or with an external CMOS clock.
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- Operates directly from VDD and remains operational even when the device goes into its lowest power down mode.
- The RTC timer clock (RTC0TCLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.

4.5.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER0) module runs from the clock selected by the RTC0 module, allowing the LPTIMER0 to operate even if the AHB and APB clocks are disabled. The LPTIMER0 counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on a low-frequency clock (RTC0TCLK)
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection, which can generate an interrupt, reset the timer, or wake some devices from low power modes.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.

4.5.5. Watchdog Timer (WDTIMER0)

The WDTIMER0 module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

- Spike suppression up to 2 times the APB period.

4.6.6. I²S (I2S0)

The I²S module receives digital data from an external source over a data line in the standard I²S, left-justified, right-justified, or time domain multiplexing format, de-serializes the data, and generates requests to transfer the data using the DMA. The module also reads stereo audio samples from the DMA, serializes the data, and sends it out of the chip on a data line in the same standard serial format for digital audio. The I²S receive interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync), and SD (data input). The block's transmit interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync) and SD (data output).

The I²S module includes the following features:

- Master or slave capability.
- Flexible 10-bit clock divider with 8-bit fractional clock divider provides support for various common sampling frequencies (16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz) for up to two 32-bit channels.
- Support for DMA data transfers.
- Support for various data formats.
- Time Division Multiplexing

6. Pin Definitions and Packaging Information

6.1. SiM3C1x7 Pin Definitions

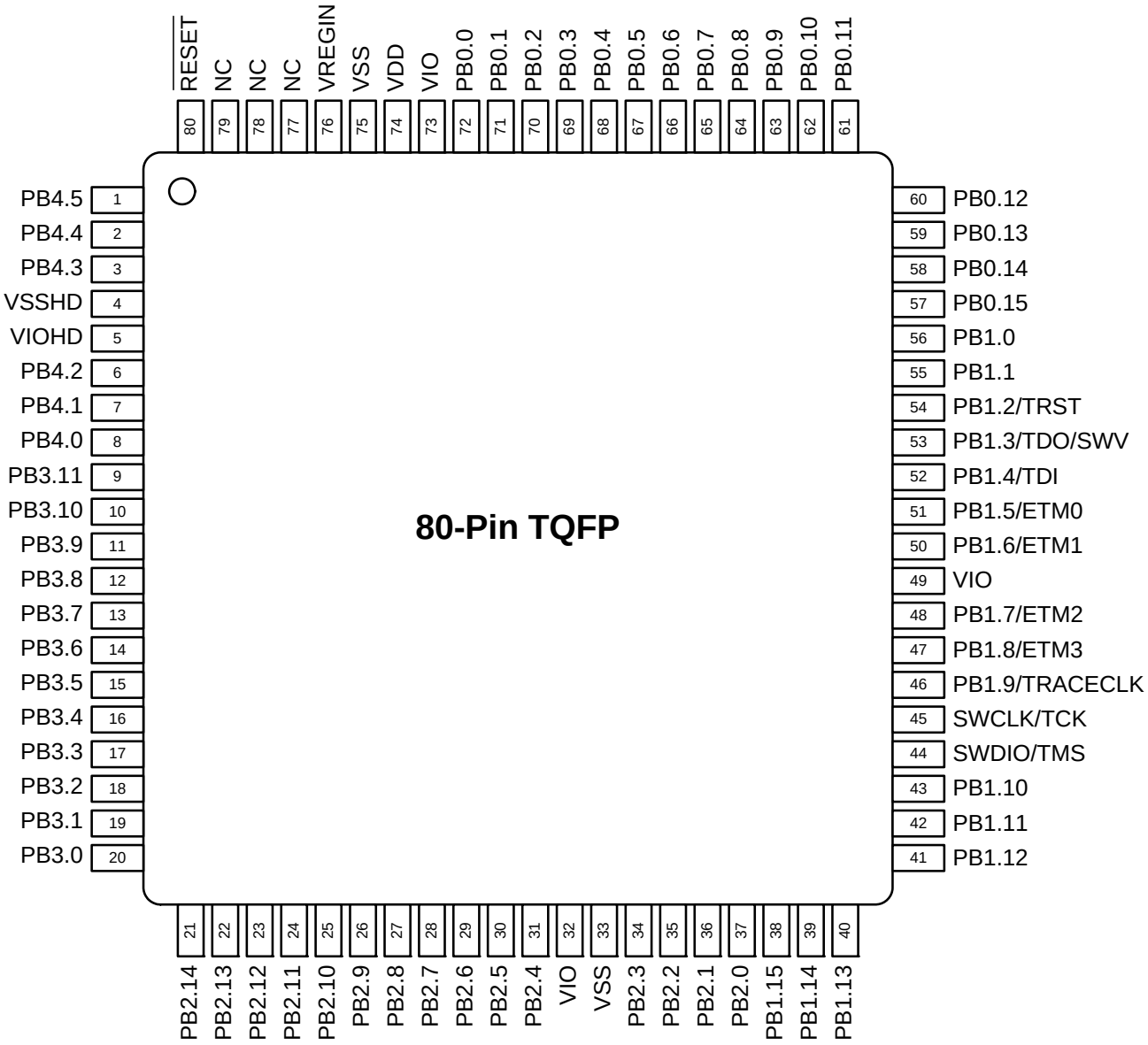


Figure 6.1. SiM3C1x7-GQ Pinout

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB2.6	Standard I/O	29	B13	XBR1	✓	AD11m/ A3		Yes	INT0.6 INT1.6	
PB2.7	Standard I/O	28	A17	XBR1	✓	AD10m/ A2		Yes	INT0.7 INT1.7	
PB2.8	Standard I/O	27	B12	XBR1	✓	AD9m/ A1		Yes		
PB2.9	Standard I/O	26	A16	XBR1	✓	AD8m/ A0		Yes		
PB2.10	Standard I/O	25	B11	XBR1	✓	AD7m/ D7		Yes		
PB2.11	Standard I/O	24	A15	XBR1	✓	AD6m/ D6		Yes		CMP0P.0 CMP1P.0
PB2.12	Standard I/O	23	A14	XBR1	✓	AD5m/ D5		Yes		CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.13	Standard I/O	22	A13	XBR1	✓	AD4m/ D4		Yes		CMP0P.1 CMP1P.1
PB2.14	Standard I/O	21	D2	XBR1	✓	AD3m/ D3		Yes		CMP0N.1 CMP1N.1
PB3.0	5 V Tolerant I/O	20	A12	XBR1	✓	AD2m/ D2				CMP0P.2 CMP1P.2
PB3.1	5 V Tolerant I/O	19	A11	XBR1	✓	AD1m/ D1				CMP0N.2 CMP1N.2
PB3.2	5 V Tolerant I/O	18	A10	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0	CMP0P.3 CMP1P.3
PB3.3	5 V Tolerant I/O	17	B8	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.8 INT1.8	CMP0N.3 CMP1N.3

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB4.0	High Drive I/O	8	A6				LSO0			
PB4.1	High Drive I/O	7	A5				LSO1			
PB4.2	High Drive I/O	6	A4				LSO2			
PB4.3	High Drive I/O	3	A2				LSO3			
PB4.4	High Drive I/O	2	A1				LSO4			
PB4.5	High Drive I/O	1	D1				LSO5			

Note: All unnamed pins on the LGA-92 package are no-connect pins. They should be soldered to the PCB for mechanical stability, but have no internal connections to the device.

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	25 59							
VDD	Power (Core)	58							
VIO	Power (I/O)	24 39							
VREGIN	Power (Regulator)	60							
VSSHD	Ground (High Drive)	2							
VIOHD	Power (High Drive)	3							
$\overline{\text{RESET}}$	Active-low Reset	64							
SWCLK/TCK	Serial Wire / JTAG	36							
SWDIO/TMS	Serial Wire / JTAG	35							
PB0.0	Standard I/O	57	XBR0	✓					ADC0.2 CS0.1
PB0.1	Standard I/O	56	XBR0	✓					ADC0.3 CS0.2
PB0.2	Standard I/O	55	XBR0	✓					ADC0.4 CS0.3
PB0.3	Standard I/O	54	XBR0	✓					ADC0.5 CS0.4
PB0.4	Standard I/O	53	XBR0	✓					ADC0.6 CS0.5 IVC0.0
PB0.5	Standard I/O	52	XBR0	✓					ADC0.7 CS0.6 IVC0.1
PB0.6	Standard I/O	51	XBR0	✓					ADC0.8 CS0.7 RTC1

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.2	5 V Tolerant I/O	14	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0 WAKE.8	CMP0P.2 CMP1P.2
PB3.3	5 V Tolerant I/O	13	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.4 INT1.4 WAKE.9	CMP0N.2 CMP1N.2
PB3.4	5 V Tolerant I/O	12	XBR1	✓	$\overline{OE}$			INT0.5 INT1.5 WAKE.10	CMP0P.3 CMP1P.3
PB3.5	5 V Tolerant I/O	11	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.6 INT1.6 WAKE.11	CMP0N.3 CMP1N.3
PB3.6	5 V Tolerant I/O	10	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.7 INT1.7 WAKE.12	CMP0P.4 CMP1P.4 EXREGSP
PB3.7	5 V Tolerant I/O	9	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 INT0.8 INT1.8 WAKE.13	CMP0N.4 CMP1N.4 EXREGSN
PB3.8	5 V Tolerant I/O	8	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T1 INT0.9 INT1.9 WAKE.14	CMP0P.5 CMP1P.5 EXREGOUT

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.1	5 V Tolerant I/O	9	XBR1	✓		DAC0T1 DAC1T1 LPT0T1 INT0.1 INT1.1 WAKE.13	CMP0N.1 CMP1N.1 EXREGSN
PB3.2	5 V Tolerant I/O	8	XBR1	✓		DAC0T2 DAC1T2 LPT0T2 INT0.2 INT1.3 WAKE.14	CMP0P.2 CMP1P.2 EXREGOUT
PB3.3	5 V Tolerant I/O	7	XBR1	✓		DAC0T3 DAC1T3 INT0.3 INT1.3 WAKE.15	CMP0N.2 CMP1N.2 EXREGBD
PB4.0	High Drive I/O	6					
PB4.1	High Drive I/O	5					
PB4.2	High Drive I/O	4					
PB4.3	High Drive I/O	1					

6.5. TQFP-80 Package Specifications

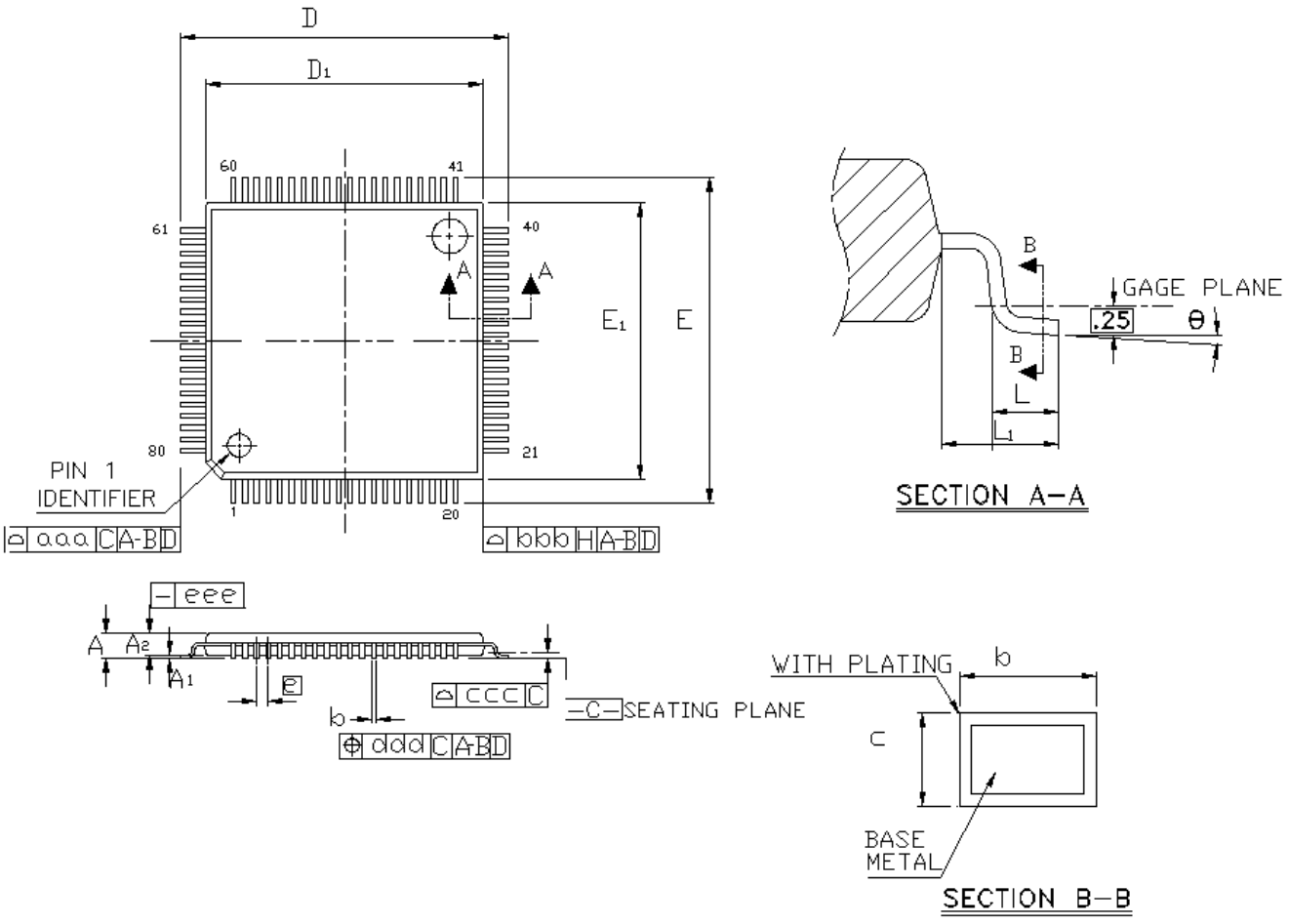


Figure 6.8. TQFP-80 Package Drawing

Table 6.6. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		

Table 6.10. TQFP-64 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

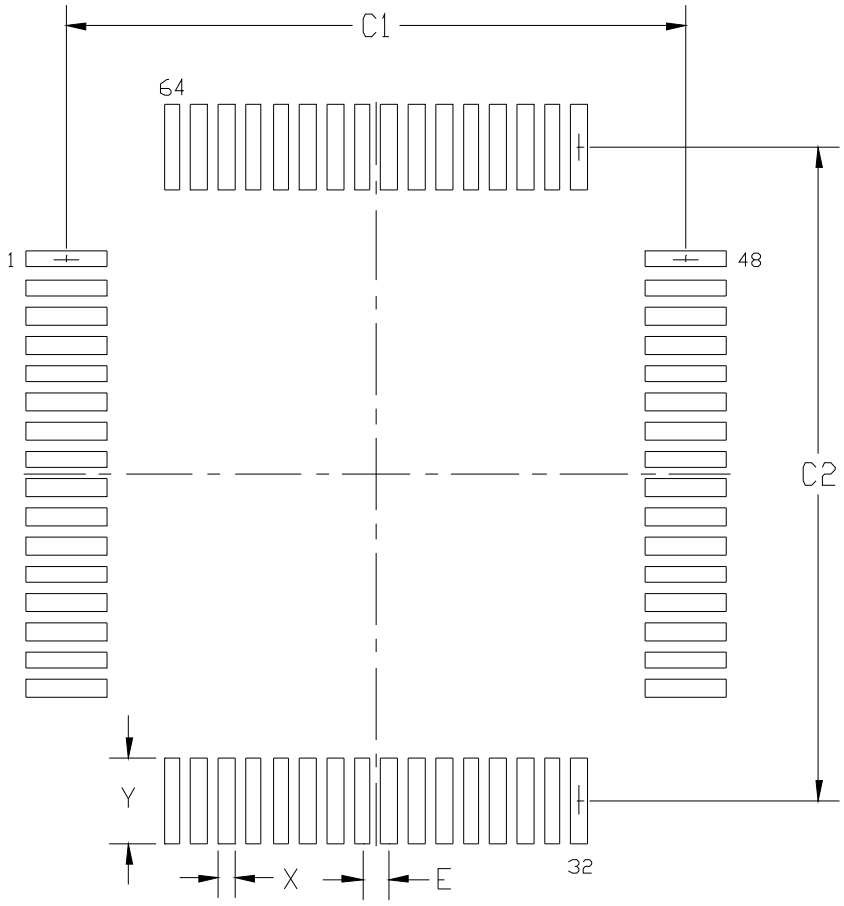


Figure 6.13. TQFP-64 Landing Diagram

Table 6.11. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.8.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.8.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

6.8.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

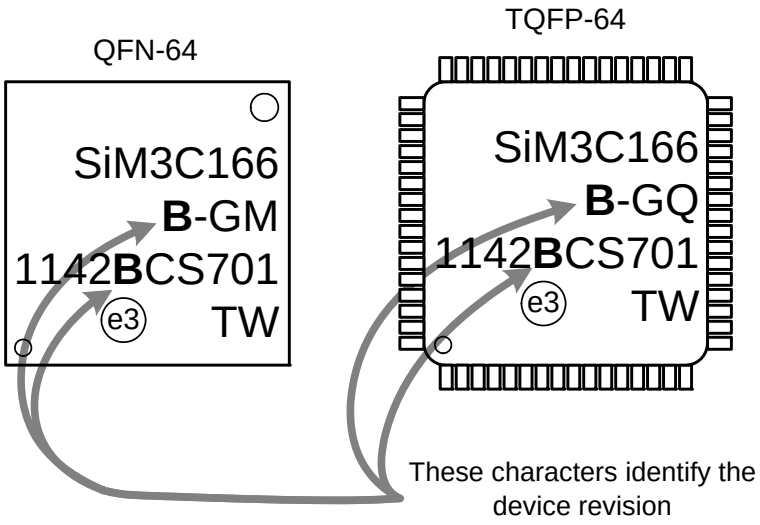


Figure 7.3. SiM3C1x6 Revision Information

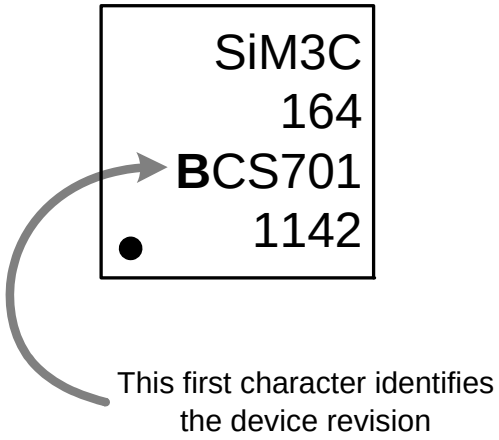


Figure 7.4. SiM3C1x4 Revision Information

7.2. Comparator Rising/Falling Edge Flags in Debug Mode (CMP0, CMP1)

7.2.1. Problem

On Revision A and Revision B devices, if the comparator output is high, the comparator rising and falling edge flags will both be set to 1 upon single-step or exit from debug mode.

7.2.2. Impacts

Firmware using the rising and falling edge flags to make decisions may see a false trigger of the comparator if the output of the comparator is high during a debug session. This does not impact the non-debug operation of the device.

7.2.3. Workaround

There is not a system-agnostic workaround for this issue.

7.2.4. Resolution

This issue exists on Revision A and Revision B devices. It may be corrected in a future device revision.