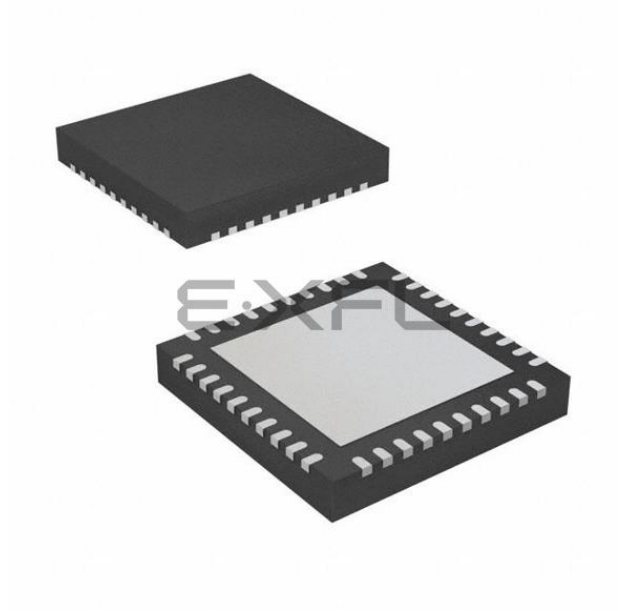

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c164-b-gm

1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3C1xx device family.

1.1.1. SiM3U1xx/SiM3C1xx Reference Manual

The Silicon Laboratories SiM3U1xx/SiM3C1xx Reference Manual provides detailed functional descriptions for the SiM3C1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3C1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vector Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm.m3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

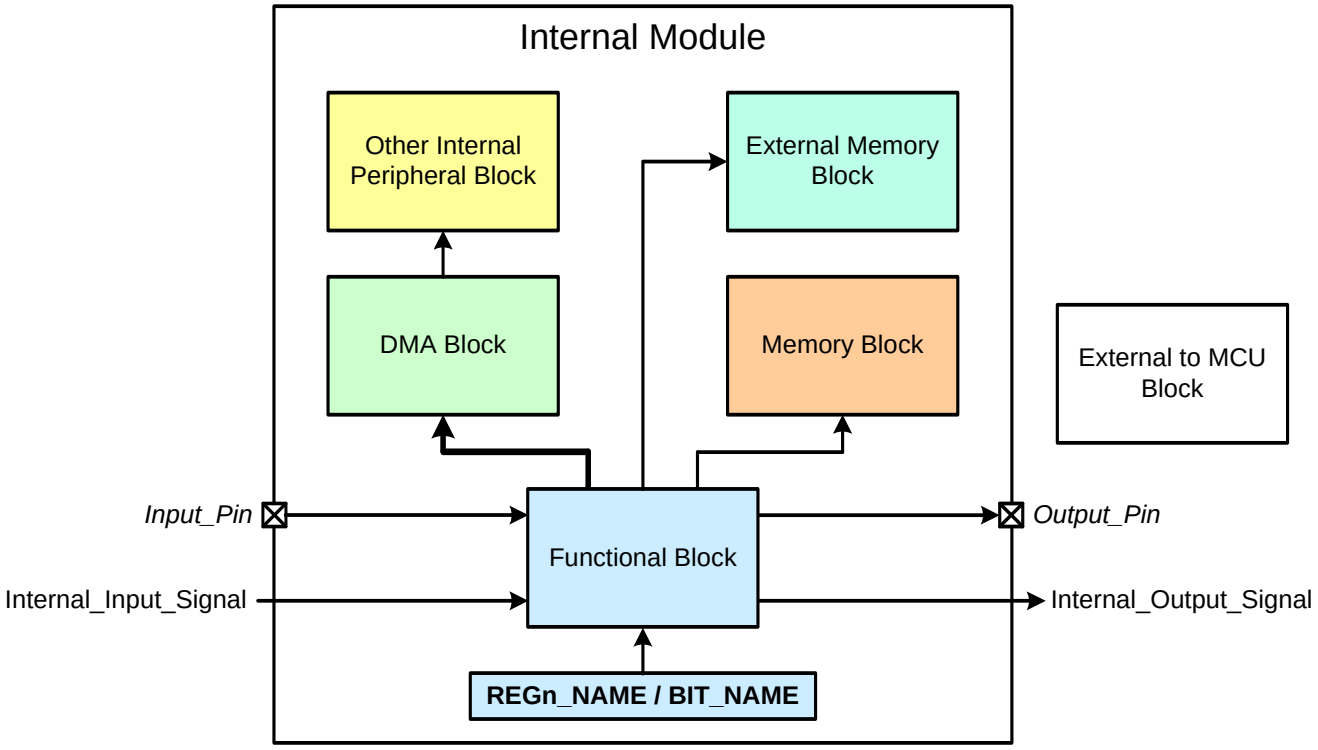


Figure 1.1. Block Diagram Conventions

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Oscillator (EXTOSC0)[8]	I_{EXTOSC}	FREQCN = 111	—	3.8	4.7	mA
		FREQCN = 110	—	840	950	µA
		FREQCN = 101	—	185	220	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	15	µA
		FREQCN = 001	—	5	10	µA
		FREQCN = 000	—	3	8	µA
SARADC0, SARADC1	I_{SARADC}	Sampling at 1 Msps, highest power mode settings.	—	1.2	1.5	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	510	µA
Temperature Sensor	I_{TSENSE}		—	75	105	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	750	µA
		Low Power Mode	—	160	190	µA
VREF0	I_{REFP}		—	75	100	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	—	µA
		CMPMD = 10	—	3	—	µA
		CMPMD = 01	—	10	—	µA
		CMPMD = 00	—	25	—	µA
Capacitive Sensing (CAPSENSE0)	I_{CS}	Continuous Conversions	—	55	80	µA
IDAC0[7], IDAC1[7]	I_{IDAC}		—	75	90	µA
IVC0[7]	I_{IVC}	I_{IN} = 0	—	1.5	2.5	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	25	µA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Current on VDD						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time	t_{PM3FW}		—	425	—	µs
Power Mode 9 Wake Time	t_{PM9}		—	12	—	µs

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Regulator Characteristics (VREG0, Supplied from VREGIN Pin)						
Output Voltage (at VDD pin)	V_{DDOUT}	$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = 0	3.15	3.3	3.4	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = 1	3.15	3.3	3.4	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X I_{DDOUT} = 500 µA	2.3	2.8	3.6	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X I_{DDOUT} = 5 mA	2.1	2.65	3.3	V
Output Current (at VDD pin)*	I_{DDOUT}	$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = X	—	—	150	mA
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X	—	—	5	mA
Output Load Regulation	V_{DDLR}	BGDIS = 0	—	0.1	1	mV/mA
Output Capacitance	C_{VDD}		1	—	10	µF

***Note:** Total current VREG0 is capable of providing. Any current consumed by the SiM3C1xx reduces the current available to external devices powered from VDD.

Table 3.6. External Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range (at VREGIN)	V_{REGIN}		3.0	—	3.6	V
Output Voltage (at EXREGOUT)	$V_{EXREGOUT}$	Programmable in 100 mV steps	1.8	—	3.6	V
NPN Current Drive	I_{NPN}	400 mV Dropout	12	—	—	mA
PNP Current Drive	I_{PNP}	$V_{EXREGBD} > V_{REGIN}$- 1.5 V	–6	—	—	mA
EXREGBD Voltage (PNP Mode)	$V_{EXREGBD}$	V_{REGIN} >= 3.5 V	V_{REGIN} – 2.0	—	—	V
		V_{REGIN} < 3.5 V	1.5	—	—	V
Standalone Mode Output Current	$I_{EXTREGBD}$	400 mV Dropout	—	—	11.5	mA
External Capacitance with External BJT	C_{BJT}		4.7	—	—	µF
Standalone Mode Load Regulation	$LR_{STAND-ALONE}$		—	1	—	mV/mA
Standalone Mode External Capacitance	$C_{STAND-ALONE}$		47	—	—	nF
Current Limit Range	I_{LIMIT}	1 Ω Sense Resistor	10	—	720	mA
Current Limit Accuracy			—	—	10	%
Foldback Limit Accuracy			—	—	20	%
Current Sense Resistor	R_{SENSE}		—	—	1	Ω
Internal Pull-Down	R_{PD}		—	5	—	kΩ
Internal Pull-Up	R_{PU}		—	10	—	kΩ
Current Sensor						
Sensing Pin Voltage	$V_{EXTREGSP}$ $V_{EXTREGSN}$	Measured at EXTREGSP or EXTREGSN pin	2.2	—	V_{REGIN}	V
Differential Sensing Voltage	V_{DIFF}	($V_{EXTREGSP}$ – $V_{EXTREGSN}$)	10	—	1600	mV
Current at EXTREGSN Pin	$I_{EXTREGSN}$		—	8	—	µA
Current at EXTREGSP Pin	$I_{EXTREGSP}$		—	V_{DIFF} x 200 + 12	—	µA

Table 3.11. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{DD} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range	2.0	2.046	2.10	mA
		1 mA Range	0.99	1.023	1.05	mA
		0.5 mA Range	493	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VDD Power Supply Rejection Ratio		2 mA Range	—	-220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

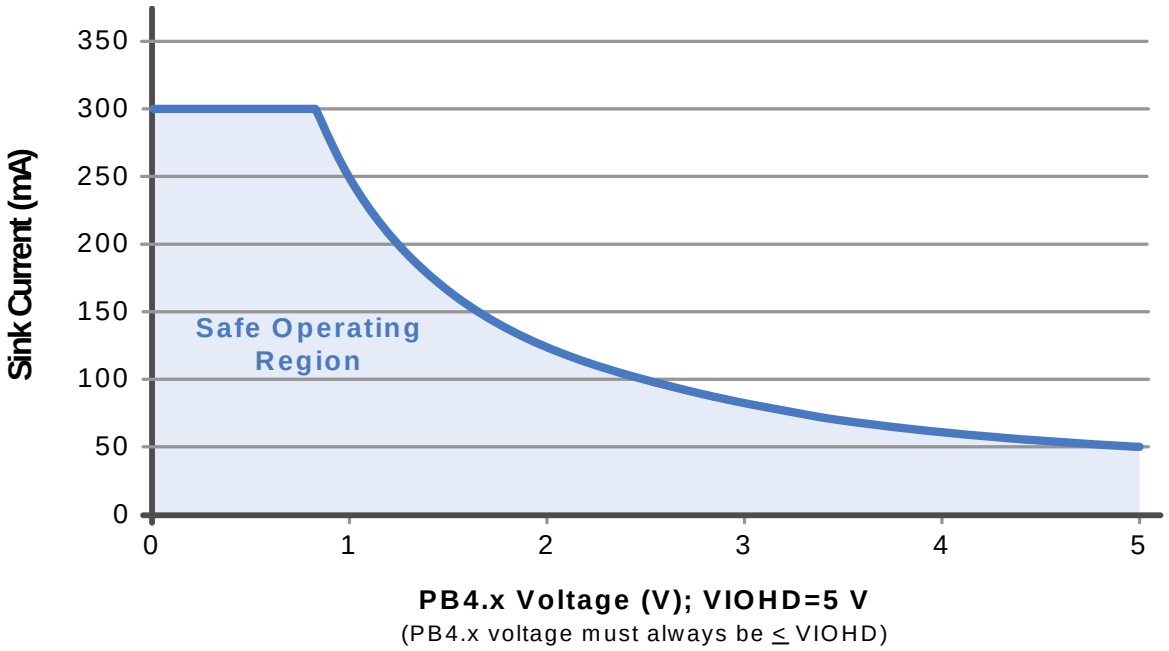


Figure 3.1. Maximum Sink Current vs. PB4.x Pin Voltage

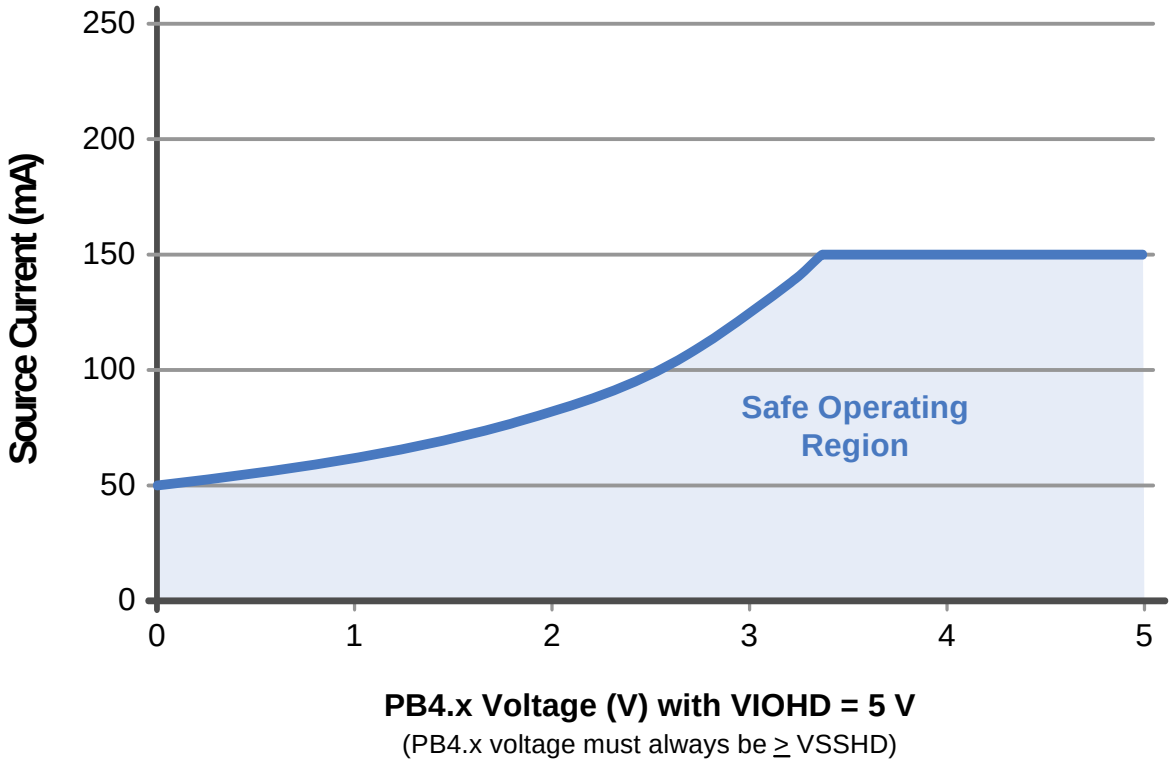
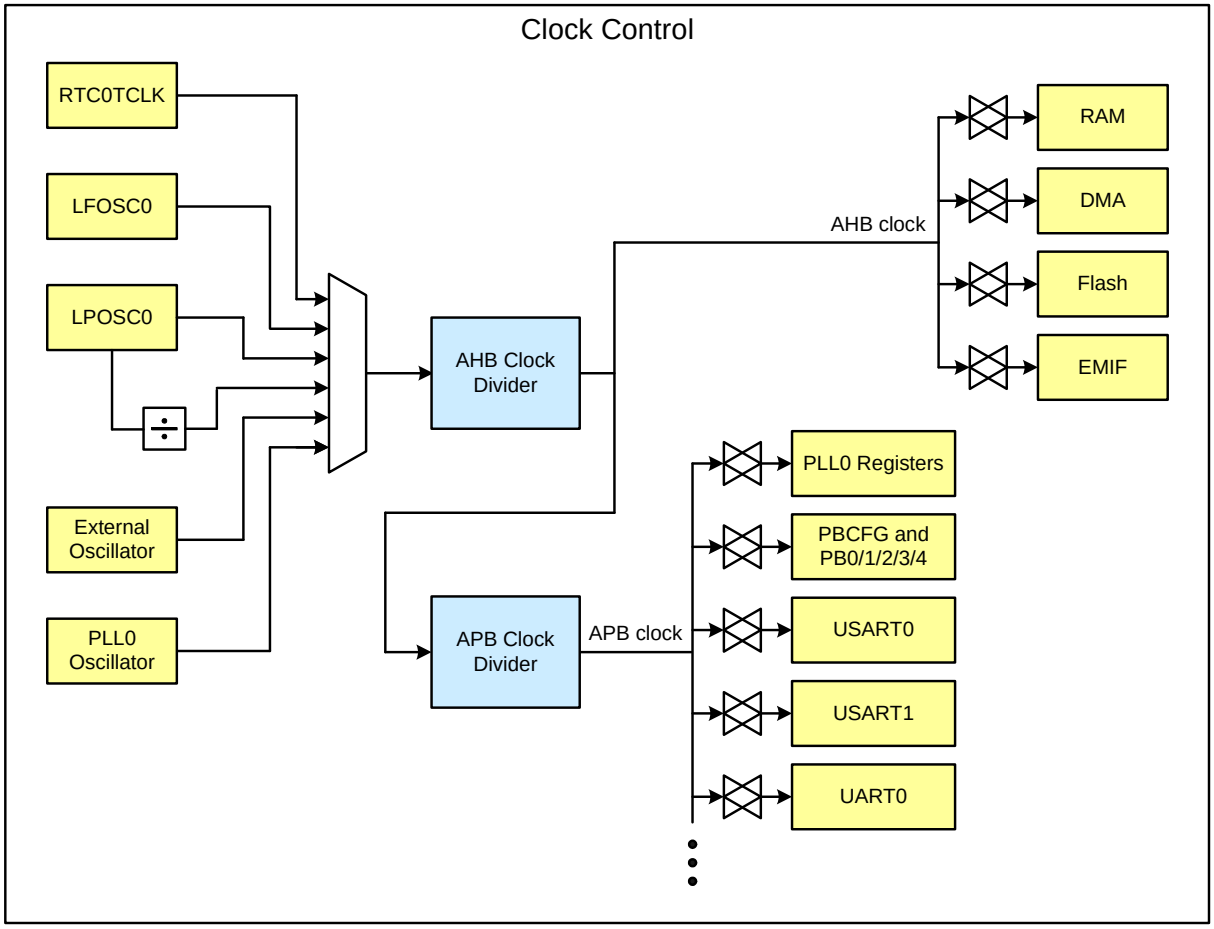


Figure 3.2. Maximum Source Current vs. PB4.x Pin Voltage

4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.



4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Five output ranges with output frequencies ranging from 23 to 80 MHz.
- Multiple reference frequency inputs.
- Three output modes: free-running DCO, frequency-locked, and phase-locked.
- Ability to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.
- Ability to suspend all output frequency updates (including dithering and spectrum spreading) using the STALL bit during jitter-sensitive operations.

4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3C1xx devices and enables or disables automatically, as needed.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC0) provides a low power internal clock source running at approximately 16.4 kHz for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator

4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, RC, C, or CMOS oscillators.
- Support external CMOS frequencies from 10 kHz to 50 MHz and external crystal frequencies from 10 kHz to 30 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

4.6. Communications Peripherals

4.6.1. External Memory Interface (EMIF0)

The External Memory Interface (EMIF0) allows external parallel asynchronous devices, like SRAMs and LCD controllers, to appear as part of the system memory map. The EMIF0 module includes the following features:

- Provides a memory mapped view of multiple external devices.
- Support for byte, half-word and word accesses regardless of external device data-width.
- Error indicator for certain invalid transfers.
- Minimum external timing allows for 3 clocks per write or 4 clocks per read.
- Output bus can be shared between non-muxed and muxed devices.
- Available extended address output allows for up to 24-bit address with 8-bit parallel devices.
- Support for 8-bit and 16-bit (muxed-mode only) devices with up to two chip-select signals.
- Support for internally muxed devices with dynamic address shifting.
- Fully programmable control signal waveforms.

4.6.2. USART (USART0, USART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device. In addition to these signals, the USART0 module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.6.3. UART (UART0, UART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device.

The UART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud-rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX) or 1 Mbaud Smartcard (TX or RX).

- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation.
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.

4.6.4. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI module includes the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Programmable FIFO threshold level to request data service for DMA transfers.
- Support for multiple masters on the same data lines.

4.6.5. I2C (I2C0, I2C1)

The I2C interface is a two-wire, bi-directional serial bus. The two clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.

5. Ordering Information

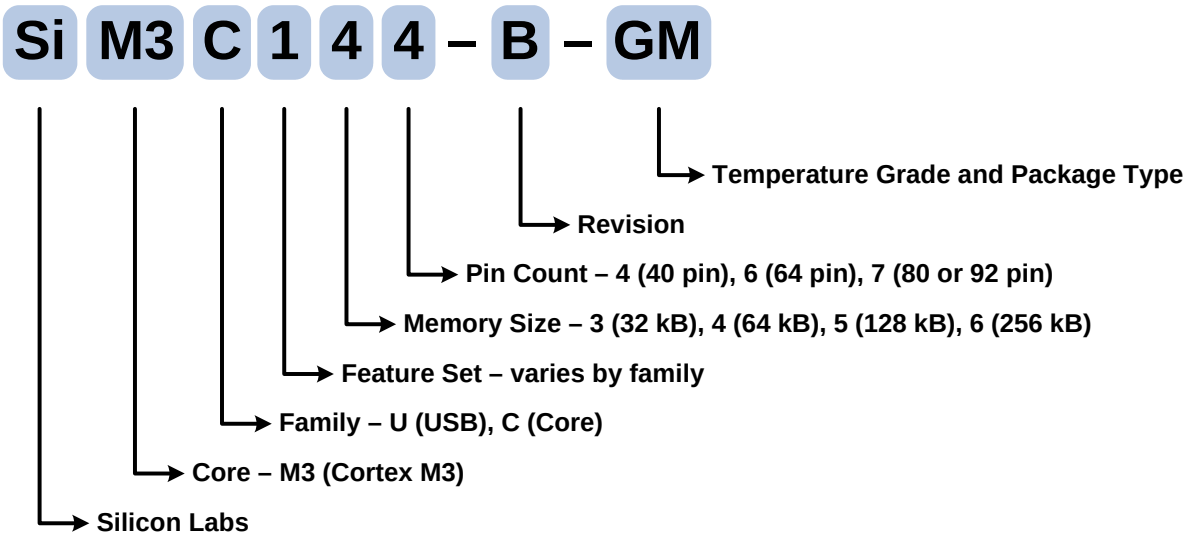


Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I^2S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB4.0	High Drive I/O	8	A6				LSO0			
PB4.1	High Drive I/O	7	A5				LSO1			
PB4.2	High Drive I/O	6	A4				LSO2			
PB4.3	High Drive I/O	3	A2				LSO3			
PB4.4	High Drive I/O	2	A1				LSO4			
PB4.5	High Drive I/O	1	D1				LSO5			

Note: All unnamed pins on the LGA-92 package are no-connect pins. They should be soldered to the PCB for mechanical stability, but have no internal connections to the device.

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.8	Standard I/O	30	XBR0	✓	AD14m/ A6			WAKE.2	ADC1.3 CS0.12
PB1.9	Standard I/O	29	XBR0	✓	AD13m/ A5			WAKE.3	ADC1.2 CS0.13
PB1.10	Standard I/O	28	XBR0	✓	AD12m/ A4			DMA0T1 WAKE.4	ADC1.1 CS0.14
PB1.11	Standard I/O	27	XBR0	✓	AD11m/ A3			DMA0T0 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.12	Standard I/O	26	XBR0	✓	AD10m/ A2			WAKE.6	
PB1.13	Standard I/O	23	XBR0	✓	AD9m/ A1				
PB1.14	Standard I/O	22	XBR0	✓	AD8m/ A0				
PB1.15	Standard I/O	21	XBR0	✓	AD7m/ D7				
PB2.0	Standard I/O	20	XBR1	✓	AD6m/ D6	LSI0	Yes	INT0.0 INT1.0	
PB2.1	Standard I/O	19	XBR1	✓	AD5m/ D5	LSI1	Yes	INT0.1 INT1.1	
PB2.2	Standard I/O	18	XBR1	✓	AD4m/ D4	LSI2	Yes	INT0.2 INT1.2	CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.3	Standard I/O	17	XBR1	✓	AD3m/ D3	LSI3	Yes	INT0.3 INT1.3	CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	16	XBR1	✓	AD2m/ D2				CMP0P.1 CMP1P.1
PB3.1	5 V Tolerant I/O	15	XBR1	✓	AD1m/ D1				CMP0N.1 CMP1N.1

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.1	5 V Tolerant I/O	9	XBR1	✓		DAC0T1 DAC1T1 LPT0T1 INT0.1 INT1.1 WAKE.13	CMP0N.1 CMP1N.1 EXREGSN
PB3.2	5 V Tolerant I/O	8	XBR1	✓		DAC0T2 DAC1T2 LPT0T2 INT0.2 INT1.3 WAKE.14	CMP0P.2 CMP1P.2 EXREGOUT
PB3.3	5 V Tolerant I/O	7	XBR1	✓		DAC0T3 DAC1T3 INT0.3 INT1.3 WAKE.15	CMP0N.2 CMP1N.2 EXREGBD
PB4.0	High Drive I/O	6					
PB4.1	High Drive I/O	5					
PB4.2	High Drive I/O	4					
PB4.3	High Drive I/O	1					

Table 6.6. TQFP-80 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
L	0.45	0.60	0.75
L1		1.00 Ref	
Θ	0°	3.5°	7°
aaa		0.20	
bbb		0.20	
ccc		0.08	
ddd		0.08	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.8. QFN-40 Package Specifications

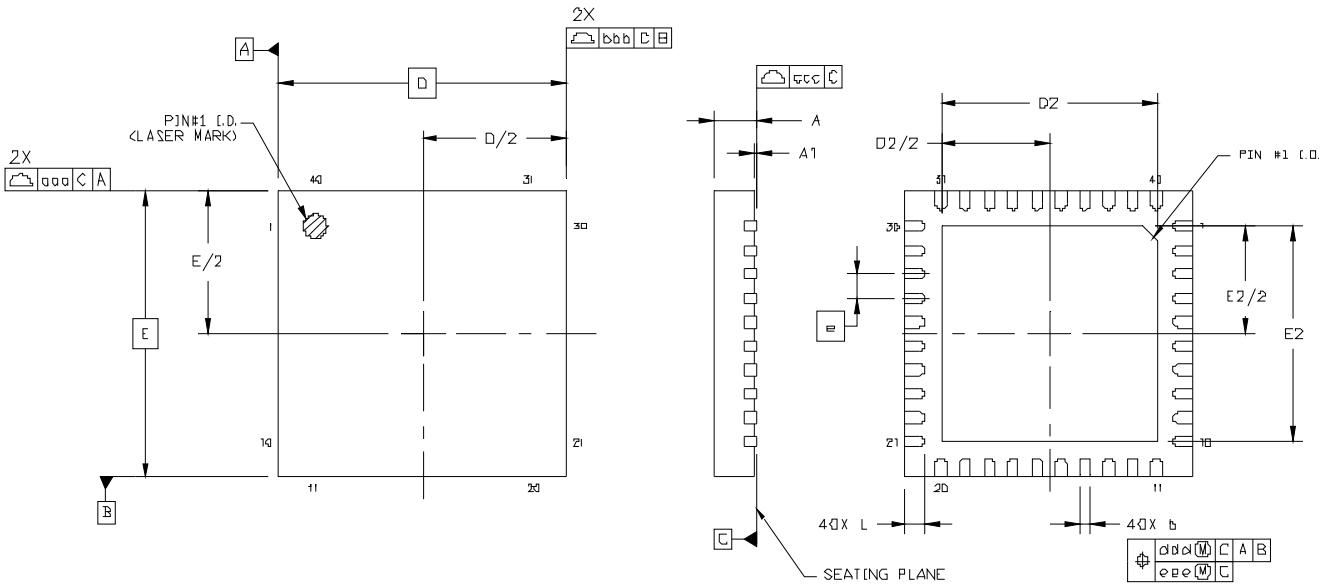


Figure 6.14. QFN-40 Package Drawing

Table 6.12. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

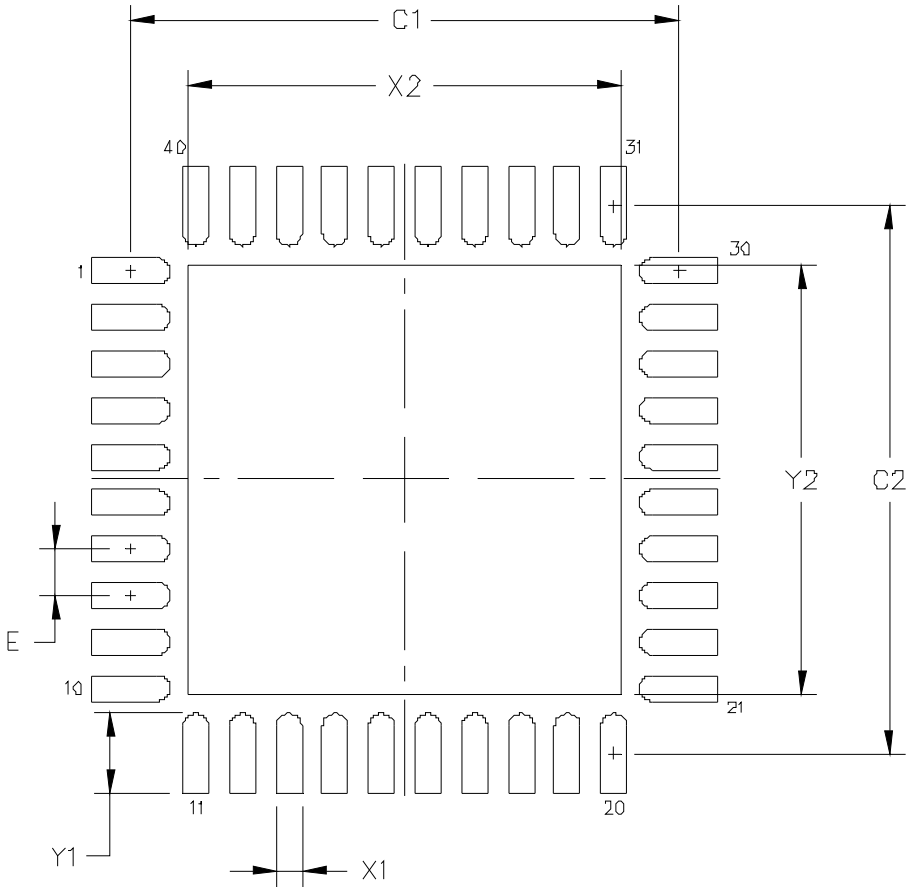


Figure 6.15. QFN-40 Landing Diagram

Table 6.13. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.