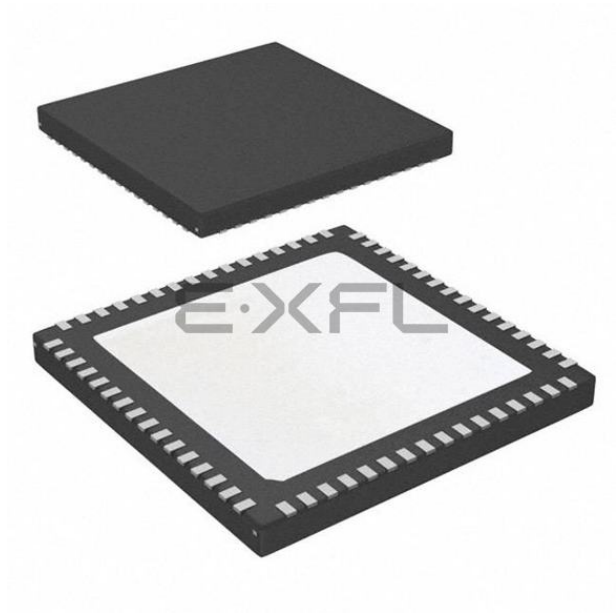

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 50 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 28x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/sim3c166-b-gmr |

# 3. Electrical Specifications

## 3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

**Table 3.1. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Supply Voltage on VDD | $V_{DD}$ | | 1.8 | — | 3.6 | V |
| Operating Supply Voltage on VREGIN | $V_{REGIN}$ | EXTVREG0 Not Used | 4 | — | 5.5 | V |
| | | EXTVREG0 Used | 3.0 | — | 3.6 | V |
| Operating Supply Voltage on VIO | $V_{IO}$ | | 1.8 | — | $V_{DD}$ | V |
| Operating Supply Voltage on VIOHD | $V_{IOHD}$ | HV Mode (default) | 2.7 | — | 6.0 | V |
| | | LV Mode | 1.8 | — | 3.6 | V |
| Voltage on I/O pins, Port Bank 0, 1 and 2 I/O | $V_{IN}$ | | $V_{SS}$ | — | $V_{IO}$ | V |
| Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$ | $V_{IN}$ | SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$ | $V_{SS}$ | — | $V_{IO}$+2.0 | V |
| | | SiM3C1x7 PB3.8 - PB3.11 | $V_{SS}$ | — | Lowest of $V_{IO}$+2.0 or $V_{REGIN}$ | V |
| | | SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$ | $V_{SS}$ | — | $V_{IO}$+2.0 | V |
| | | SiM3C1x6 PB3.6–PB3.9 | $V_{SS}$ | — | Lowest of $V_{IO}$+2.0 or $V_{REGIN}$ | V |
| | | SiM3C1x4 $\overline{\text{RESET}}$ | $V_{SS}$ | — | $V_{IO}$+2.0 | V |
| | | SiM3C1x4 PB3.0–PB3.3 | $V_{SS}$ | — | Lowest of $V_{IO}$+2.0 or $V_{REGIN}$ | V |
| Voltage on I/O pins, Port Bank 4 I/O | $V_{IN}$ | | $V_{SSHD}$ | — | $V_{IOHD}$ | V |
| System Clock Frequency (AHB) | $f_{AHB}$ | | 0 | — | 80 | MHz |
| Peripheral Clock Frequency (APB) | $f_{APB}$ | | 0 | — | 50 | MHz |
| Operating Ambient Temperature | $T_A$ | | –40 | — | 85 | °C |
| Operating Junction Temperature | $T_J$ | | –40 | — | 105 | °C |

**Note:** All voltages with respect to $V_{SS}$.

**Table 3.2. Power Consumption (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Analog Peripheral Supply Currents** | | | | | | |
| Voltage Regulator (VREG0) | $I_{VREGIN}$ | Normal Mode, $T_A$ = 25 °C<br>BGDIS = 0, SUSEN = 0 | — | 300 | — | µA |
| | | Normal Mode, $T_A$ = 85 °C<br>BGDIS = 0, SUSEN = 0 | — | — | 650 | µA |
| | | Suspend Mode, $T_A$ = 25 °C<br>BGDIS = 0, SUSEN = 1 | — | 75 | — | µA |
| | | Suspend Mode, $T_A$ = 85 °C<br>BGDIS = 0, SUSEN = 1 | — | — | 115 | µA |
| | | Sleep Mode, $T_A$ = 25 °C<br>BGDIS = 1, SUSEN = X | — | 90 | — | nA |
| | | Sleep Mode, $T_A$ = 85 °C<br>BGDIS = 1, SUSEN = X | — | — | 500 | nA |
| Voltage Regulator (VREG0) Sense | $I_{VRSENSE}$ | SENSEEN = 1 | — | 3 | — | µA |
| External Regulator (EXTVREG0) | $I_{EXTVREG}$ | Regulator | — | 215 | 250 | µA |
| | | Current Sensor | — | 7 | — | µA |
| PLL0 Oscillator (PLL0OSC) | $I_{PLLOSC}$ | Operating at 80 MHz | — | 1.75 | 1.86 | mA |
| Low-Power Oscillator (LPOSC0) | $I_{LPOSC}$ | Operating at 20 MHz | — | 190 | — | µA |
| | | Operating at 2.5 MHz | — | 40 | — | µA |
| Low-Frequency Oscillator (LFOSC0) | $I_{LFOSC}$ | Operating at 16.4 kHz,<br>$T_A$ = 25 °C | — | 215 | — | nA |
| | | Operating at 16.4 kHz,<br>$T_A$ = 85 °C | — | — | 500 | nA |

**Notes:**

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where $I_{DD}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

**Table 3.8. Internal Oscillators (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Low Power Oscillator (LPOSC0)** | | | | | | |
| Oscillator Frequency | $f_{LPOSC}$ | Full Temperature and Supply Range | 19 | 20 | 21 | MHz |
| | | $T_A$ = 25 °C, $V_{DD}$ = 3.3 V | 19.5 | 20 | 20.5 | MHz |
| Divided Oscillator Frequency | $f_{LPOSCD}$ | Full Temperature and Supply Range | 2.375 | 2.5 | 2.625 | MHz |
| Power Supply Sensitivity | $PSS_{LPOSC}$ | $T_A$ = 25 °C | — | 0.5 | — | %/V |
| Temperature Sensitivity | $TS_{LPOSC}$ | $V_{DD}$ = 3.3 V | — | 55 | — | ppm/°C |
| **Low Frequency Oscillator (LFOSC0)** | | | | | | |
| Oscillator Frequency | $f_{LFOSC}$ | Full Temperature and Supply Range | 13.4 | 16.4 | 19.7 | kHz |
| | | $T_A$ = 25 °C, $V_{DD}$ = 3.3 V | 15.8 | 16.4 | 17.3 | kHz |
| Power Supply Sensitivity | $PSS_{LFOSC}$ | $T_A$ = 25 °C | — | 2.4 | — | %/V |
| Temperature Sensitivity | $TS_{LFOSC}$ | $V_{DD}$ = 3.3 V | — | 0.2 | — | %/°C |
| **RTC0 Oscillator (RTC0OSC)** | | | | | | |
| Missing Clock Detector Trigger Frequency | $f_{RTCMCD}$ | | — | 8 | 15 | kHz |
| RTC Robust Duty Cycle Range | $DC_{RTC}$ | | 25 | — | 55 | % |
| ***Note:** PLL0OSC in free-running oscillator mode. | | | | | | |

**Table 3.9. External Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External Input CMOS Clock Frequency* | $f_{CMOS}$ | | 0 | — | 50 | MHz |
| External Input CMOS Clock High Time | $t_{CMOSH}$ | | 9 | — | — | ns |
| External Input CMOS Clock Low Time | $t_{CMOSL}$ | | 9 | — | — | ns |
| External Crystal Clock Frequency | $f_{XTAL}$ | | 0.01 | — | 30 | MHz |
| ***Note:** Minimum of 10 kHz during debug operations. | | | | | | |

**Table 3.11. IDAC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Performance** | | | | | | |
| Resolution | $N_{bits}$ | | | 10 | | Bits |
| Integral Nonlinearity | INL | | — | ±0.5 | ±2 | LSB |
| Differential Nonlinearity (Guaranteed Monotonic) | DNL | | — | ±0.5 | ±1 | LSB |
| Output Compliance Range | $V_{OCR}$ | | — | — | $V_{DD}$ – 1.0 | V |
| Full Scale Output Current | $I_{OUT}$ | 2 mA Range | 2.0 | 2.046 | 2.10 | mA |
| | | 1 mA Range | 0.99 | 1.023 | 1.05 | mA |
| | | 0.5 mA Range | 493 | 511.5 | 525 | µA |
| Offset Error | $E_{OFF}$ | | — | 250 | — | nA |
| Full Scale Error Tempco | $TC_{FS}$ | 2 mA Range | — | 100 | — | ppm/°C |
| VDD Power Supply Rejection Ratio | | 2 mA Range | — | -220 | — | ppm/V |
| Test Load Impedance (to $V_{SS}$) | $R_{TEST}$ | | — | 1 | — | kΩ |
| **Dynamic Performance** | | | | | | |
| Output Settling Time to 1/2 LSB | | min output to max output | — | 1.2 | — | µs |
| Startup Time | | | — | 3 | — | µs |

**Table 3.16. Comparator (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Positive Hysteresis Mode 3 (CPMD = 11) | $HYS_{CP+}$ | CMPHYP = 00 | — | 1.4 | — | mV |
| | | CMPHYP = 01 | — | 4 | — | mV |
| | | CMPHYP = 10 | — | 8 | — | mV |
| | | CMPHYP = 11 | — | 16 | — | mV |
| Negative Hysteresis Mode 3 (CPMD = 11) | $HYS_{CP-}$ | CMPHYN = 00 | — | 1.4 | — | mV |
| | | CMPHYN = 01 | — | –4 | — | mV |
| | | CMPHYN = 10 | — | –8 | — | mV |
| | | CMPHYN = 11 | — | –16 | — | mV |
| Input Range (CP+ or CP–) | $V_{IN}$ | | –0.25 | — | $V_{DD}$+0.25 | V |
| Input Pin Capacitance | $C_{CP}$ | PB2 Pins | — | 7.5 | — | pF |
| | | PB3 Pins | — | 10.5 | — | pF |
| Common-Mode Rejection Ratio | $CMRR_{CP}$ | | — | 75 | — | dB |
| Power Supply Rejection Ratio | $PSRR_{CP}$ | | — | 72 | — | dB |
| Input Offset Voltage | $V_{OFF}$ | | –10 | 0 | 10 | mV |
| Input Offset Tempco | $TC_{OFF}$ | | — | 3.5 | — | µV/°C |
| Reference DAC Resolution | $N_{Bits}$ | | | 6 | | bits |

## 3.2. Thermal Conditions

### Table 3.18. Thermal Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance* | $\theta_{JA}$ | LGA-92 Packages | — | 35 | — | °C/W |
| | | TQFP-80 Packages | — | 40 | — | °C/W |
| | | QFN-64 Packages | — | 25 | — | °C/W |
| | | TQFP-64 Packages | — | 30 | — | °C/W |
| | | QFN-40 Packages | — | 30 | — | °C/W |
| ***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad. | | | | | | |

## 3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

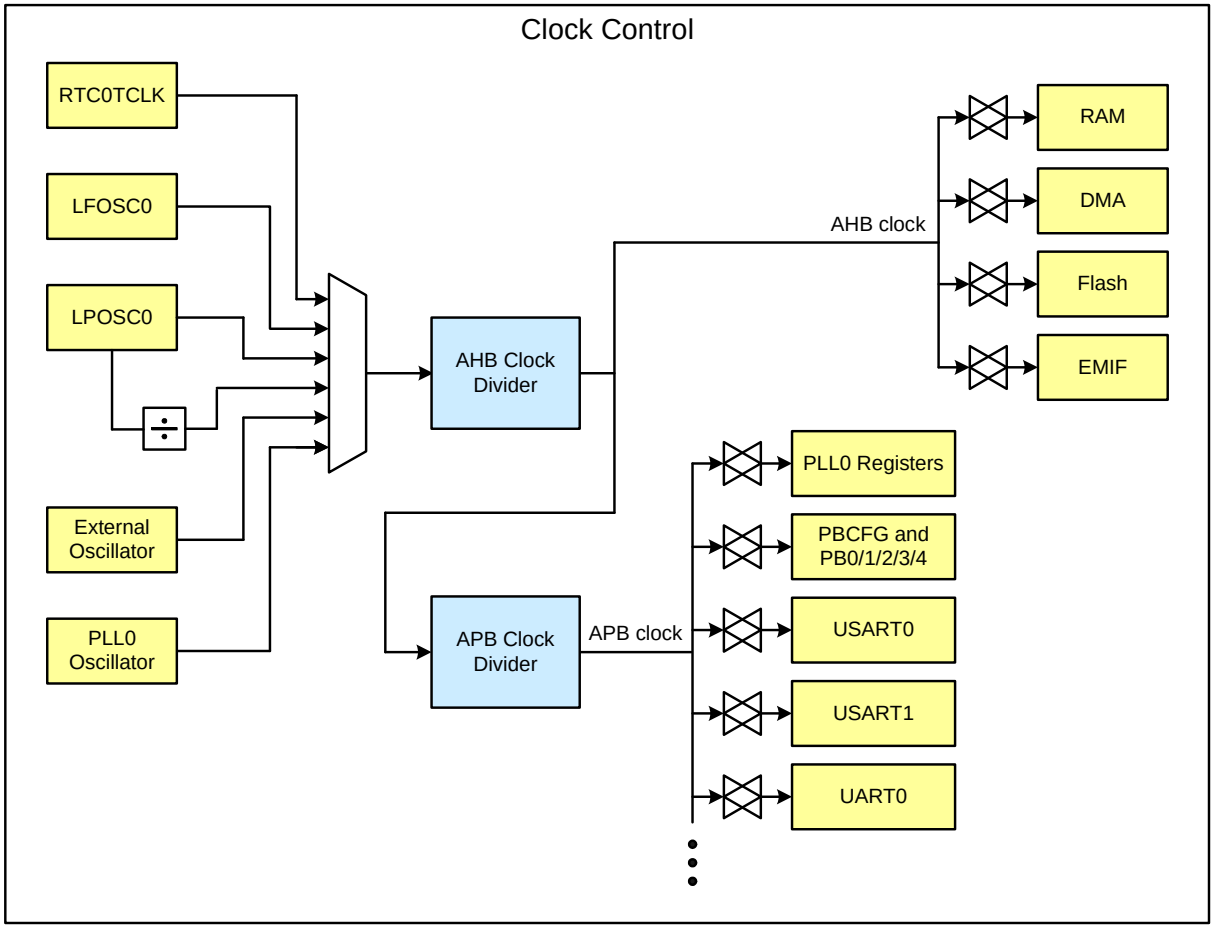
### Table 3.19. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Ambient Temperature Under Bias | $T_{BIAS}$ | | –55 | 125 | °C |
| Storage Temperature | $T_{STG}$ | | –65 | 150 | °C |
| Voltage on VDD | $V_{DD}$ | | $V_{SS}$–0.3 | 4.2 | V |
| Voltage on VREGIN | $V_{REGIN}$ | EXTVREG0 Not Used | $V_{SS}$–0.3 | 6.0 | V |
| | | EXTVREG0 Used | $V_{SS}$–0.3 | 3.6 | V |
| Voltage on VIO | $V_{IO}$ | | $V_{SS}$–0.3 | 4.2 | V |
| Voltage on VIOHD | $V_{IOHD}$ | | $V_{SS}$–0.3 | 6.5 | V |
| Voltage on I/O pins, non Port Bank 3 I/O | $V_{IN}$ | $\overline{\text{RESET}}$, $V_{IO} \geq 3.3$ V | $V_{SS}$–0.3 | 5.8 | V |
| | | $\overline{\text{RESET}}$, $V_{IO} < 3.3$ V | $V_{SS}$–0.3 | $V_{IO}$+2.5 | V |
| | | Port Bank 0, 1, and 2 I/O | $V_{SS}$–0.3 | $V_{IO}$+0.3 | V |
| | | Port Bank 4 I/O | $V_{SSHD}$–0.3 | $V_{IOHD}$+0.3 | V |
| ***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board. | | | | | |

## 4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.



## 4.5. Counters/Timers and PWM

### 4.5.1. Programmable Counter Array (EPCA0, PCA0, PCA1)

The SiM3C1xx devices include two types of PCA module: Enhanced and Standard.

The Enhanced Programmable Counter Array (EPCA0) and Standard Programmable Counter Array (PCA0, PCA1) modules are timer/counter systems allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

The Enhanced PCA module is multi-purpose, but is optimized for motor control applications. The EPCA module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never both active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers and outputs.
- Pulse-Width Modulation (PWM) waveform generation.
- High-speed square wave generation.
- Input capture mode.
- DMA capability for both input capture and waveform generation.
- PWM generation halt input.

The Standard PCA module (PCA) includes the following features:

- Two independent channels.
- Center- and edge-aligned waveform generation.
- Programmable clock divisor and multiple options for clock source selection.
- Pulse-Width Modulation waveform generation.

### 4.5.2. 32-bit Timer (TIMER0, TIMER1)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.
- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation.
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.

#### 4.6.4. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI module includes the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Programmable FIFO threshold level to request data service for DMA transfers.
- Support for multiple masters on the same data lines.

#### 4.6.5. I2C (I2C0, I2C1)

The I2C interface is a two-wire, bi-directional serial bus. The two clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

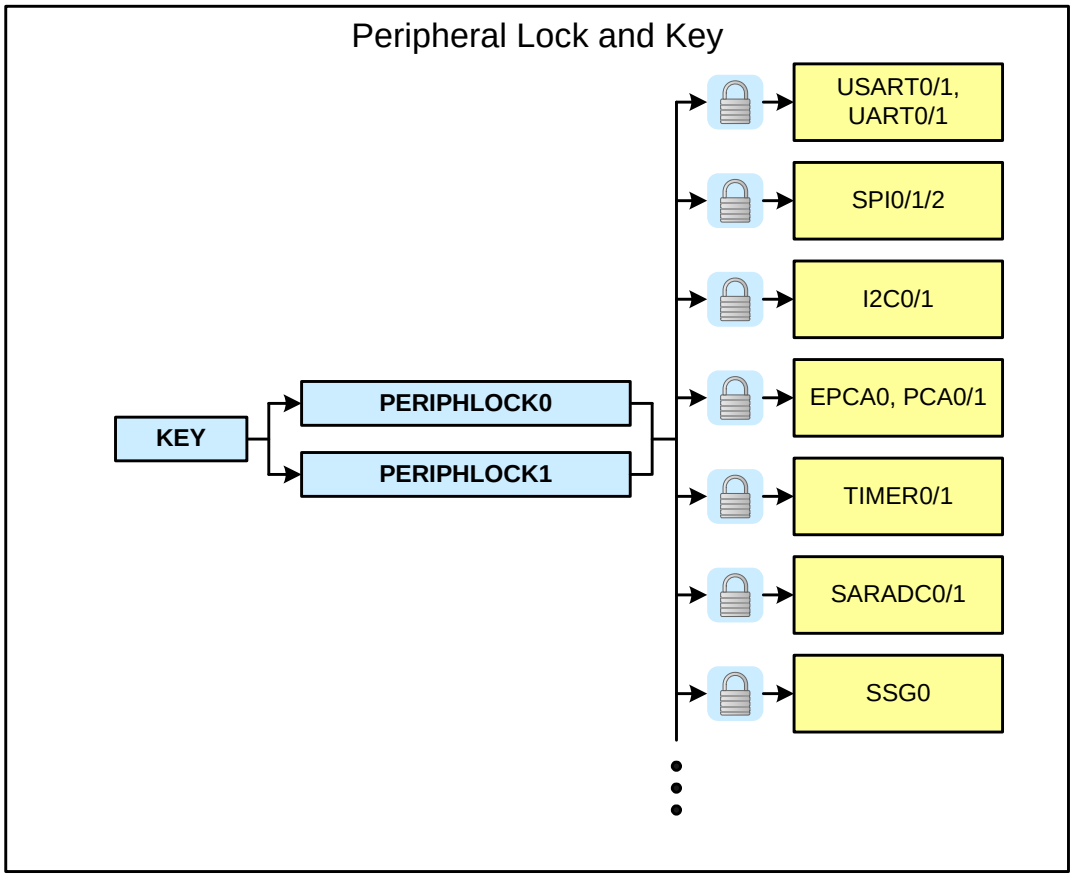
The I2C module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.

## 4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.




## 4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabiites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.

# 6. Pin Definitions and Packaging Information

## 6.1. SiM3C1x7 Pin Definitions

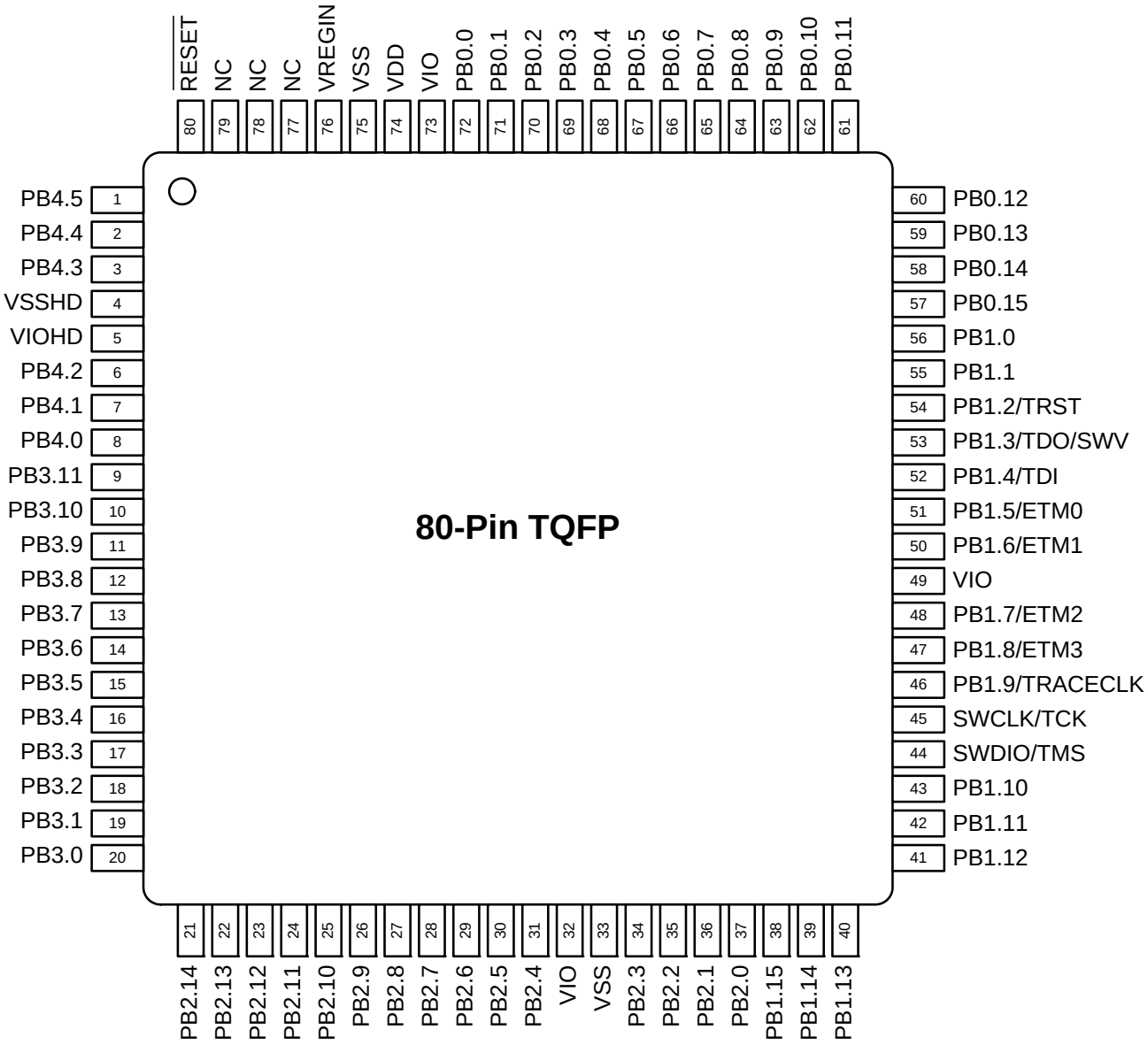



**Figure 6.1. SiM3C1x7-GQ Pinout**

**Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)**

| Pin Name | Type | Pin Numbers TQFP-80 | Pin Numbers LGA-92 | Crossbar Capability (see Port Config Section) | Port Match | External Memory Interface (m = muxed mode) | Port-Mapped Level Shifter | Output Toggle Logic | External Trigger Inputs | Analog or Additional Functions |
|---|---|---|---|---|---|---|---|---|---|---|
| PB0.8 | Standard I/O | 64 | A39 | XBR0 | ✓ | | | | | ADC0.7<br>CS0.7<br>IVC0.1 |
| PB0.9 | Standard I/O | 63 | A38 | XBR0 | ✓ | | | | | ADC0.8<br>RTC1 |
| PB0.10 | Standard I/O | 62 | A37 | XBR0 | ✓ | | | | | RTC2 |
| PB0.11 | Standard I/O | 61 | D4 | XBR0 | ✓ | | | | | ADC0.9<br>VREFGND |
| PB0.12 | Standard I/O | 60 | A36 | XBR0 | ✓ | | | | | ADC0.10<br>VREF |
| PB0.13 | Standard I/O | 59 | A35 | XBR0 | ✓ | | | | | IDAC0 |
| PB0.14 | Standard I/O | 58 | B27 | XBR0 | ✓ | | | | | IDAC1 |
| PB0.15 | Standard I/O | 57 | A34 | XBR0 | ✓ | | | | | XTAL1 |
| PB1.0 | Standard I/O | 56 | A33 | XBR0 | ✓ | | | | | XTAL2 |
| PB1.1 | Standard I/O | 55 | B25 | XBR0 | ✓ | | | | | ADC0.11 |
| PB1.2/TRST | Standard I/O /JTAG | 54 | A32 | XBR0 | ✓ | | | | | |
| PB1.3/TDO/ SWV | Standard I/O /JTAG/ Serial Wire Viewer | 53 | B24 | XBR0 | ✓ | | | | | ADC0.12<br>ADC1.12 |
| PB1.4/TDI | Standard I/O /JTAG | 52 | A31 | XBR0 | ✓ | | | | | ADC0.13<br>ADC1.13 |
| PB1.5/ETM0 | Standard I/O /ETM | 51 | B23 | XBR0 | ✓ | | | | | ADC0.14<br>ADC1.14 |
| PB1.6/ETM1 | Standard I/O /ETM | 50 | A30 | XBR0 | ✓ | | | | | ADC0.15<br>ADC1.15 |
| PB1.7/ETM2 | Standard I/O /ETM | 48 | B22 | XBR0 | ✓ | | | | | ADC1.11<br>CS0.8 |
| PB1.8/ETM3 | Standard I/O /ETM | 47 | B21 | XBR0 | ✓ | | | | | ADC1.10<br>CS0.9 |

**Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)**

| Pin Name | Type | Pin Numbers TQFP-80 | Pin Numbers LGA-92 | Crossbar Capability (see Port Config Section) | Port Match | External Memory Interface (m = muxed mode) | Port-Mapped Level Shifter | Output Toggle Logic | External Trigger Inputs | Analog or Additional Functions |
|---|---|---|---|---|---|---|---|---|---|---|
| PB2.6 | Standard I/O | 29 | B13 | XBR1 | ✓ | AD11m/ A3 | | Yes | INT0.6 INT1.6 | |
| PB2.7 | Standard I/O | 28 | A17 | XBR1 | ✓ | AD10m/ A2 | | Yes | INT0.7 INT1.7 | |
| PB2.8 | Standard I/O | 27 | B12 | XBR1 | ✓ | AD9m/ A1 | | Yes | | |
| PB2.9 | Standard I/O | 26 | A16 | XBR1 | ✓ | AD8m/ A0 | | Yes | | |
| PB2.10 | Standard I/O | 25 | B11 | XBR1 | ✓ | AD7m/ D7 | | Yes | | |
| PB2.11 | Standard I/O | 24 | A15 | XBR1 | ✓ | AD6m/ D6 | | Yes | | CMP0P.0 CMP1P.0 |
| PB2.12 | Standard I/O | 23 | A14 | XBR1 | ✓ | AD5m/ D5 | | Yes | | CMP0N.0 CMP1N.0 RTC0TCLK_OUT |
| PB2.13 | Standard I/O | 22 | A13 | XBR1 | ✓ | AD4m/ D4 | | Yes | | CMP0P.1 CMP1P.1 |
| PB2.14 | Standard I/O | 21 | D2 | XBR1 | ✓ | AD3m/ D3 | | Yes | | CMP0N.1 CMP1N.1 |
| PB3.0 | 5 V Tolerant I/O | 20 | A12 | XBR1 | ✓ | AD2m/ D2 | | | | CMP0P.2 CMP1P.2 |
| PB3.1 | 5 V Tolerant I/O | 19 | A11 | XBR1 | ✓ | AD1m/ D1 | | | | CMP0N.2 CMP1N.2 |
| PB3.2 | 5 V Tolerant I/O | 18 | A10 | XBR1 | ✓ | AD0m/ D0 | | | DAC0T0 DAC1T0 LPT0T0 | CMP0P.3 CMP1P.3 |
| PB3.3 | 5 V Tolerant I/O | 17 | B8 | XBR1 | ✓ | $\overline{WR}$ | | | DAC0T1 DAC1T1 INT0.8 INT1.8 | CMP0N.3 CMP1N.3 |

**Table 6.2. Pin Definitions and alternate functions for SiM3C1x6**

| Pin Name | Type | Pin Numbers | Crossbar Capability (see Port Config Section) | Port Match | External Memory Interface (m = muxed mode) | Port-Mapped Level Shifter | Output Toggle Logic | External Trigger Inputs | Analog or Additional Functions |
|---|---|---|---|---|---|---|---|---|---|
| VSS | Ground | 25<br>59 | | | | | | | |
| VDD | Power (Core) | 58 | | | | | | | |
| VIO | Power (I/O) | 24<br>39 | | | | | | | |
| VREGIN | Power (Regulator) | 60 | | | | | | | |
| VSSHD | Ground (High Drive) | 2 | | | | | | | |
| VIOHD | Power (High Drive) | 3 | | | | | | | |
| $\overline{\text{RESET}}$ | Active-low Reset | 64 | | | | | | | |
| SWCLK/TCK | Serial Wire / JTAG | 36 | | | | | | | |
| SWDIO/TMS | Serial Wire / JTAG | 35 | | | | | | | |
| PB0.0 | Standard I/O | 57 | XBR0 | ✓ | | | | | ADC0.2<br>CS0.1 |
| PB0.1 | Standard I/O | 56 | XBR0 | ✓ | | | | | ADC0.3<br>CS0.2 |
| PB0.2 | Standard I/O | 55 | XBR0 | ✓ | | | | | ADC0.4<br>CS0.3 |
| PB0.3 | Standard I/O | 54 | XBR0 | ✓ | | | | | ADC0.5<br>CS0.4 |
| PB0.4 | Standard I/O | 53 | XBR0 | ✓ | | | | | ADC0.6<br>CS0.5<br>IVC0.0 |
| PB0.5 | Standard I/O | 52 | XBR0 | ✓ | | | | | ADC0.7<br>CS0.6<br>IVC0.1 |
| PB0.6 | Standard I/O | 51 | XBR0 | ✓ | | | | | ADC0.8<br>CS0.7<br>RTC1 |

## 6.3. SiM3C1x4 Pin Definitions

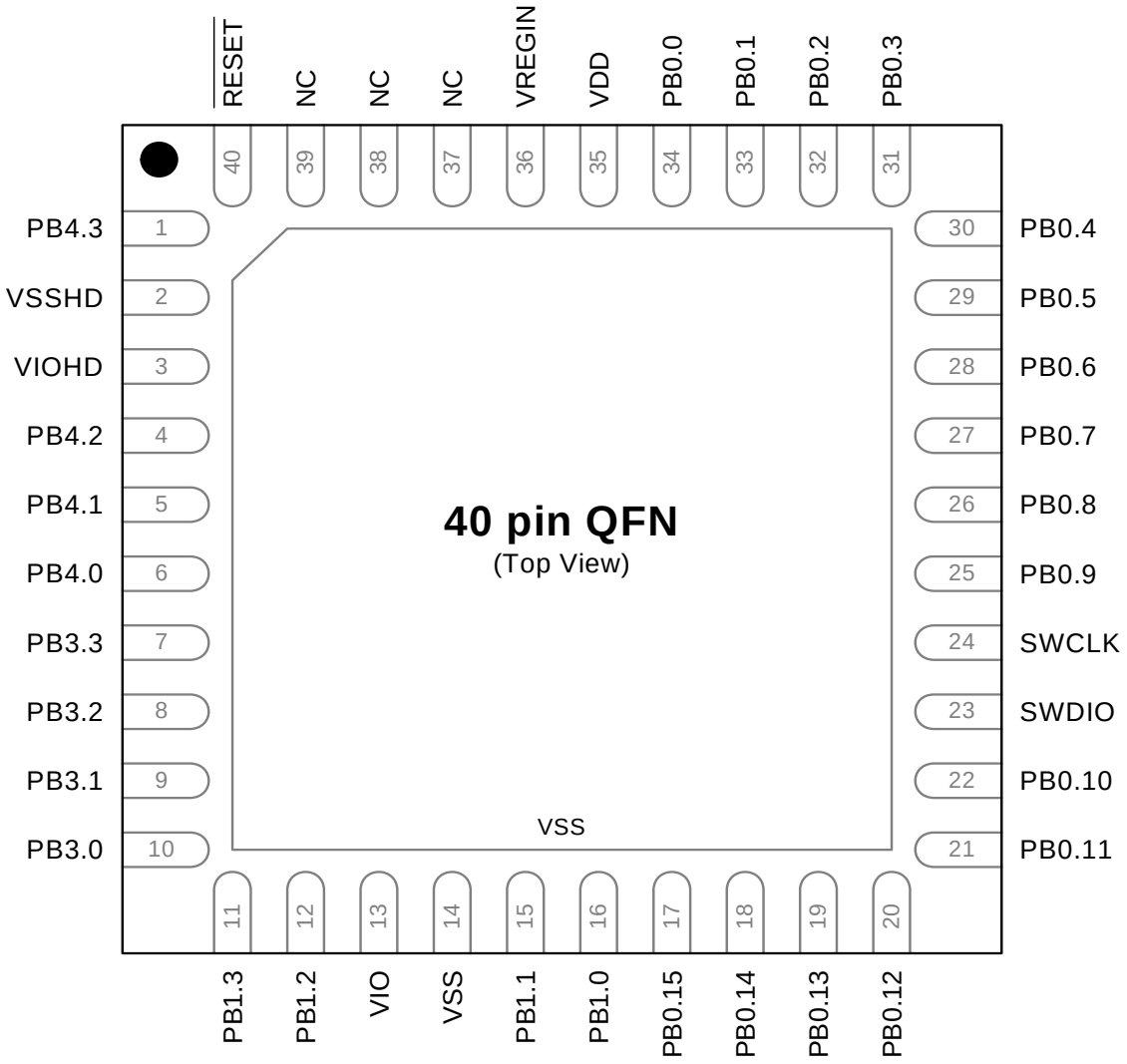



**Figure 6.5. SiM3C1x4-GM Pinout**

## 6.4. LGA-92 Package Specifications

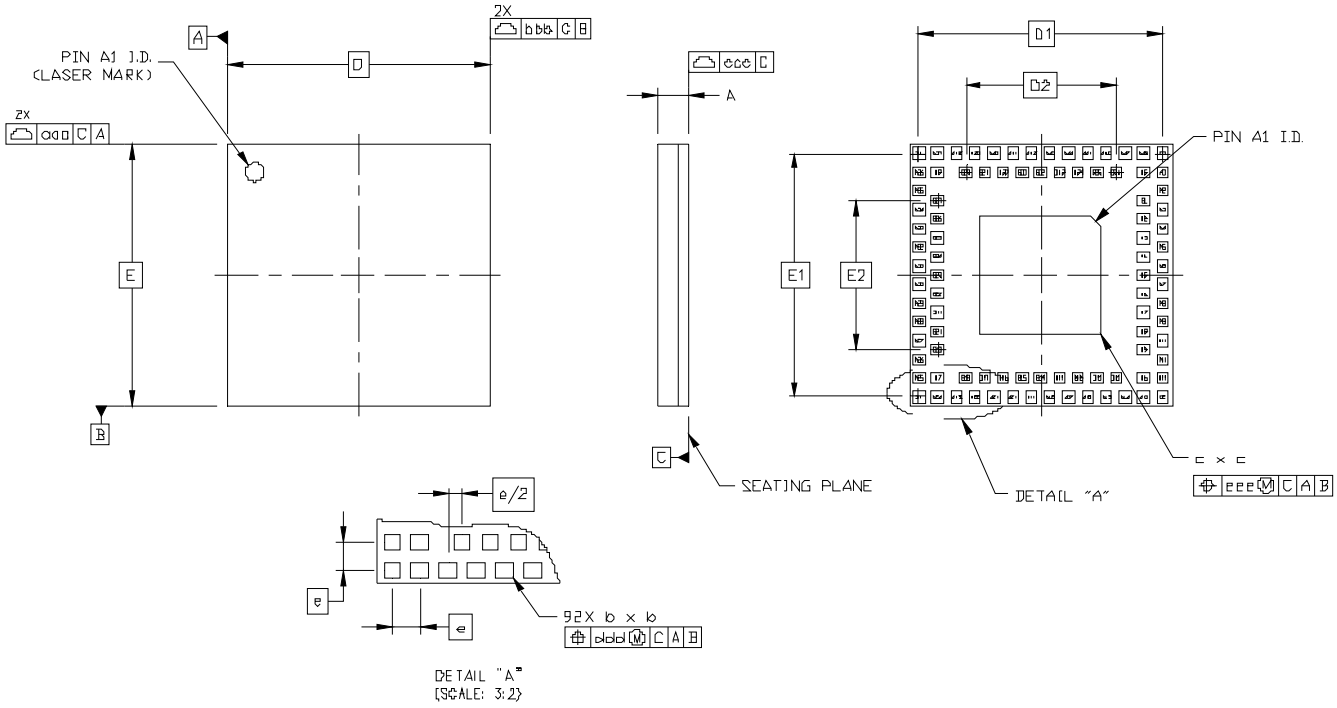



**Figure 6.6. LGA-92 Package Drawing**

**Table 6.4. LGA-92 Package Dimensions**

| Dimension | Min | Nominal | Max |
|---|---|---|---|
| **A** | 0.74 | 0.84 | 0.94 |
| **b** | 0.25 | 0.30 | 0.35 |
| **c** | 3.15 | 3.20 | 3.25 |
| **D** | | 7.00 BSC | |
| **D1** | | 6.50 BSC | |
| **D2** | | 4.00 BSC | |
| **e** | | 0.50 BSC | |
| **E** | | 7.00 BSC | |
| **E1** | | 6.50 BSC | |
| **E2** | | 4.00 BSC | |
| **aaa** | — | — | 0.10 |
| **bbb** | — | — | 0.10 |
| **ccc** | — | — | 0.08 |
| **ddd** | — | — | 0.10 |
| **eee** | — | — | 0.10 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

### 6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

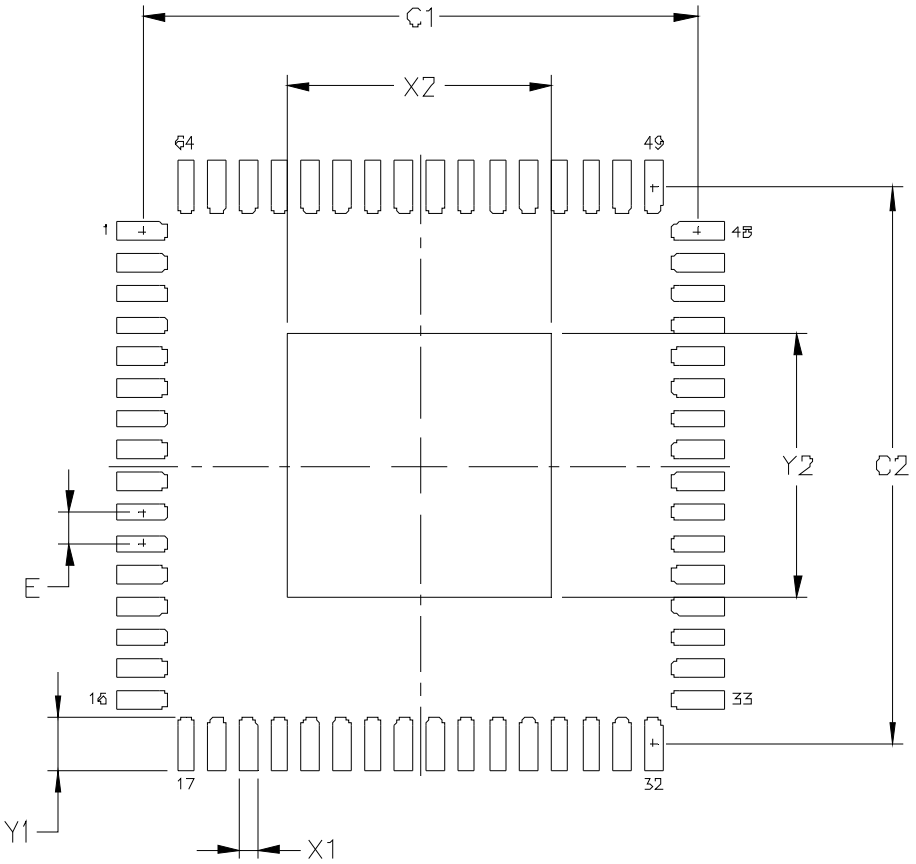



**Figure 6.11. QFN-64 Landing Diagram**

**Table 6.9. QFN-64 Landing Diagram Dimensions**

| Dimension | mm |
|---|---|
| **C1** | 8.90 |
| **C2** | 8.90 |
| **E** | 0.50 |
| **X1** | 0.30 |
| **Y1** | 0.85 |
| **X2** | 4.25 |
| **Y2** | 4.25 |

**Notes:**
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

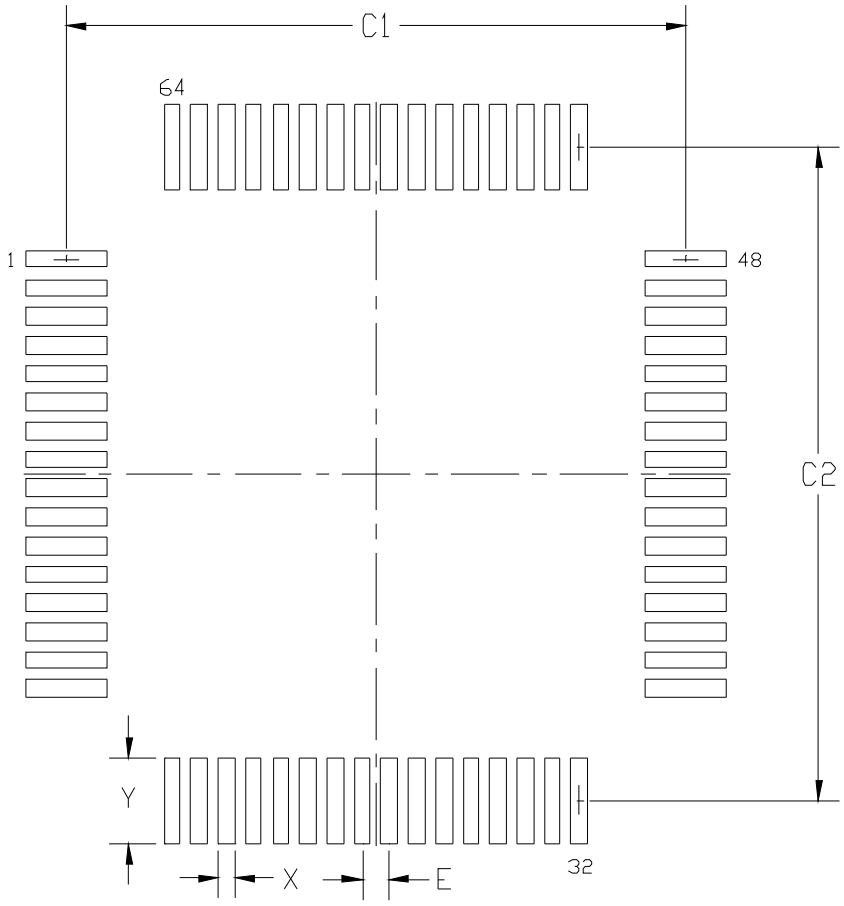



**Figure 6.13. TQFP-64 Landing Diagram**

**Table 6.11. TQFP-64 Landing Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| **C1** | 11.30 | 11.40 |
| **C2** | 11.30 | 11.40 |
| **E** | 0.50 BSC | |
| **X** | 0.20 | 0.30 |
| **Y** | 1.40 | 1.50 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

### 6.8.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.8.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

### 6.8.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.