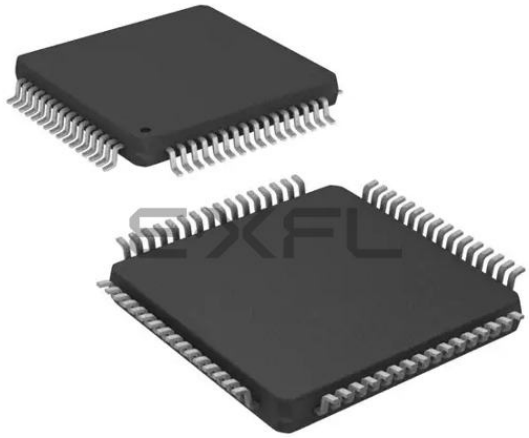

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Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3c166-b-gqr

2. Typical Connection Diagrams

This section provides typical connection diagrams for SiM3C1xx devices.

2.1. Power

Figure 2.1 shows a typical connection diagram for the power pins of the SiM3C1xx devices when the internal regulator is in use.

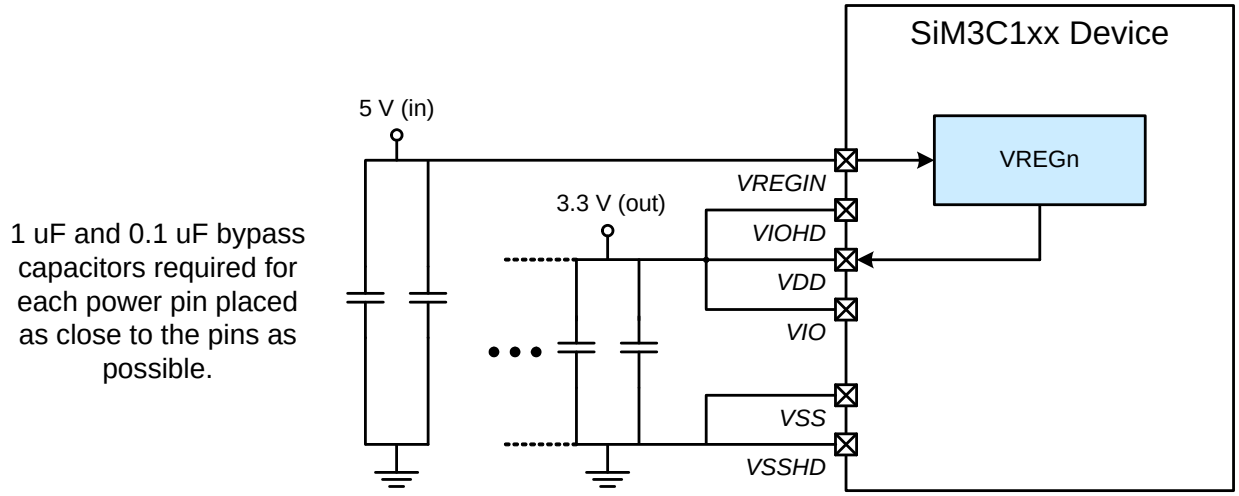


Figure 2.1. Connection Diagram with Voltage Regulator Used

Figure 2.2 shows a typical connection diagram for the power pins of the SiM3C1xx devices when the internal regulator is not used.

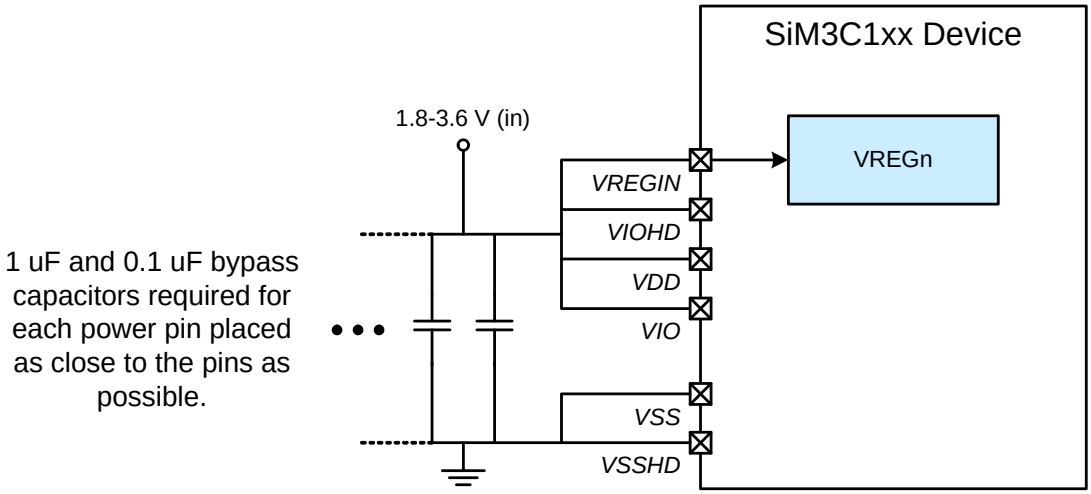


Figure 2.2. Connection Diagram with Voltage Regulator Not Used

Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	33	36.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	10.5	13.3	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	2.0	3.8	mA
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	22	24.9	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	10	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.2	3	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	30.5	35.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	8.5	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.7	—	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	20	23	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	5.3	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.0	—	mA
Power Mode 2[2,3,4]—Core halted with peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	19	22	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.3	—	mA
Power Mode 3[2,3]	I_{DD}	V_{DD} = 1.8 V, T_A = 25 °C	—	175	—	µA
		V_{DD} = 3.0 V, T_A = 25 °C	—	250	—	µA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Current on VDD						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time	t_{PM3FW}		—	425	—	µs
Power Mode 9 Wake Time	t_{PM9}		—	12	—	µs

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} High Supply Monitor Threshold (VDDHITHEN = 1)	V_{VDDMH}	Early Warning	2.10	2.20	2.30	V
		Reset	1.95	2.05	2.1	V
V_{DD} Low Supply Monitor Threshold (VDDHITHEN = 0)	V_{VDDML}	Early Warning	1.81	1.85	1.88	V
		Reset	1.70	1.74	1.77	V
V_{REGIN} Supply Monitor Threshold	V_{VREGM}	Early Warning	4.2	4.4	4.6	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.4	—	V
		Falling Voltage on V_{DD}	0.8	1	1.3	V
V_{DD} Ramp Time	t_{RMP}	Time to $V_{DD} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.4	1	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13	kHz
V_{DD} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.6. External Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range (at VREGIN)	V_{REGIN}		3.0	—	3.6	V
Output Voltage (at EXREGOUT)	$V_{EXREGOUT}$	Programmable in 100 mV steps	1.8	—	3.6	V
NPN Current Drive	I_{NPN}	400 mV Dropout	12	—	—	mA
PNP Current Drive	I_{PNP}	$V_{EXREGBD} > V_{REGIN}$- 1.5 V	–6	—	—	mA
EXREGBD Voltage (PNP Mode)	$V_{EXREGBD}$	V_{REGIN} >= 3.5 V	V_{REGIN} – 2.0	—	—	V
		V_{REGIN} < 3.5 V	1.5	—	—	V
Standalone Mode Output Current	$I_{EXTREGBD}$	400 mV Dropout	—	—	11.5	mA
External Capacitance with External BJT	C_{BJT}		4.7	—	—	µF
Standalone Mode Load Regulation	$LR_{STAND-ALONE}$		—	1	—	mV/mA
Standalone Mode External Capacitance	$C_{STAND-ALONE}$		47	—	—	nF
Current Limit Range	I_{LIMIT}	1 Ω Sense Resistor	10	—	720	mA
Current Limit Accuracy			—	—	10	%
Foldback Limit Accuracy			—	—	20	%
Current Sense Resistor	R_{SENSE}		—	—	1	Ω
Internal Pull-Down	R_{PD}		—	5	—	kΩ
Internal Pull-Up	R_{PU}		—	10	—	kΩ
Current Sensor						
Sensing Pin Voltage	$V_{EXTREGSP}$ $V_{EXTREGSN}$	Measured at EXTREGSP or EXTREGSN pin	2.2	—	V_{REGIN}	V
Differential Sensing Voltage	V_{DIFF}	($V_{EXTREGSP}$ – $V_{EXTREGSN}$)	10	—	1600	mV
Current at EXTREGSN Pin	$I_{EXTREGSN}$		—	8	—	µA
Current at EXTREGSP Pin	$I_{EXTREGSP}$		—	V_{DIFF} x 200 + 12	—	µA

Table 3.11. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{DD} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range	2.0	2.046	2.10	mA
		1 mA Range	0.99	1.023	1.05	mA
		0.5 mA Range	493	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VDD Power Supply Rejection Ratio		2 mA Range	—	-220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Table 3.17. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard I/O (PB0, PB1, and PB2), 5 V Tolerant I/O (PB3), and $\overline{\text{RESET}}$						
Output High Voltage*	V_{OH}	Low Drive, I_{OH} = –2 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –5 mA	V_{IO} – 0.7	—	—	V
Output Low Voltage*	V_{OL}	Low Drive, I_{OL} = 3 mA	—	—	0.6	V
		High Drive, I_{OL} = 12.5 mA	—	—	0.6	V
Input High Voltage	V_{IH}	1.8 ≤ V_{IO} ≤ 2.0	0.7 x V_{IO}	—	—	V
		2.0 ≤ V_{IO} ≤ 3.6	V_{IO} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}	PB0, PB1 and PB2 Pins	—	4	—	pF
		PB3 Pins	—	7	—	pF
Weak Pull-Up Current (Input Voltage = 0 V)	I_{PU}	V_{IO} = 1.8	–6	–3.5	–2	µA
		V_{IO} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	0 ≤ V_{IN} ≤ V_{IO}	–1	—	1	µA
Input Leakage Current of Port Bank 3 I/O, V_{IN} above V_{IO}	I_L	V_{IO} < V_{IN} < V_{IO}+2.0 V (pins without EXREG functions)	0	5	150	µA
		V_{IO} < V_{IN} < V_{REGIN} (pins with EXREG functions)	0	5	150	µA
High Drive I/O (PB4)						
Output High Voltage	V_{OH}	Standard Mode, Low Drive, I_{OH} = –3 mA	V_{IOHD} – 0.7	—	—	V
		Standard Mode, High Drive, I_{OH} = –10 mA	V_{IOHD} – 0.7	—	—	V
Output Low Voltage	V_{OL}	Standard Mode, Low Drive, I_{OH} = 3 mA	—	—	0.6	V
		Standard Mode, High Drive, I_{OH} = 12.5 mA	—	—	0.6	V
Output Rise Time	t_R	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

3.2. Thermal Conditions

Table 3.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	LGA-92 Packages	—	35	—	°C/W
		TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		V_{SS}–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	V_{SS}–0.3	6.0	V
		EXTVREG0 Used	V_{SS}–0.3	3.6	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIOHD	V_{IOHD}		V_{SS}–0.3	6.5	V
Voltage on I/O pins, non Port Bank 3 I/O	V_{IN}	$\overline{\text{RESET}}$, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$\overline{\text{RESET}}$, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		Port Bank 0, 1, and 2 I/O	V_{SS}–0.3	V_{IO}+0.3	V
		Port Bank 4 I/O	V_{SSHD}–0.3	V_{IOHD}+0.3	V
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

Table 3.19. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Power Dissipation at T_A = 85 °C	P_D	LGA-92 Package	—	570	mW
		TQFP-80 Package	—	500	mW
		QFN-64 Package	—	800	mW
		TQFP-64 Package	—	650	mW
		QFN-40 Package	—	650	mW
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and RESET pins are powered from the IO supply voltage. The SiM3C1xx devices are available in 40-pin or 64-pin QFN, 64-pin or 80-pin TQFP, or 92-pin LGA packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

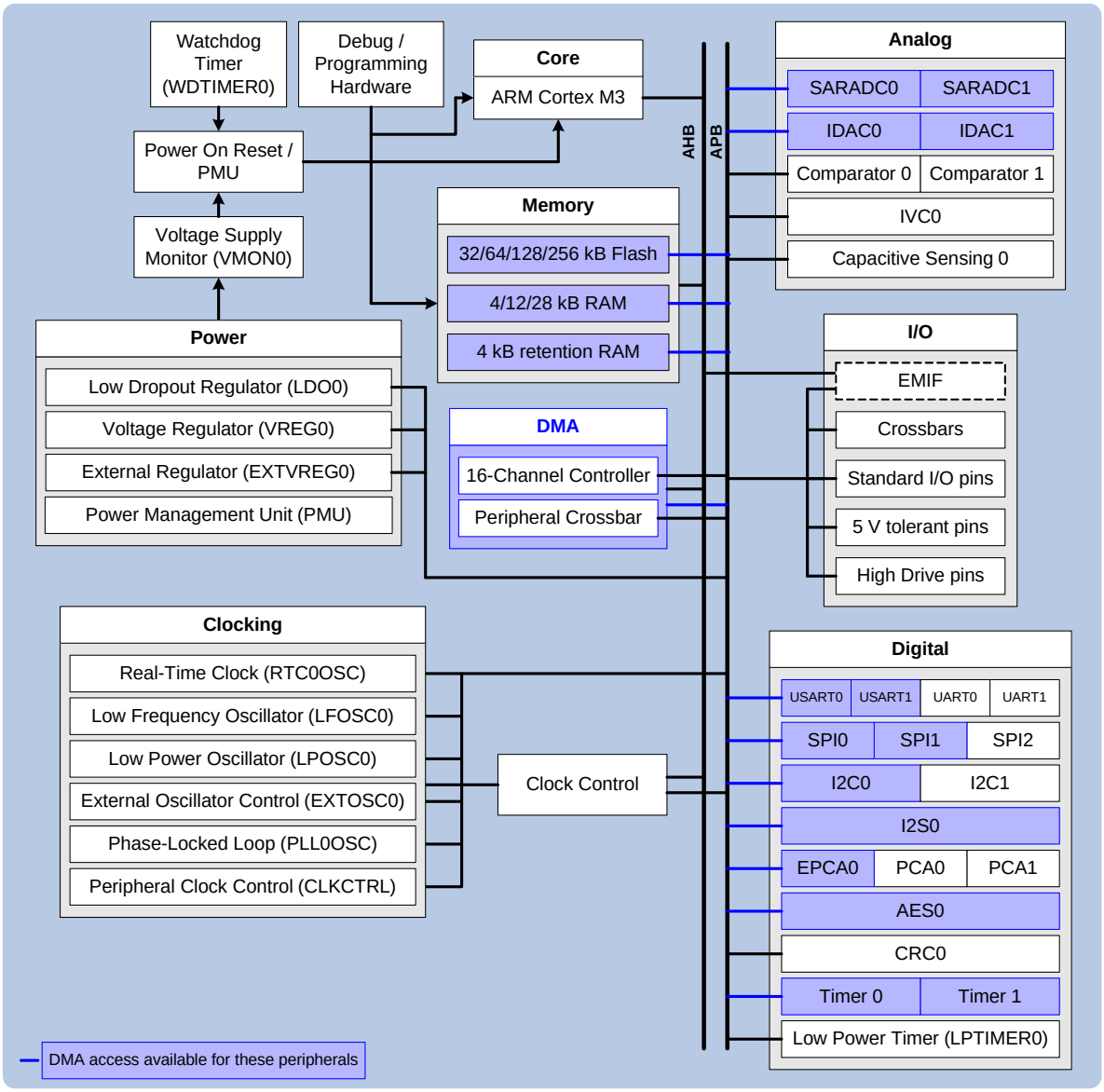


Figure 4.1. Precision32™ SiM3C1xx Family Block Diagram

4.1.5. Device Power Modes

The SiM3C1xx devices feature four low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low-Power Timer (LPT0), RTC0 (alarms and oscillator failure notification), Comparator 0, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0)

Normal Mode is the default mode of the device. The core and peripherals are fully operational, and instructions are executed from flash memory.

4.1.5.2. Power Mode 1

In Power Mode 1 the core and peripherals are fully operational, with instructions executing from RAM. Compared with Normal Mode, the active power consumption of the device in PM1 is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAM does not require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2

In Power Mode 2 the core halts and any enabled peripherals continue to run at the selected clock speed. The power consumption in PM2 corresponds to the AHB and APB clocks left enabled, thus the power can be tuned to the optimal level for the needs of the application. To place the device in PM2, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0 with the DMACTRL0 AHB clock disabled, PM2 can achieve similar power consumption to PM3, but with the ability to wake on APB-clocked interrupts. For example, enabling only the APB clock to the Ports will allow the firmware to wake on a PMATCH0, PBEXT0 or PBEXT1 interrupt with minimal impact on the supply current.

4.1.5.4. Power Mode 3

In Power Mode 3, the AHB and APB clocks are halted. The device may only wake from enabled interrupt sources which do not require the APB clock (RTC0ALRM, RTC0FAIL, LPTIMER0, VDDLOW and VREGLOW). A special fast wake option allows the device to operate at a very low level from the RTC0TCLK or LFOSC0 oscillator while in PM3, but quickly switch to the faster LPOSC0 when the wake event occurs. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

The device will enter PM3 on a WFI or WFE instruction. Because all AHB master clocks are disabled, the LPOSC will automatically halt and go into a low-power suspended state. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 9

In Power Mode 9, the core and all peripherals are halted, all clocks are stopped, and the pins and peripherals are set to a lower power mode. In addition, standard RAM contents are not preserved, though retention RAM contents are still available after exiting the power mode. This mode provides the lowest power consumption for the device, but requires an appropriate reset to exit. The available reset sources to wake from PM9 are controlled by the Power Management Unit (PMU).

Before entering PM9, the desired reset source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the RSTSRC0_CONFIG register must be set to indicate that PM9 is the desired power mode.

The device will enter PM9 on a WFI or WFE instruction, and remain in PM9 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.8. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.
- Clocks to all AHB peripherals are enabled.
- Clocks to all APB peripherals other than Watchdog Timer, EMIF0, and DMAXBAR are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VDD Supply Monitor and power-on resets, the $\overline{\text{RESET}}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled with the Low Frequency Oscillator (LFO0) as its clock source. Program execution begins at location 0x00000000.

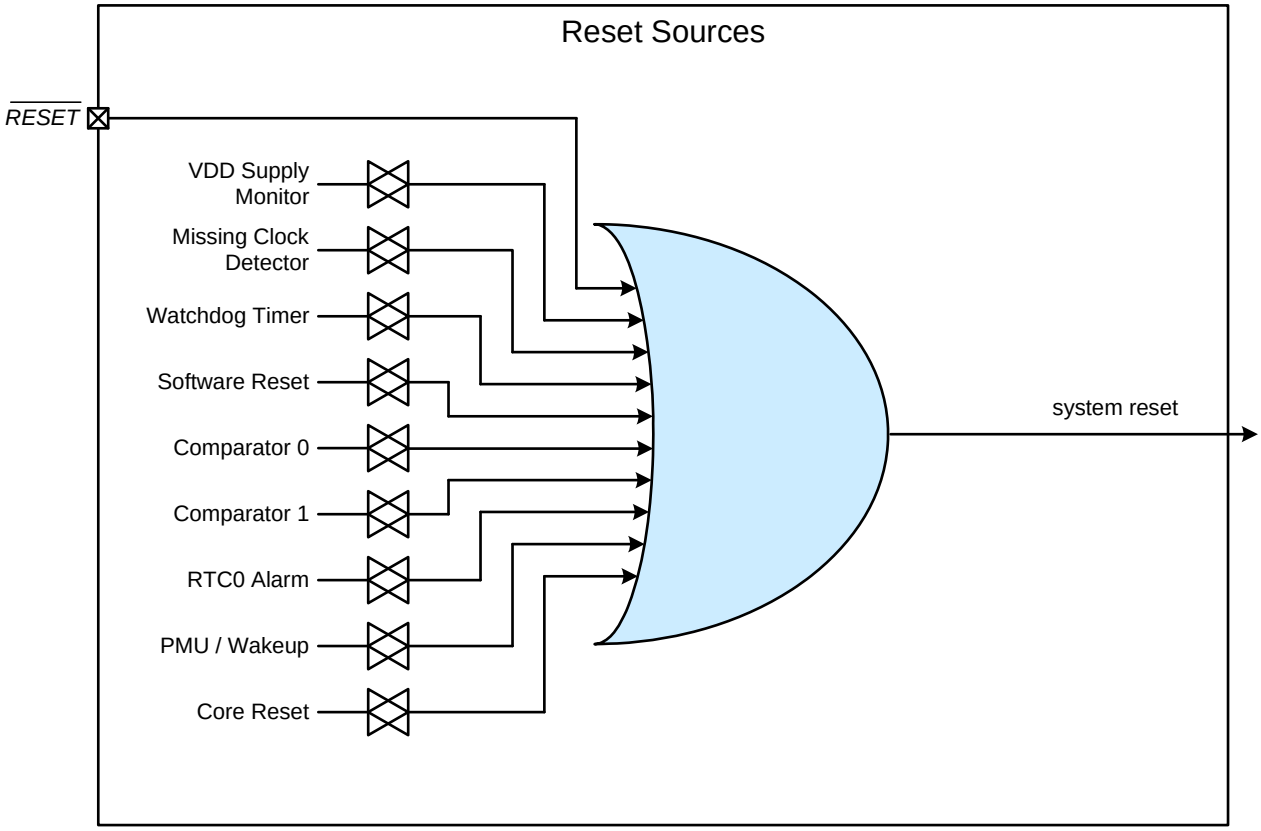


Table 5.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (kB)	External Memory Interface (EMIF)	Maximum Number of EMIF Address/Data Pins	Digital Port I/Os (Total)	Digital Port I/Os with High Drive Capability	Number of SARADC0 Channels	Number of SARADC1 Channels	Number of CAPSENSE0 Channels	Number of Comparator 0/1 Inputs (+/-)	Number of PMU Pin Wake Sources	JTAG Debugging Interface	ETM Debugging Interface	Serial Wire Debugging Interface	Lead-free (RoHS Compliant)	Package
SiM3C167-B-GM	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	LGA-92
SiM3C167-B-GQ	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	TQFP-80
SiM3C166-B-GM	256	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C166-B-GQ	256	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C164-B-GM	256	32			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C157-B-GM	128	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	LGA-92
SiM3C157-B-GQ	128	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	TQFP-80
SiM3C156-B-GM	128	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C156-B-GQ	128	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C154-B-GM	128	32			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C146-B-GM	64	16	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C146-B-GQ	64	16	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C144-B-GM	64	16			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C136-B-GM	32	8	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C136-B-GQ	32	8	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C134-B-GM	32	8			28	4	7	11	12	3/3	10			✓	✓	QFN-40

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	64	A39	XBR0	✓					ADC0.7 CS0.7 IVC0.1
PB0.9	Standard I/O	63	A38	XBR0	✓					ADC0.8 RTC1
PB0.10	Standard I/O	62	A37	XBR0	✓					RTC2
PB0.11	Standard I/O	61	D4	XBR0	✓					ADC0.9 VREFGND
PB0.12	Standard I/O	60	A36	XBR0	✓					ADC0.10 VREF
PB0.13	Standard I/O	59	A35	XBR0	✓					IDAC0
PB0.14	Standard I/O	58	B27	XBR0	✓					IDAC1
PB0.15	Standard I/O	57	A34	XBR0	✓					XTAL1
PB1.0	Standard I/O	56	A33	XBR0	✓					XTAL2
PB1.1	Standard I/O	55	B25	XBR0	✓					ADC0.11
PB1.2/TRST	Standard I/O /JTAG	54	A32	XBR0	✓					
PB1.3/TDO/ SWV	Standard I/O /JTAG/ Serial Wire Viewer	53	B24	XBR0	✓					ADC0.12 ADC1.12
PB1.4/TDI	Standard I/O /JTAG	52	A31	XBR0	✓					ADC0.13 ADC1.13
PB1.5/ETM0	Standard I/O /ETM	51	B23	XBR0	✓					ADC0.14 ADC1.14
PB1.6/ETM1	Standard I/O /ETM	50	A30	XBR0	✓					ADC0.15 ADC1.15
PB1.7/ETM2	Standard I/O /ETM	48	B22	XBR0	✓					ADC1.11 CS0.8
PB1.8/ETM3	Standard I/O /ETM	47	B21	XBR0	✓					ADC1.10 CS0.9

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.9/ TRACECLK	Standard I/O /ETM	46	A28	XBR0	✓					ADC1.9
PB1.10	Standard I/O	43	A26	XBR0	✓	A23m/ A15			DMA0T1	ADC1.8
PB1.11	Standard I/O	42	A25	XBR0	✓	A22m/ A14			DMA0T0	ADC1.7
PB1.12	Standard I/O	41	D3	XBR0	✓	A21m/ A13				ADC1.6
PB1.13	Standard I/O	40	A24	XBR0	✓	A20m/ A12			ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.14	Standard I/O	39	A23	XBR0	✓	A19m/ A11			ADC1T15 WAKE.1	ADC1.4 CS0.11
PB1.15	Standard I/O	38	A22	XBR0	✓	A18m/ A10			WAKE.2	ADC1.3 CS0.12
PB2.0	Standard I/O	37	B17	XBR1	✓	A17m/ A9	LSI0	Yes	INT0.0 INT1.0 WAKE.3	ADC1.2 CS0.13
PB2.1	Standard I/O	36	A21	XBR1	✓	A16m/ A8	LSI1	Yes	INT0.1 INT1.1 WAKE.4	ADC1.1 CS0.14
PB2.2	Standard I/O	35	B16	XBR1	✓	AD15m/ A7	LSI2	Yes	INT0.2 INT1.2 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB2.3	Standard I/O	34	A20	XBR1	✓	AD14m/ A6	LSI3	Yes	INT0.3 INT1.3 WAKE.6	
PB2.4	Standard I/O	31	B14	XBR1	✓	AD13m/ A5	LSI4	Yes	INT0.4 INT1.4 WAKE.7	
PB2.5	Standard I/O	30	A18	XBR1	✓	AD12m / A4	LSI5	Yes	INT0.5 INT1.5	

6.2. SiM3C1x6 Pin Definitions

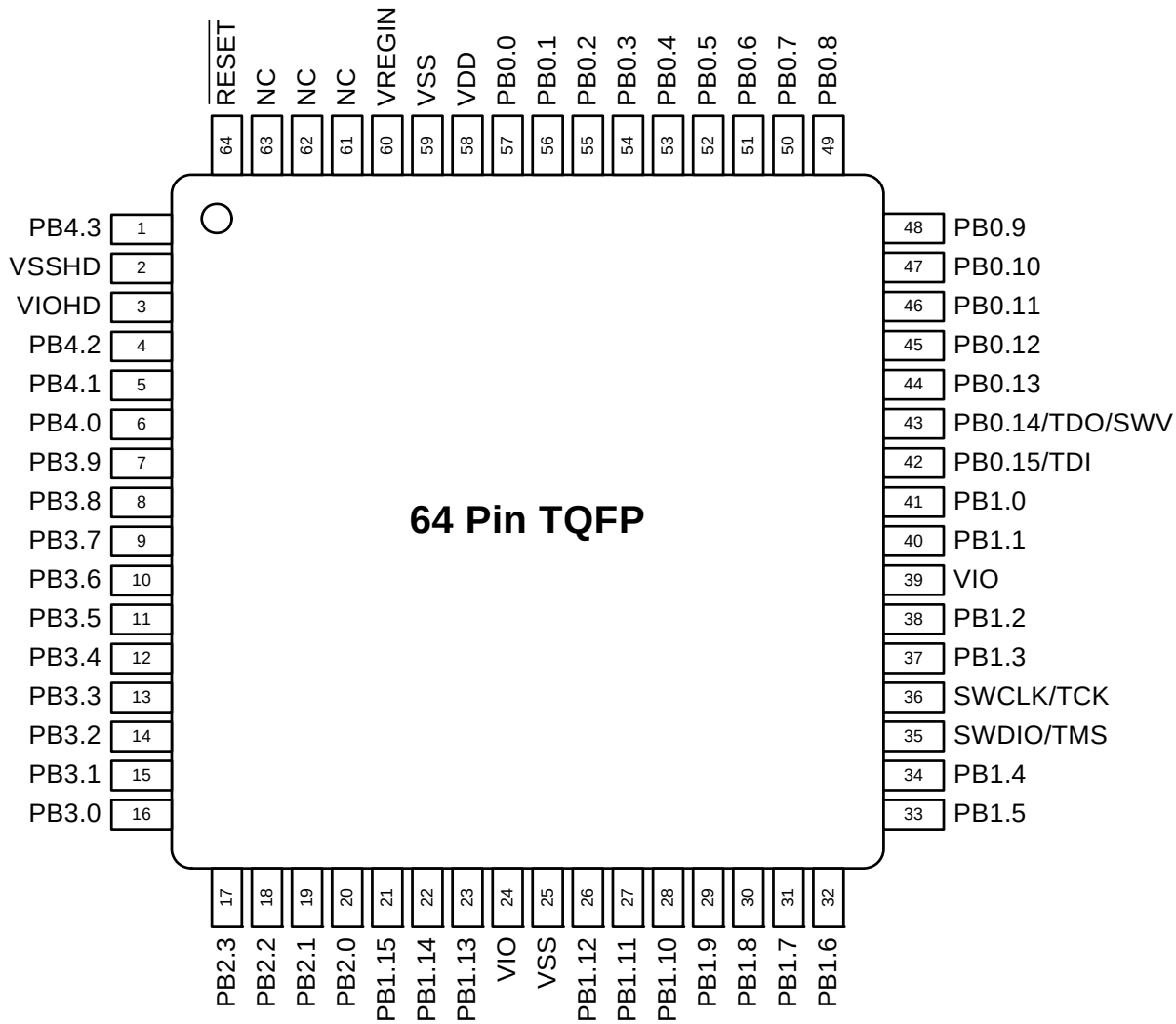


Figure 6.3. SiM3C1x6-GQ Pinout

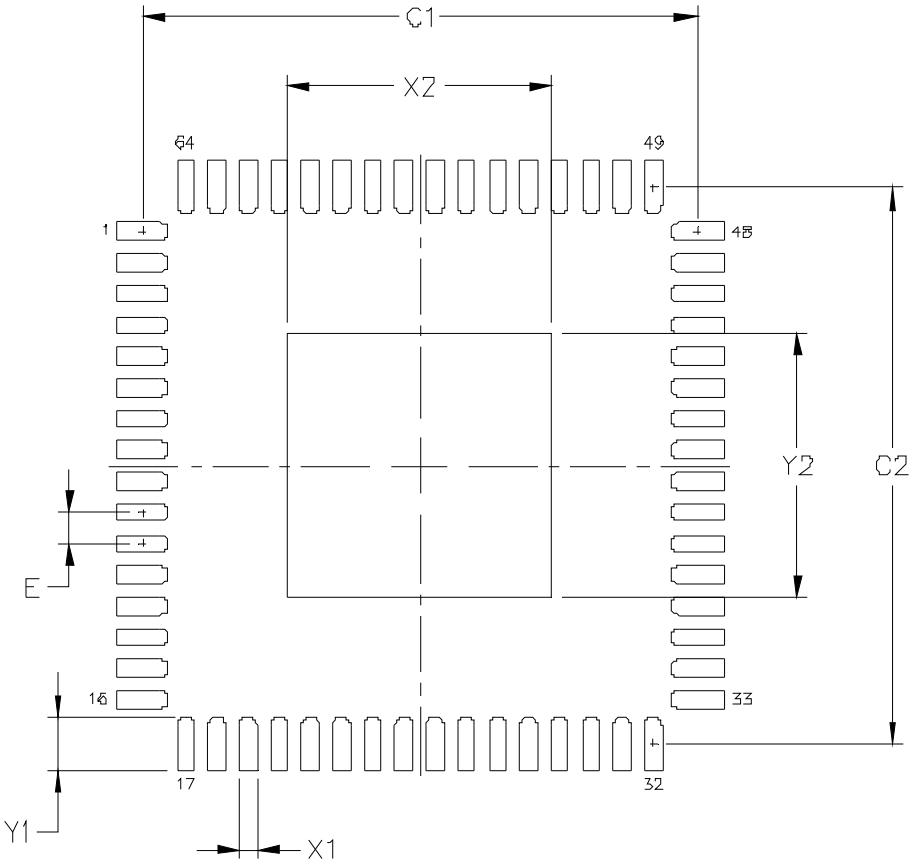


Figure 6.11. QFN-64 Landing Diagram

Table 6.9. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

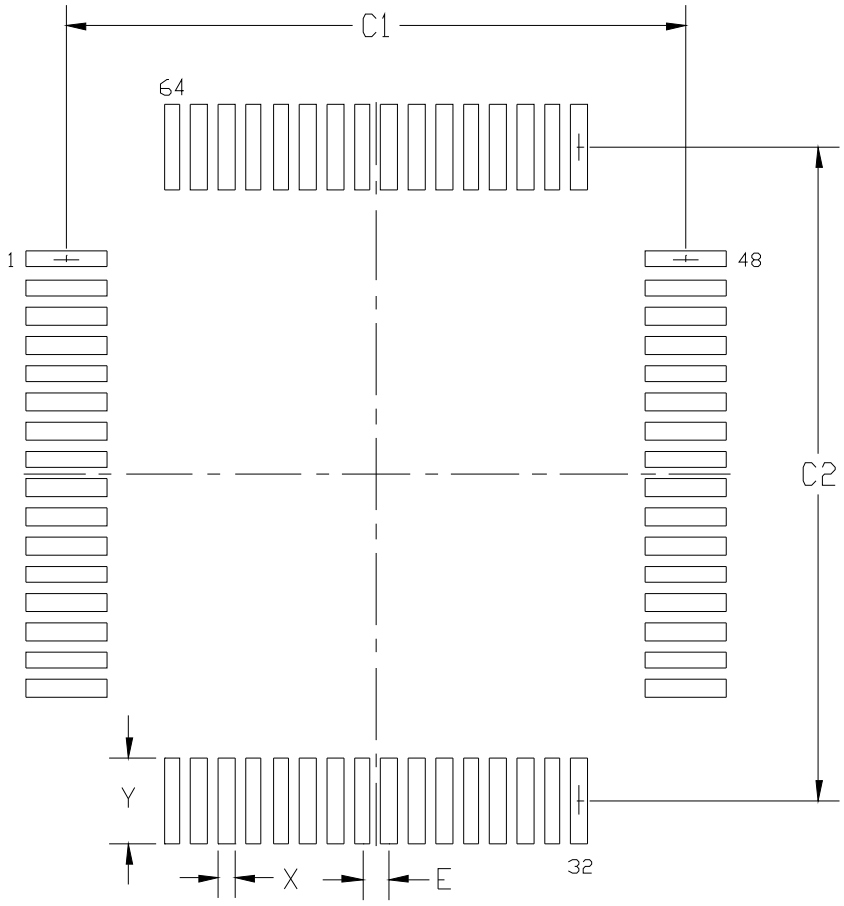


Figure 6.13. TQFP-64 Landing Diagram

Table 6.11. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

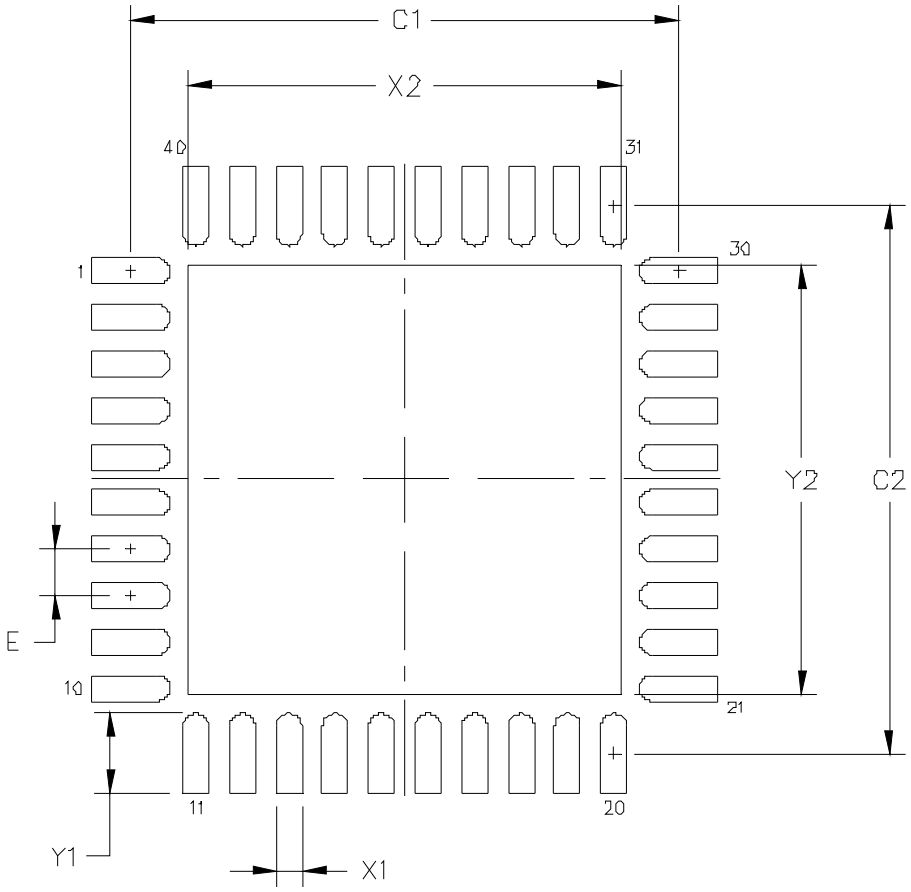
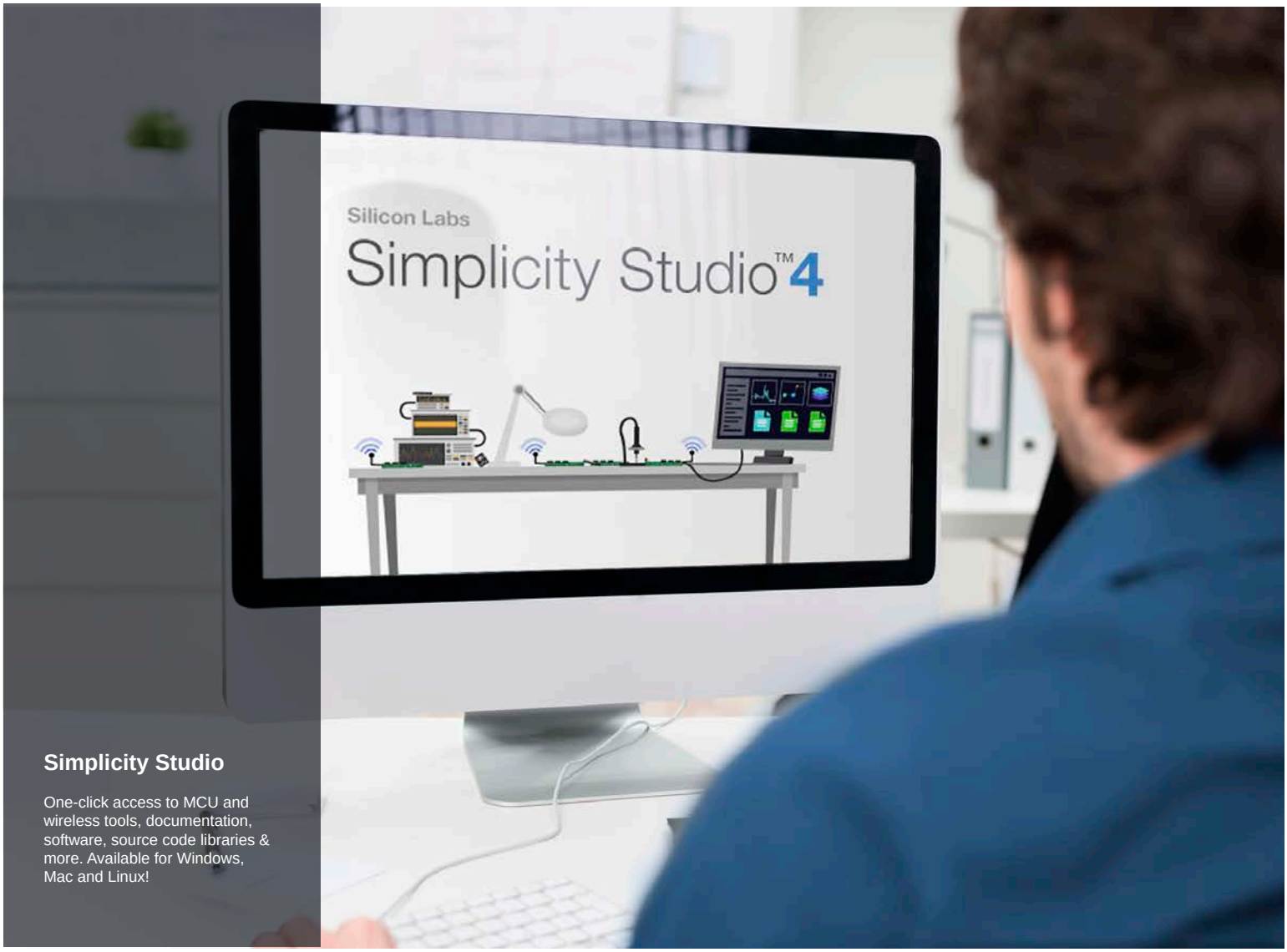


Figure 6.15. QFN-40 Landing Diagram

Table 6.13. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.



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