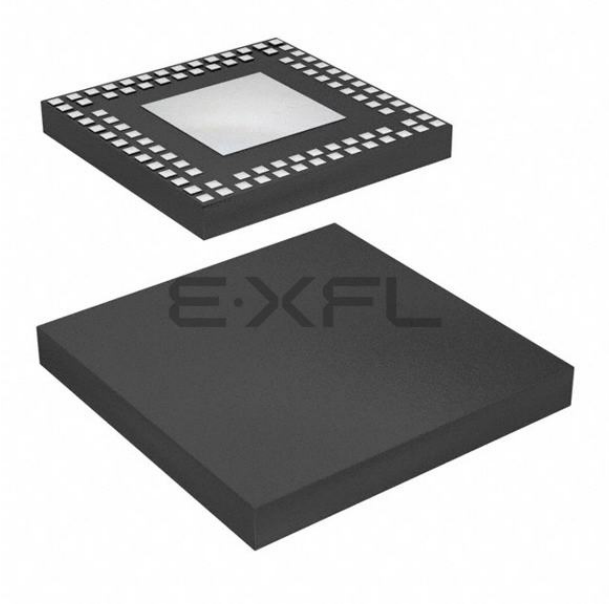

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 65 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 32x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 92-VFLGA Dual Rows, Exposed Pad |
| Supplier Device Package | 92-LGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/sim3c167-b-gmr |

# Table of Contents

**Table 3.2. Power Consumption**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital Core Supply Current** | | | | | | |
| Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks ON | $I_{DD}$ | $F_{AHB}$ = 80 MHz, $F_{APB}$ = 40 MHz | — | 33 | 36.5 | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 20 MHz | — | 10.5 | 13.3 | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 2.5 MHz | — | 2.0 | 3.8 | mA |
| Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks OFF | $I_{DD}$ | $F_{AHB}$ = 80 MHz, $F_{APB}$ = 40 MHz | — | 22 | 24.9 | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 20 MHz | — | 7.8 | 10 | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 2.5 MHz | — | 1.2 | 3 | mA |
| Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks ON | $I_{DD}$ | $F_{AHB}$ = 80 MHz, $F_{APB}$ = 40 MHz | — | 30.5 | 35.5 | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 20 MHz | — | 8.5 | — | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 2.5 MHz | — | 1.7 | — | mA |
| Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks OFF | $I_{DD}$ | $F_{AHB}$ = 80 MHz, $F_{APB}$ = 40 MHz | — | 20 | 23 | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 20 MHz | — | 5.3 | — | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 2.5 MHz | — | 1.0 | — | mA |
| Power Mode 2[2,3,4]—Core halted with peripheral clocks ON | $I_{DD}$ | $F_{AHB}$ = 80 MHz, $F_{APB}$ = 40 MHz | — | 19 | 22 | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 20 MHz | — | 7.8 | — | mA |
| | | $F_{AHB}$ = $F_{APB}$ = 2.5 MHz | — | 1.3 | — | mA |
| Power Mode 3[2,3] | $I_{DD}$ | $V_{DD}$ = 1.8 V, $T_A$ = 25 °C | — | 175 | — | µA |
| | | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | — | 250 | — | µA |

**Notes:**
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where $I_{DD}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

**Table 3.2. Power Consumption (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Mode 9[2,3]—Low Power Shutdown with VREG0 disabled, powered through VDD and VIO | $I_{DD}$ | RTC Disabled, $V_{DD}$ = 1.8 V, $T_A$ = 25 °C | — | 85 | — | nA |
| | | RTC w/ 16.4 kHz LFO, $V_{DD}$ = 1.8 V, $T_A$ = 25 °C | — | 350 | — | nA |
| | | RTC w/ 32.768 kHz Crystal, $V_{DD}$ = 1.8 V, $T_A$ = 25 °C | — | 620 | — | nA |
| | | RTC Disabled, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | — | 145 | — | nA |
| | | RTC w/ 16.4 kHz LFO, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | — | 500 | — | nA |
| | | RTC w/ 32.768 kHz Crystal, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | — | 800 | — | nA |
| Power Mode 9[2,3]—Low Power Shutdown with VREG0 in low-power mode, VDD and VIO powered through VREG0 (Includes VREG0 current) | $I_{VREGIN}$ | RTC Disabled, VREGIN = 5 V, $T_A$ = 25 °C | — | 300 | — | nA |
| | | RTC w/ 16.4 kHz LFO, VREGIN = 5 V, $T_A$ = 25 °C | — | 650 | — | nA |
| | | RTC w/ 32.768 kHz Crystal, VREGIN = 5 V, $T_A$ = 25 °C | — | 950 | — | nA |
| VIOHD Current (High-drive I/O disabled) | $I_{VIOHD}$ | HV Mode (default) | — | 2.5 | 5 | µA |
| | | LV Mode | — | 2 | — | nA |

**Notes:**

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where $I_{DD}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

**Table 3.6. External Regulator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range (at VREGIN) | $V_{REGIN}$ | | 3.0 | — | 3.6 | V |
| Output Voltage (at EXREGOUT) | $V_{EXREGOUT}$ | Programmable in 100 mV steps | 1.8 | — | 3.6 | V |
| NPN Current Drive | $I_{NPN}$ | 400 mV Dropout | 12 | — | — | mA |
| PNP Current Drive | $I_{PNP}$ | $V_{EXREGBD} > V_{REGIN}$ - 1.5 V | –6 | — | — | mA |
| EXREGBD Voltage (PNP Mode) | $V_{EXREGBD}$ | $V_{REGIN}$ >= 3.5 V | $V_{REGIN}$ – 2.0 | — | — | V |
| | | $V_{REGIN}$ < 3.5 V | 1.5 | — | — | V |
| Standalone Mode Output Current | $I_{EXTREGBD}$ | 400 mV Dropout | — | — | 11.5 | mA |
| External Capacitance with External BJT | $C_{BJT}$ | | 4.7 | — | — | µF |
| Standalone Mode Load Regulation | $LR_{STAND\text{-}ALONE}$ | | — | 1 | — | mV/mA |
| Standalone Mode External Capacitance | $C_{STAND\text{-}ALONE}$ | | 47 | — | — | nF |
| Current Limit Range | $I_{LIMIT}$ | 1 Ω Sense Resistor | 10 | — | 720 | mA |
| Current Limit Accuracy | | | — | — | 10 | % |
| Foldback Limit Accuracy | | | — | — | 20 | % |
| Current Sense Resistor | $R_{SENSE}$ | | — | — | 1 | Ω |
| Internal Pull-Down | $R_{PD}$ | | — | 5 | — | kΩ |
| Internal Pull-Up | $R_{PU}$ | | — | 10 | — | kΩ |
| **Current Sensor** | | | | | | |
| Sensing Pin Voltage | $V_{EXTREGSP}$ $V_{EXTREGSN}$ | Measured at EXTREGSP or EXTREGSN pin | 2.2 | — | $V_{REGIN}$ | V |
| Differential Sensing Voltage | $V_{DIFF}$ | ($V_{EXTREGSP}$ – $V_{EXTREGSN}$) | 10 | — | 1600 | mV |
| Current at EXTREGSN Pin | $I_{EXTREGSN}$ | | — | 8 | — | µA |
| Current at EXTREGSP Pin | $I_{EXTREGSP}$ | | — | $V_{DIFF}$ x 200 + 12 | — | µA |

**Table 3.14. Voltage Reference Electrical Characteristics**

$V_{DD}$ = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Internal Fast Settling Reference** | | | | | | |
| Output Voltage | $V_{REFFS}$ | –40 to +85 °C, $V_{DD}$ = 1.8–3.6 V | 1.62 | 1.65 | 1.68 | V |
| Temperature Coefficient | $TC_{REFFS}$ | | — | 50 | — | ppm/°C |
| Turn-on Time | $t_{REFFS}$ | | — | — | 1.5 | µs |
| Power Supply Rejection | $PSRR_{REFFS}$ | | — | 400 | — | ppm/V |
| **On-Chip Precision Reference (VREF0)** | | | | | | |
| Valid Supply Range | $V_{DD}$ | VREF2X = 0 | 1.8 | — | 3.6 | V |
| | | VREF2X = 1 | 2.7 | — | 3.6 | V |
| Output Voltage | $V_{REFP}$ | 25 °C ambient, VREF2X = 0 | 1.195 | 1.2 | 1.205 | V |
| | | 25 °C ambient, VREF2X = 1 | 2.39 | 2.4 | 2.41 | V |
| Short-Circuit Current | $I_{SC}$ | | — | — | 10 | mA |
| Temperature Coefficient | $TC_{VREFP}$ | | — | 25 | — | ppm/°C |
| Load Regulation | $LR_{VREFP}$ | Load = 0 to 200 µA to VREFGND | — | 4.5 | — | ppm/µA |
| Load Capacitor | $C_{VREFP}$ | Load = 0 to 200 µA to VREFGND | 0.1 | — | — | µF |
| Turn-on Time | $t_{VREFPON}$ | 4.7 µF tantalum, 0.1 µF ceramic bypass | — | 3.8 | — | ms |
| | | 0.1 µF ceramic bypass | — | 200 | — | µs |
| Power Supply Rejection | $PSRR_{VREFP}$ | VREF2X = 0 | — | 320 | — | ppm/V |
| | | VREF2X = 1 | — | 560 | — | ppm/V |
| **External Reference** | | | | | | |
| Input Current | $I_{EXTREF}$ | Sample Rate = 250 ksps; VREF = 3.0 V | — | 5.25 | — | µA |

**Table 3.17. Port I/O (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Fall Time | $t_F$ | Slew Rate Mode 0, $V_{IOHD}$ = 5 V | — | 50 | — | ns |
| | | Slew Rate Mode 1, $V_{IOHD}$ = 5 V | — | 300 | — | ns |
| | | Slew Rate Mode 2, $V_{IOHD}$ = 5 V | — | 1 | — | µs |
| | | Slew Rate Mode 3, $V_{IOHD}$ = 5 V | — | 3 | — | µs |
| Input High Voltage | $V_{IH}$ | 1.8 V≤ $V_{IOHD}$ ≤ 2.0 V | 0.7 x $V_{IOHD}$ | — | — | V |
| | | 2.0 V≤ $V_{IOHD}$ ≤ 6 V | $V_{IOHD}$ – 0.6 | — | — | V |
| Input Low Voltage | $V_{IL}$ | | — | — | 0.6 | V |
| N-Channel Sink Current Limit (2.7 V ≤ $V_{IOHD}$ ≤ 6 V, $V_{OL}$ = 0.8 V) See Figure 3.1 | $I_{SINKL}$ | Mode 0 | — | 1.75 | — | mA |
| | | Mode 1 | — | 2.5 | — | |
| | | Mode 2 | — | 3.5 | — | |
| | | Mode 3 | — | 4.75 | — | |
| | | Mode 4 | — | 7 | — | |
| | | Mode 5 | — | 9.5 | — | |
| | | Mode 6 | — | 14 | — | |
| | | Mode 7 | — | 18.75 | — | |
| | | Mode 8 | — | 28.25 | — | |
| | | Mode 9 | — | 37.5 | — | |
| | | Mode 10 | — | 56.25 | — | |
| | | Mode 11 | — | 75 | — | |
| | | Mode 12 | — | 112.5 | — | |
| | | Mode 13 | — | 150 | — | |
| | | Mode 14 | — | 225 | — | |
| | | Mode 15 | — | 300 | — | |
| Total N-Channel Sink Current on P4.0-P4.5 (DC) | $I_{SINKLT}$ | | — | — | 400 | mA |

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ $V_{OL}$ adhere to the low drive setting.

## 4.1. Power

### 4.1.1. LDO and Voltage Regulator (VREG0)

The SiM3C1xx devices include two internal regulators: the core LDO Regulator and the Voltage Regulator (VREG0).

The LDO Regulator converts a 1.8–3.6 V supply to the core operating voltage of 1.8 V. This LDO consumes little power and provides flexibility in choosing a power supply for the system.

The Voltage Regulator regulates from 5.5 to 2.7 V and can serve as an input to the LDO. This allows the device to be powered from up to a 5.5 V supply without any external components other than bypass capacitors.

### 4.1.2. Voltage Supply Monitor (VMON0)

The SiM3C1xx devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware. The supply monitor includes additional circuitry that can monitor the main supply voltage and the VREGIN input voltage divided by 4 (VREGIN / 4).

The supply monitor module includes the following features:

- Main supply “VDD Low” (VDD below the early warning threshold) notification.
- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.
- VREGIN divided by 4 (VREGIN / 4) supply “VREGIN Low” notification.

### 4.1.3. External Regulator (EXTVREG0)

The External Regulator provides all the circuitry needed for a high-power regulator except the power transistor (NPN or PNP) and current sensing resistor (if current limiting is enabled).

The External Regulator module has the following features:

- Interfaces with either an NPN or PNP external transistor that serves as the pass device for the high current regulator.
- Automatic current limiting.
- Automatic foldback limiting.
- Sources up to 1 A for use by external circuitry.
- Variable output voltage from 1.8–3.6 V in 100 mV steps.

### 4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3C1xx manages the power systems of the device. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins. It also recognizes and manages the various wake sources for low-power modes of the device.

The PMU module includes the following features:

- Up to 16 pin wake inputs can wake the device from Power Mode 9.
- The Low Power Timer, RTC0 (alarms and oscillator fail), Comparator 0, and the $\overline{\text{RESET}}$ pin can also serve as wake sources for Power Mode 9.
- All PM9 wake sources (except for the $\overline{\text{RESET}}$ pin) can also reset the Low Power Timer or RTC0 modules.
- Disables the level shifters to pins and peripherals to further reduce power usage in PM9. These level shifters must be re-enabed by firmware after exiting PM9.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM9.

### 4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Five output ranges with output frequencies ranging from 23 to 80 MHz.
- Multiple reference frequency inputs.
- Three output modes: free-running DCO, frequency-locked, and phase-locked.
- Ability to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.
- Ability to suspend all output frequency updates (including dithering and spectrum spreading) using the STALL bit during jitter-sensitive operations.

### 4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3C1xx devices and enables or disables automatically, as needed.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

### 4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC0) provides a low power internal clock source running at approximately 16.4 kHz for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator

### 4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, RC, C, or CMOS oscillators.
- Support external CMOS frequencies from 10 kHz to 50 MHz and external crystal frequencies from 10 kHz to 30 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

## 4.6. Communications Peripherals

### 4.6.1. External Memory Interface (EMIF0)

The External Memory Interface (EMIF0) allows external parallel asynchronous devices, like SRAMs and LCD controllers, to appear as part of the system memory map. The EMIF0 module includes the following features:

- Provides a memory mapped view of multiple external devices.
- Support for byte, half-word and word accesses regardless of external device data-width.
- Error indicator for certain invalid transfers.
- Minimum external timing allows for 3 clocks per write or 4 clocks per read.
- Output bus can be shared between non-muxed and muxed devices.
- Available extended address output allows for up to 24-bit address with 8-bit parallel devices.
- Support for 8-bit and 16-bit (muxed-mode only) devices with up to two chip-select signals.
- Support for internally muxed devices with dynamic address shifting.
- Fully programmable control signal waveforms.

### 4.6.2. USART (USART0, USART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device. In addition to these signals, the USART0 module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

### 4.6.3. UART (UART0, UART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device.

The UART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud-rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX) or 1 Mbaud Smartcard (TX or RX).

- Spike suppression up to 2 times the APB period.

### 4.6.6. $I^2S$ (I2S0)

The $I^2S$ module receives digital data from an external source over a data line in the standard $I^2S$, left-justified, right-justified, or time domain multiplexing format, de-serializes the data, and generates requests to transfer the data using the DMA. The module also reads stereo audio samples from the DMA, serializes the data, and sends it out of the chip on a data line in the same standard serial format for digital audio. The $I^2S$ receive interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync), and SD (data input). The block’s transmit interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync) and SD (data output).

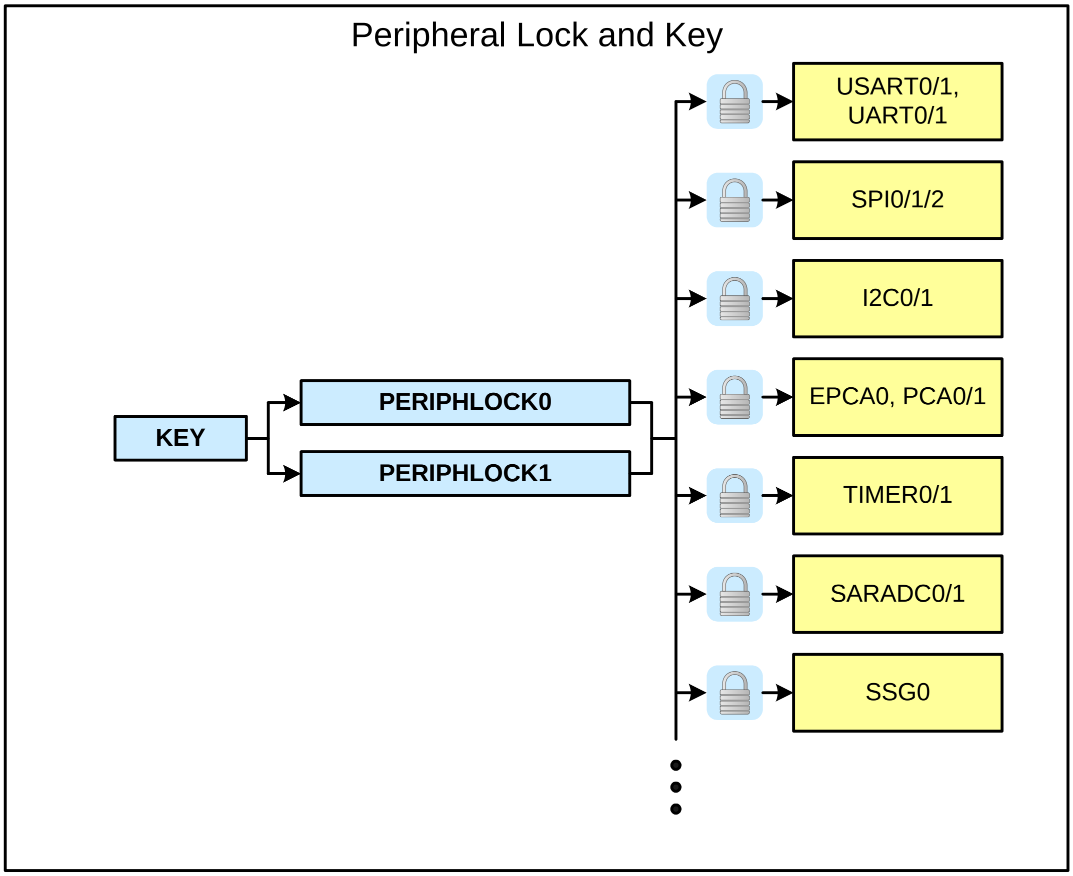
The $I^2S$ module includes the following features:

- Master or slave capability.
- Flexible 10-bit clock divider with 8-bit fractional clock divider provides support for various common sampling frequencies (16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz) for up to two 32-bit channels.
- Support for DMA data transfers.
- Support for various data formats.
- Time Division Multiplexing

## 4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.




## 4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabiites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.

# 5. Ordering Information

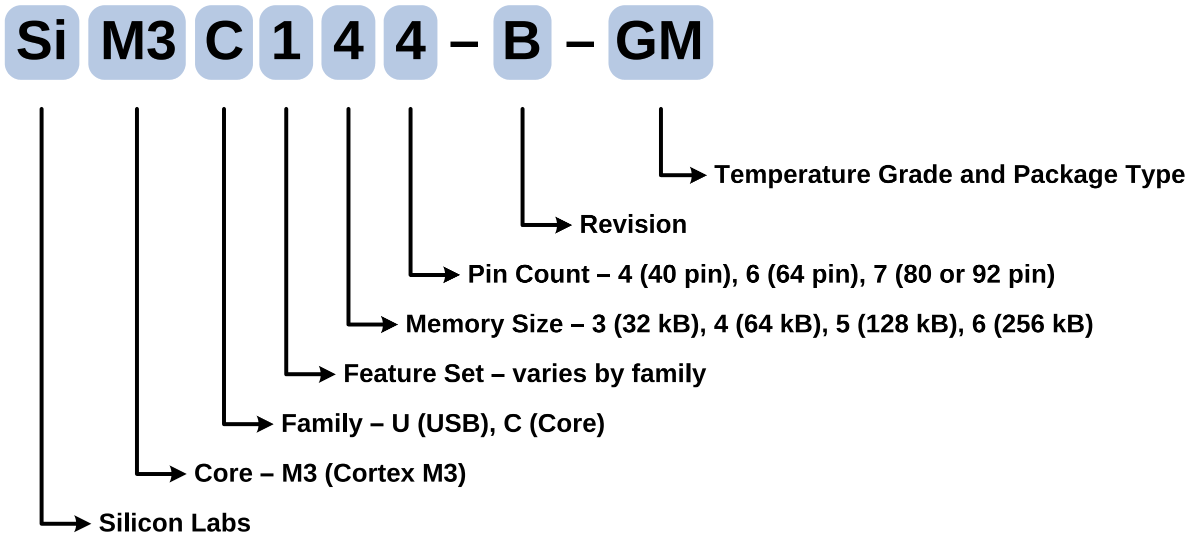



**Figure 5.1. SiM3C1xx Part Numbering**

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I$^2$S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

**Table 6.1. Pin Definitions and alternate functions for SiM3C1x7**

| Pin Name | Type | Pin Numbers TQFP-80 | Pin Numbers LGA-92 | Crossbar Capability (see Port Config Section) | Port Match | External Memory Interface (m = muxed mode) | Port-Mapped Level Shifter | Output Toggle Logic | External Trigger Inputs | Analog or Additional Functions |
|---|---|---|---|---|---|---|---|---|---|---|
| VSS | Ground | 33<br>75 | B15<br>B34 | | | | | | | |
| VDD | Power (Core) | 74 | A44 | | | | | | | |
| VIO | Power (I/O) | 32<br>49<br>73 | A19<br>A29<br>A43 | | | | | | | |
| VREGIN | Power (Regulator) | 76 | A45 | | | | | | | |
| VSSHD | Ground (High Drive) | 4 | B2 | | | | | | | |
| VIOHD | Power (High Drive) | 5 | A3 | | | | | | | |
| $\overline{\text{RESET}}$ | Active-low Reset | 80 | A48 | | | | | | | |
| SWCLK/TCK | Serial Wire/JTAG | 45 | B20 | | | | | | | |
| SWDIO/TMS | Serial Wire/JTAG | 44 | A27 | | | | | | | |
| PB0.0 | Standard I/O | 72 | B33 | XBR0 | ✓ | | | | | ADC0.0 |
| PB0.1 | Standard I/O | 71 | B32 | XBR0 | ✓ | | | | | ADC0.1<br>CS0.0 |
| PB0.2 | Standard I/O | 70 | A42 | XBR0 | ✓ | | | | | ADC0.2<br>CS0.1 |
| PB0.3 | Standard I/O | 69 | B31 | XBR0 | ✓ | | | | | ADC0.3<br>CS0.2 |
| PB0.4 | Standard I/O | 68 | A41 | XBR0 | ✓ | | | | | ADC0.4<br>CS0.3 |
| PB0.5 | Standard I/O | 67 | B30 | XBR0 | ✓ | | | | | ADC0.5<br>CS0.4 |
| PB0.6 | Standard I/O | 66 | A40 | XBR0 | ✓ | | | | | CS0.5 |
| PB0.7 | Standard I/O | 65 | B29 | XBR0 | ✓ | | | | | ADC0.6<br>CS0.6<br>IVC0.0 |

**Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)**

| Pin Name | Type | Pin Numbers TQFP-80 | Pin Numbers LGA-92 | Crossbar Capability (see Port Config Section) | Port Match | External Memory Interface (m = muxed mode) | Port-Mapped Level Shifter | Output Toggle Logic | External Trigger Inputs | Analog or Additional Functions |
|---|---|---|---|---|---|---|---|---|---|---|
| PB3.4 | 5 V Tolerant I/O | 16 | A9 | XBR1 | ✓ | $\overline{\text{OE}}$ | | | INT0.9<br>INT1.9<br>WAKE.8 | CMP0P.4<br>CMP1P.4 |
| PB3.5 | 5 V Tolerant I/O | 15 | B7 | XBR1 | ✓ | ALEm | | | DAC0T2<br>DAC1T2<br>INT0.10<br>INT1.10<br>WAKE.9 | CMP0N.4<br>CMP1N.4 |
| PB3.6 | 5 V Tolerant I/O | 14 | A8 | XBR1 | ✓ | CS0 | | | DAC0T3<br>DAC1T3<br>INT0.11<br>INT1.11<br>WAKE.10 | CMP0P.5<br>CMP1P.5 |
| PB3.7 | 5 V Tolerant I/O | 13 | B6 | XBR1 | ✓ | $\overline{\text{BE1}}$ | | | DAC0T4<br>DAC1T4<br>LPT0T1<br>INT0.12<br>INT1.12<br>WAKE.11 | CMP0N.5<br>CMP1N.5 |
| PB3.8 | 5 V Tolerant I/O | 12 | A7 | XBR1 | ✓ | CS1 | | | DAC0T5<br>DAC1T5<br>LPT0T2<br>INT0.13<br>INT1.13<br>WAKE.12 | CMP0P.6<br>CMP1P.6<br>EXREGSP |
| PB3.9 | 5 V Tolerant I/O | 11 | B5 | XBR1 | ✓ | $\overline{\text{BE0}}$ | | | DAC0T6<br>DAC1T6<br>INT0.14<br>INT1.14<br>WAKE.13 | CMP0N.6<br>CMP1N.6<br>EXREGSN |
| PB3.10 | 5 V Tolerant I/O | 10 | B4 | XBR1 | ✓ | | | | INT0.15<br>INT1.15<br>WAKE.14 | CMP0P.7<br>CMP1P.7<br>EXREGOUT |
| PB3.11 | 5 V Tolerant I/O | 9 | B3 | XBR1 | ✓ | | | | WAKE.15 | CMP0N.7<br>CMP1N.7<br>EXREGBD |

**Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)**

| Pin Name | Type | Pin Numbers | Crossbar Capability (see Port Config Section) | Port Match | External Memory Interface (m = muxed mode) | Port-Mapped Level Shifter | Output Toggle Logic | External Trigger Inputs | Analog or Additional Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB3.2 | 5 V Tolerant I/O | 14 | XBR1 | ✓ | AD0m/ D0 | | | DAC0T0 DAC1T0 LPT0T0 WAKE.8 | CMP0P.2 CMP1P.2 |
| PB3.3 | 5 V Tolerant I/O | 13 | XBR1 | ✓ | $\overline{\text{WR}}$ | | | DAC0T1 DAC1T1 INT0.4 INT1.4 WAKE.9 | CMP0N.2 CMP1N.2 |
| PB3.4 | 5 V Tolerant I/O | 12 | XBR1 | ✓ | $\overline{\text{OE}}$ | | | INT0.5 INT1.5 WAKE.10 | CMP0P.3 CMP1P.3 |
| PB3.5 | 5 V Tolerant I/O | 11 | XBR1 | ✓ | ALEm | | | DAC0T2 DAC1T2 INT0.6 INT1.6 WAKE.11 | CMP0N.3 CMP1N.3 |
| PB3.6 | 5 V Tolerant I/O | 10 | XBR1 | ✓ | CS0 | | | DAC0T3 DAC1T3 INT0.7 INT1.7 WAKE.12 | CMP0P.4 CMP1P.4 EXREGSP |
| PB3.7 | 5 V Tolerant I/O | 9 | XBR1 | ✓ | $\overline{\text{BE1}}$ | | | DAC0T4 DAC1T4 INT0.8 INT1.8 WAKE.13 | CMP0N.4 CMP1N.4 EXREGSN |
| PB3.8 | 5 V Tolerant I/O | 8 | XBR1 | ✓ | CS1 | | | DAC0T5 DAC1T5 LPT0T1 INT0.9 INT1.9 WAKE.14 | CMP0P.5 CMP1P.5 EXREGOUT |

### 6.3. SiM3C1x4 Pin Definitions

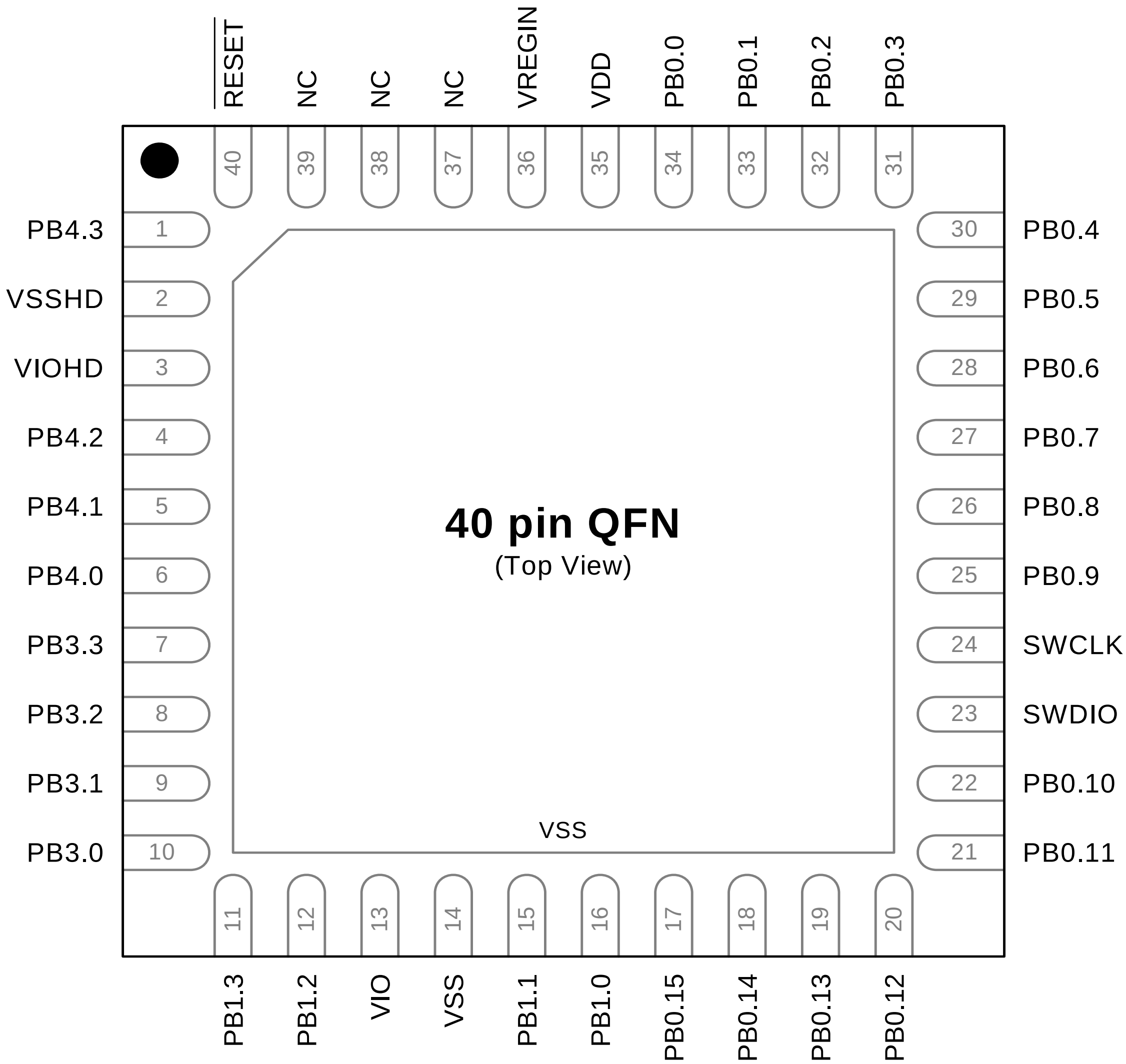



**Figure 6.5. SiM3C1x4-GM Pinout**

### 6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

### 6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

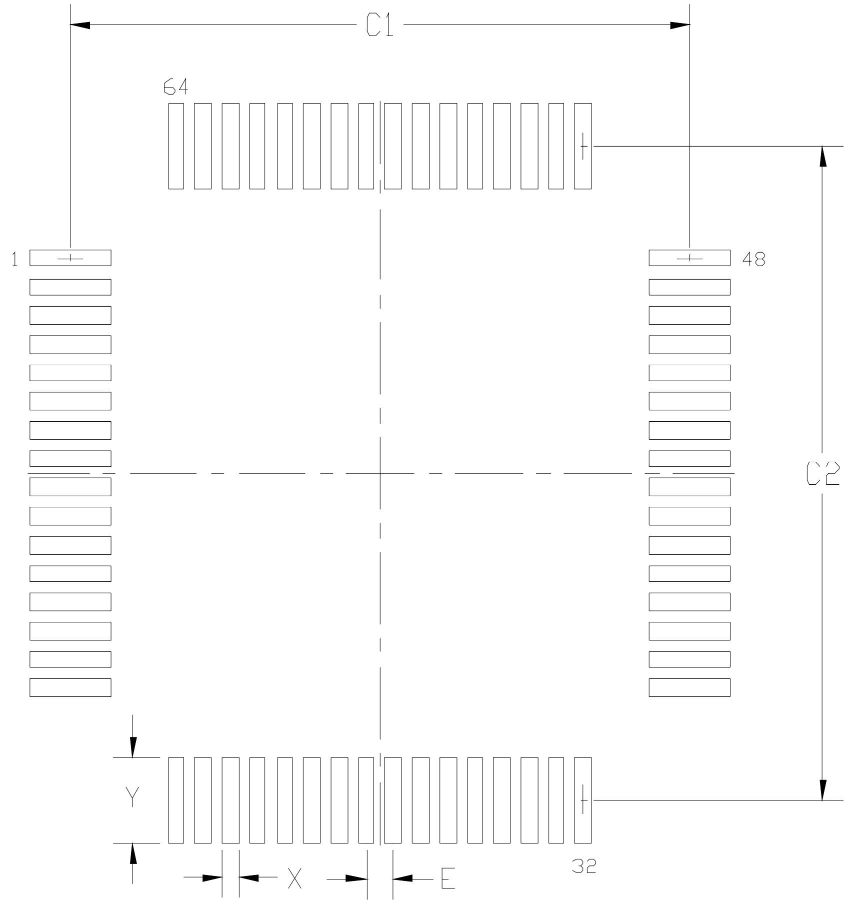



**Figure 6.13. TQFP-64 Landing Diagram**

**Table 6.11. TQFP-64 Landing Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| **C1** | 11.30 | 11.40 |
| **C2** | 11.30 | 11.40 |
| **E** | 0.50 BSC | |
| **X** | 0.20 | 0.30 |
| **Y** | 1.40 | 1.50 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

## 6.8. QFN-40 Package Specifications

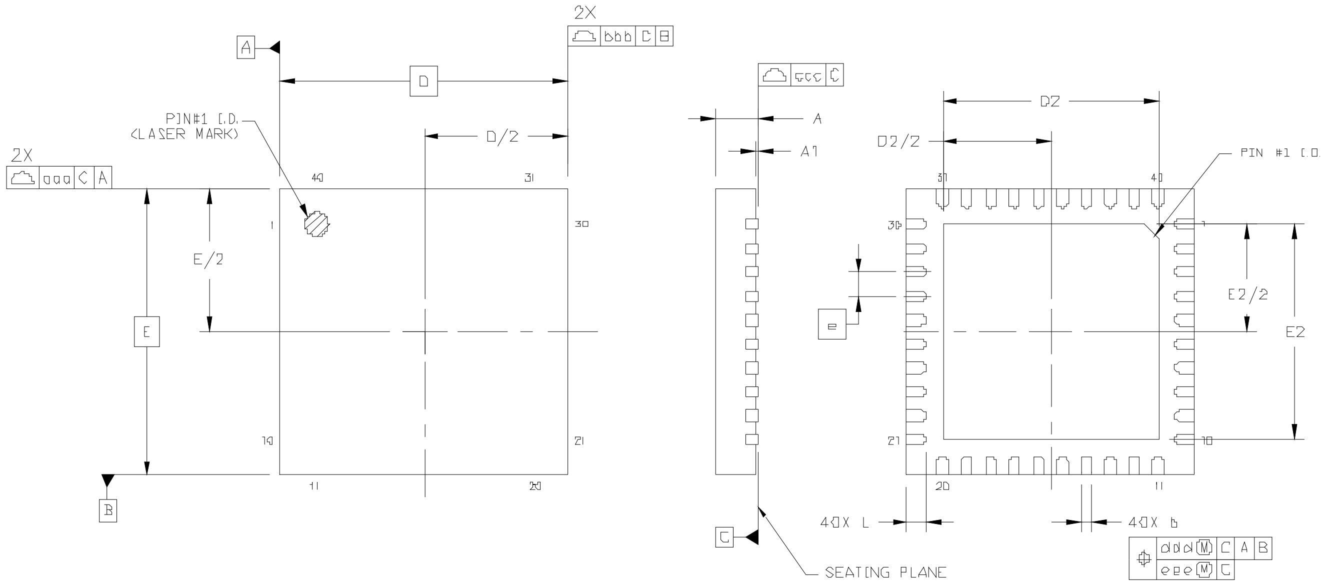



Figure 6.14. QFN-40 Package Drawing

Table 6.12. QFN-40 Package Dimensions

| Dimension | Min | Nominal | Max |
|---|---|---|---|
| **A** | 0.80 | 0.85 | 0.90 |
| **A1** | 0.00 | 0.02 | 0.05 |
| **b** | 0.18 | 0.25 | 0.30 |
| **D** | | 6.00 BSC | |
| **D2** | 4.35 | 4.50 | 4.65 |
| **e** | | 0.50 BSC | |
| **E** | | 6.00 BSC | |
| **E2** | 4.35 | 4.5 | 4.65 |
| **L** | 0.30 | 0.40 | 0.50 |
| **aaa** | | 0.10 | |
| **bbb** | | 0.10 | |
| **ccc** | | 0.08 | |
| **ddd** | | 0.10 | |
| **eee** | | 0.05 | |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

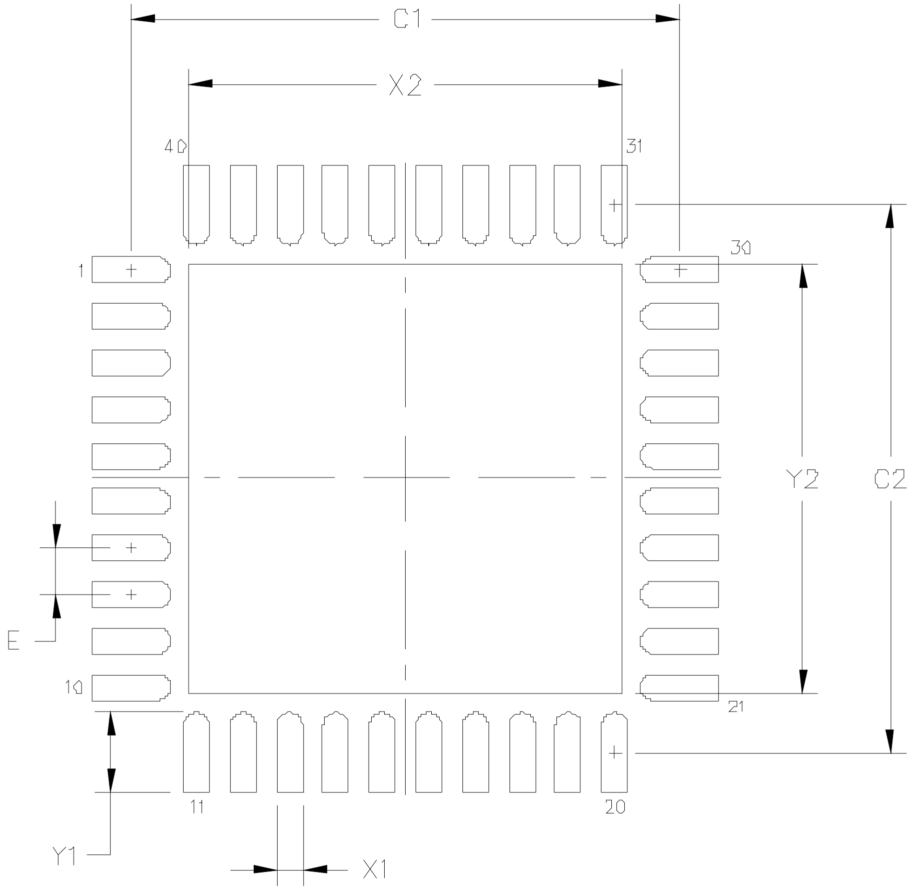



Figure 6.15. QFN-40 Landing Diagram

Table 6.13. QFN-40 Landing Diagram Dimensions

| Dimension | mm |
|---|---|
| **C1** | 5.90 |
| **C2** | 5.90 |
| **E** | 0.50 |
| **X1** | 0.30 |
| **Y1** | 0.85 |
| **X2** | 4.65 |
| **Y2** | 4.65 |

**Notes:**
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.