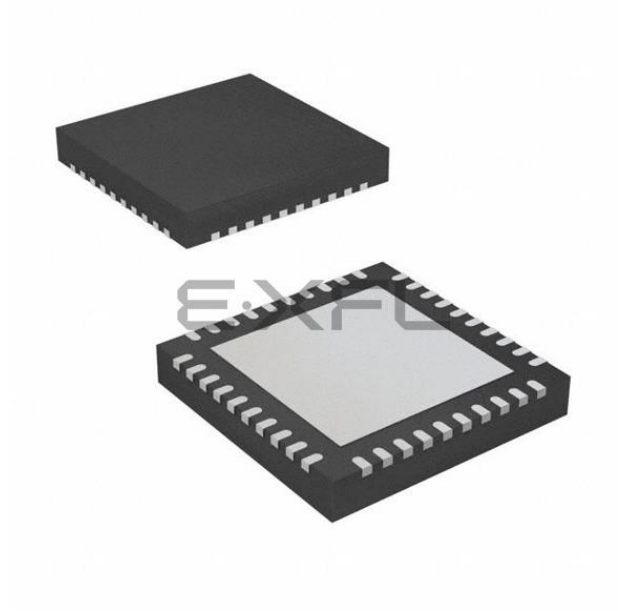

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Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u134-b-gmr

Table of Contents

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	33	36.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	10.5	13.3	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	2.0	3.8	mA
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	22	24.9	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	10	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.2	3	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	30.5	35.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	8.5	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.7	—	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	20	23	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	5.3	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.0	—	mA
Power Mode 2[2,3,4]—Core halted with peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	19	22	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.3	—	mA
Power Mode 3[2,3]	I_{DD}	V_{DD} = 1.8 V, T_A = 25 °C	—	175	—	µA
		V_{DD} = 3.0 V, T_A = 25 °C	—	250	—	µA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Peripheral Supply Currents						
Voltage Regulator (VREG0)	I_{VREGIN}	Normal Mode, T_A = 25 °C BGDIS = 0, SUSEN = 0	—	300	—	µA
		Normal Mode, T_A = 85 °C BGDIS = 0, SUSEN = 0	—	—	650	µA
		Suspend Mode, T_A = 25 °C BGDIS = 0, SUSEN = 1	—	75	—	µA
		Suspend Mode, T_A = 85 °C BGDIS = 0, SUSEN = 1	—	—	115	µA
		Sleep Mode, T_A = 25 °C BGDIS = 1, SUSEN = X	—	90	—	nA
		Sleep Mode, T_A = 85 °C BGDIS = 1, SUSEN = X	—	—	500	nA
Voltage Regulator (VREG0) Sense	$I_{VRSENSE}$	SENSEEN = 1	—	3	—	µA
External Regulator (EXTVREG0)	$I_{EXTVREG}$	Regulator	—	215	250	µA
		Current Sensor	—	7	—	µA
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 80 MHz	—	1.75	1.86	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	190	—	µA
		Operating at 2.5 MHz	—	40	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz, T_A = 25 °C	—	215	—	nA
		Operating at 16.4 kHz, T_A = 85 °C	—	—	500	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.15. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	760	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	±14	—	mV
Slope	M		—	2.8	—	mV/°C
Slope Error*	E_M		—	±120	—	µV/°C
Linearity			—	1	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

Table 3.19. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Voltage on I/O pins, Port Bank 3 I/O	V_{IN}	SiM3C1x7, PB3.0–PB3.7, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		SiM3C1x7, PB3.0–PB3.7, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		SiM3C1x7, PB3.8 - PB3.11	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
		SiM3C1x6, PB3.0–PB3.5, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		SiM3C1x6, PB3.0–PB3.5, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		SiM3C1x6, PB3.6–PB3.9	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
		SiM3C1x4, PB3.0–PB3.3	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
Total Current Sunk into Supply Pins	I_{SUPP}	V_{DD}, V_{REGIN}, V_{IO}, V_{IOHD}	—	400	mA
Total Current Sourced out of Ground Pins	I_{VSS}	V_{SS}, V_{SSHD}	400	—	mA
Current Sourced or Sunk by Any I/O Pin	I_{PIO}	PB0, PB1, PB2, PB3, and $\overline{\text{RESET}}$	–100	100	mA
		PB4	–300	300	mA
Current Injected on Any I/O Pin	I_{INJ}	PB0, PB1, PB2, PB3, and $\overline{\text{RESET}}$	–100	100	mA
		PB4	–300	300	mA
Total Injected Current on I/O Pins	ΣI_{INJ}	Sum of all I/O and $\overline{\text{RESET}}$	–400	400	mA

***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.

4.1. Power

4.1.1. LDO and Voltage Regulator (VREG0)

The SiM3C1xx devices include two internal regulators: the core LDO Regulator and the Voltage Regulator (VREG0).

The LDO Regulator converts a 1.8–3.6 V supply to the core operating voltage of 1.8 V. This LDO consumes little power and provides flexibility in choosing a power supply for the system.

The Voltage Regulator regulates from 5.5 to 2.7 V and can serve as an input to the LDO. This allows the device to be powered from up to a 5.5 V supply without any external components other than bypass capacitors.

4.1.2. Voltage Supply Monitor (VMON0)

The SiM3C1xx devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware. The supply monitor includes additional circuitry that can monitor the main supply voltage and the VREGIN input voltage divided by 4 (VREGIN / 4).

The supply monitor module includes the following features:

- Main supply “VDD Low” (VDD below the early warning threshold) notification.
- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.
- VREGIN divided by 4 (VREGIN / 4) supply “VREGIN Low” notification.

4.1.3. External Regulator (EXTVREG0)

The External Regulator provides all the circuitry needed for a high-power regulator except the power transistor (NPN or PNP) and current sensing resistor (if current limiting is enabled).

The External Regulator module has the following features:

- Interfaces with either an NPN or PNP external transistor that serves as the pass device for the high current regulator.
- Automatic current limiting.
- Automatic foldback limiting.
- Sources up to 1 A for use by external circuitry.
- Variable output voltage from 1.8–3.6 V in 100 mV steps.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3C1xx manages the power systems of the device. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins. It also recognizes and manages the various wake sources for low-power modes of the device.

The PMU module includes the following features:

- Up to 16 pin wake inputs can wake the device from Power Mode 9.
- The Low Power Timer, RTC0 (alarms and oscillator fail), Comparator 0, and the $\overline{\text{RESET}}$ pin can also serve as wake sources for Power Mode 9.
- All PM9 wake sources (except for the $\overline{\text{RESET}}$ pin) can also reset the Low Power Timer or RTC0 modules.
- Disables the level shifters to pins and peripherals to further reduce power usage in PM9. These level shifters must be re-enabed by firmware after exiting PM9.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM9.

4.2. I/O

4.2.1. General Features

The SiM3C1xx ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB2 only) to generate simple square waves.
- A subset of pins can also serve as inputs to the Port Mapped Level Shifters available on the High Drive Pins.

4.2.2. High Drive Pins (PB4)

The High Drive pins have the following additional features:

- Programmable safe state: high, low, or high impedance.
- Programmable drive strength and slew rates.
- Programmable hardware current limiting.
- Powered from a separate source (VIOHD, which can be up to 6 V) from the rest of the device.
- Supports various functions, including GPIO, UART1 pins, EPCA0 pins, or Port Mapped Level Shifting.

4.2.3. 5 V Tolerant Pins (PB3)

The 5 V tolerant pins can be connected to external circuitry operating at voltages above the device supply without needing extra components to shift the voltage level.

4.2.4. Crossbars

The SiM3C1xx devices have two Crossbars with the following features:

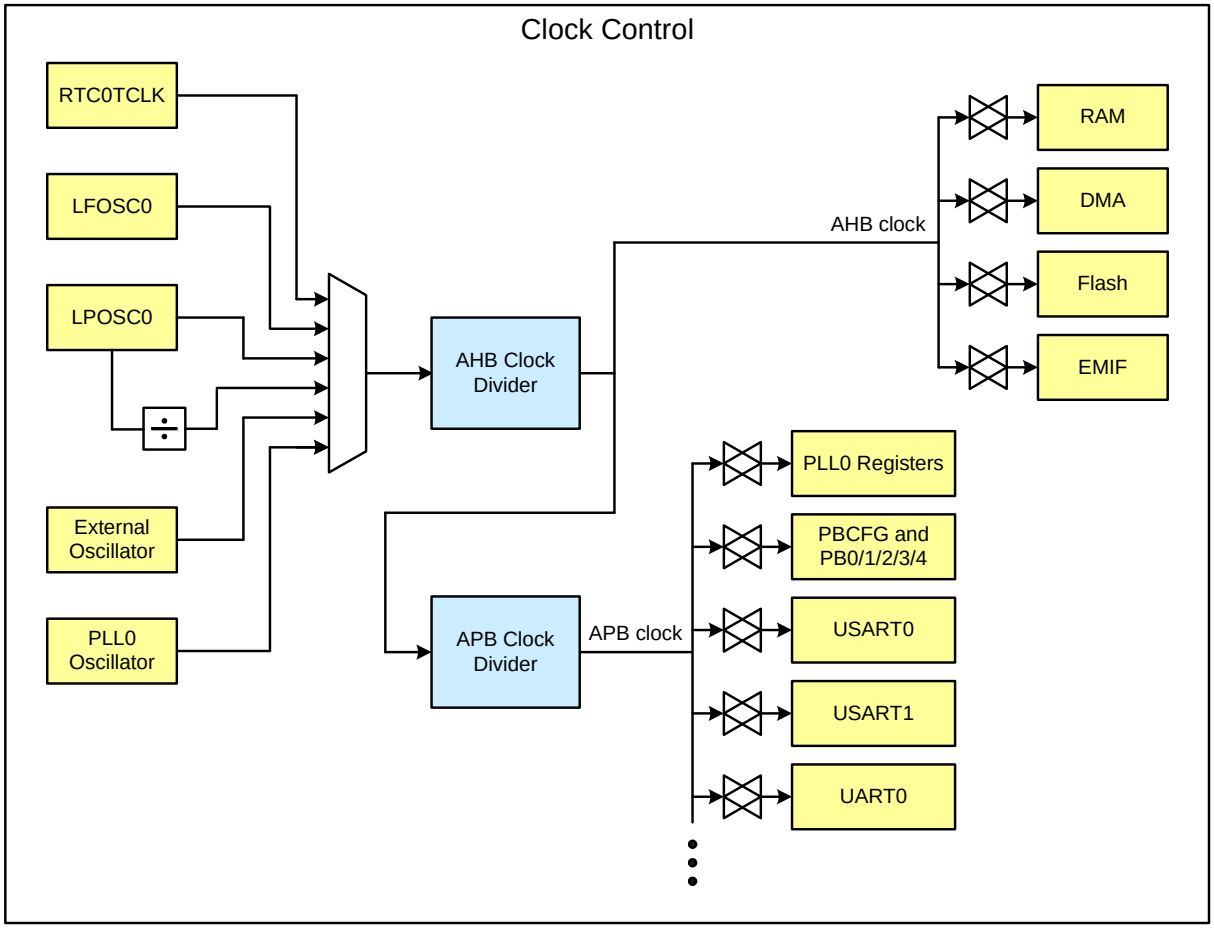
- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The Crossbars have a fixed priority for each I/O function and assign these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the Crossbars skip that pin when assigning the next selected resource. Additionally, the Crossbars will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.



4.5.3. Real-Time Clock (RTC0)

The RTC0 module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC0 provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3C1xx devices.

The RTC0 module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC0 output can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal low frequency oscillator (LFOSC0), an external 32.768 kHz crystal (no additional resistors or capacitors necessary), or with an external CMOS clock.
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- Operates directly from VDD and remains operational even when the device goes into its lowest power down mode.
- The RTC timer clock (RTC0TCLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.

4.5.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER0) module runs from the clock selected by the RTC0 module, allowing the LPTIMER0 to operate even if the AHB and APB clocks are disabled. The LPTIMER0 counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on a low-frequency clock (RTC0TCLK)
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection, which can generate an interrupt, reset the timer, or wake some devices from low power modes.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.

4.5.5. Watchdog Timer (WDTIMER0)

The WDTIMER0 module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

4.8. Reset Sources

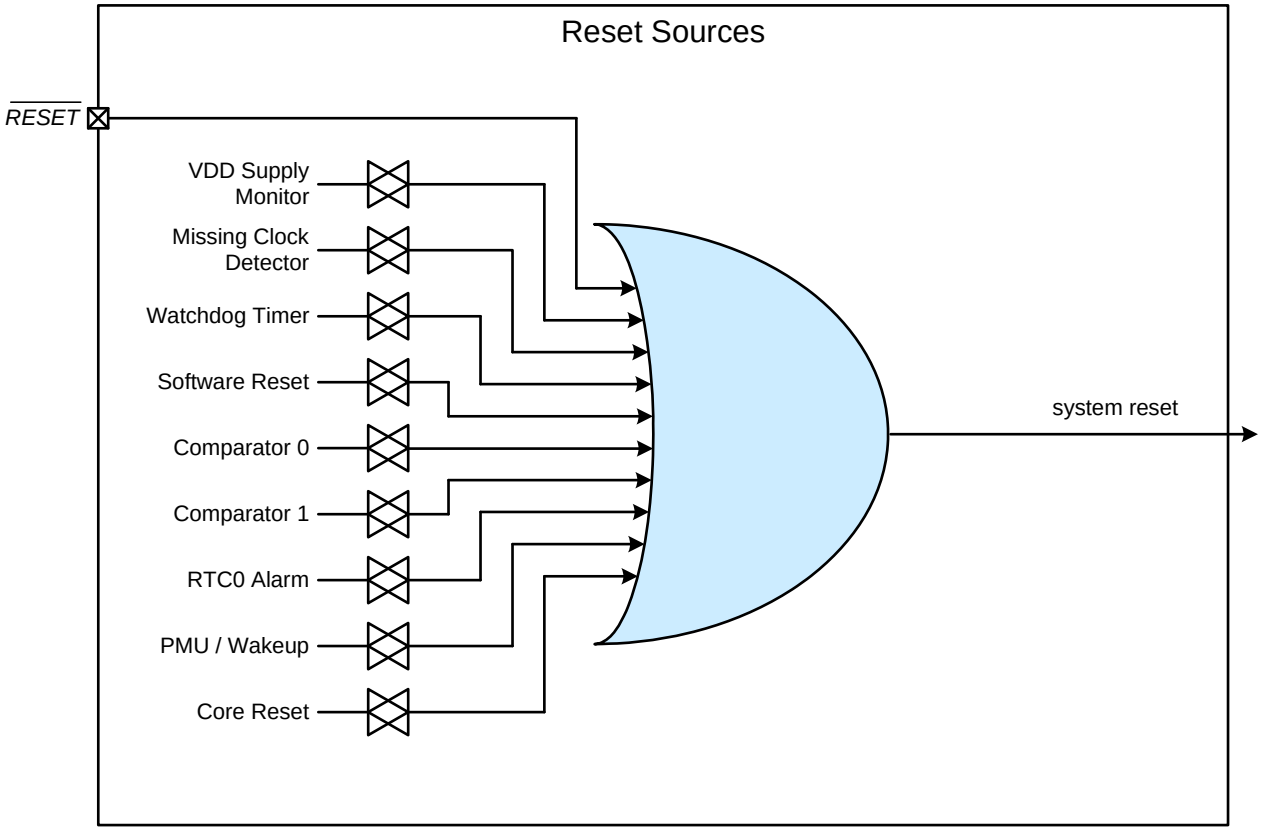
Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

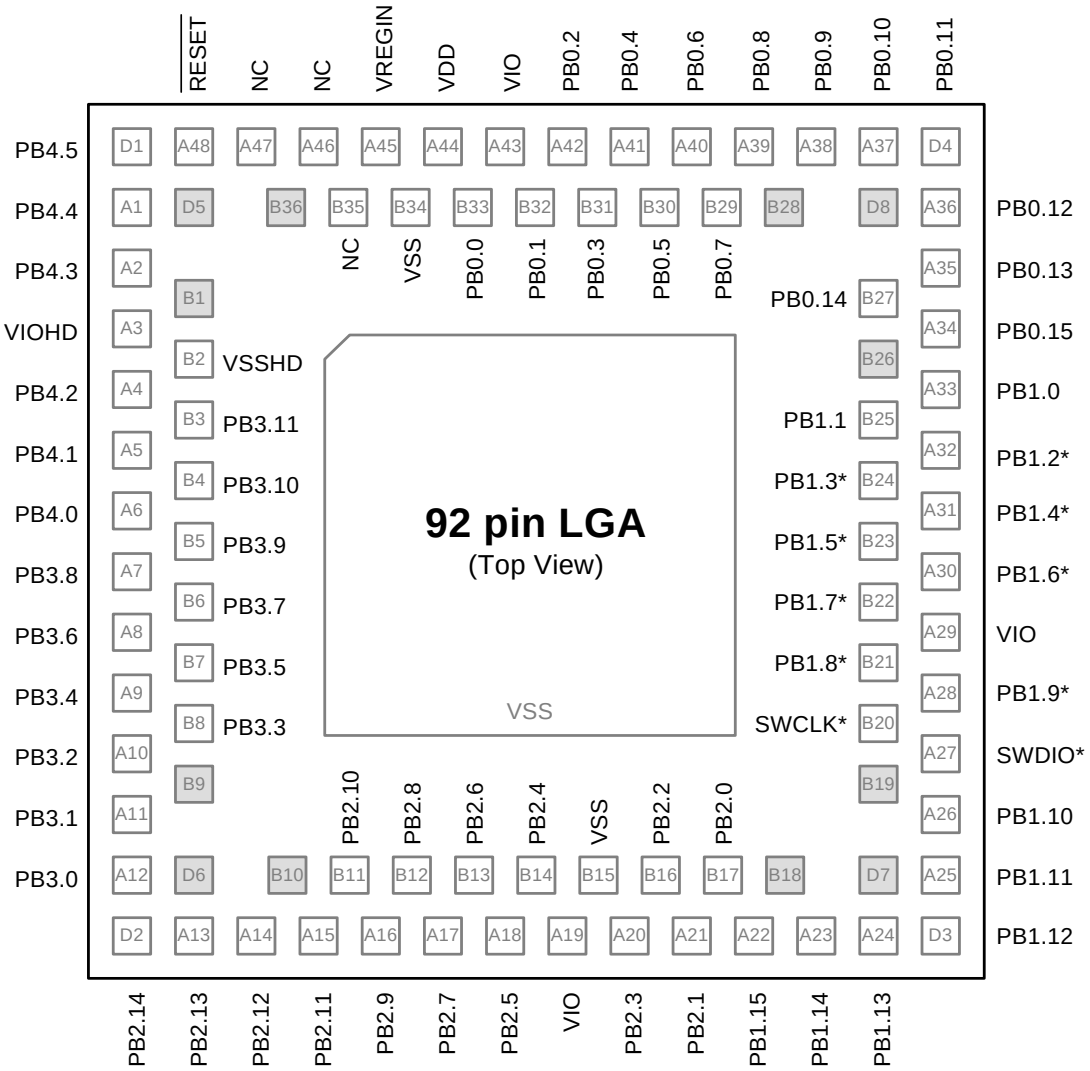
- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.
- Clocks to all AHB peripherals are enabled.
- Clocks to all APB peripherals other than Watchdog Timer, EMIF0, and DMAXBAR are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VDD Supply Monitor and power-on resets, the $\overline{\text{RESET}}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled with the Low Frequency Oscillator (LFO0) as its clock source. Program execution begins at location 0x00000000.





*Noted pins are listed in the pinout table and 80-pin TQFP package figure with additional names. These alternate functions are also present on the 92-pin LGA package and are identical to those on the 80-pin TQFP package.

Figure 6.2. SiM3C1x7-GM Pinout

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	64	A39	XBR0	✓					ADC0.7 CS0.7 IVC0.1
PB0.9	Standard I/O	63	A38	XBR0	✓					ADC0.8 RTC1
PB0.10	Standard I/O	62	A37	XBR0	✓					RTC2
PB0.11	Standard I/O	61	D4	XBR0	✓					ADC0.9 VREFGND
PB0.12	Standard I/O	60	A36	XBR0	✓					ADC0.10 VREF
PB0.13	Standard I/O	59	A35	XBR0	✓					IDAC0
PB0.14	Standard I/O	58	B27	XBR0	✓					IDAC1
PB0.15	Standard I/O	57	A34	XBR0	✓					XTAL1
PB1.0	Standard I/O	56	A33	XBR0	✓					XTAL2
PB1.1	Standard I/O	55	B25	XBR0	✓					ADC0.11
PB1.2/TRST	Standard I/O /JTAG	54	A32	XBR0	✓					
PB1.3/TDO/ SWV	Standard I/O /JTAG/ Serial Wire Viewer	53	B24	XBR0	✓					ADC0.12 ADC1.12
PB1.4/TDI	Standard I/O /JTAG	52	A31	XBR0	✓					ADC0.13 ADC1.13
PB1.5/ETM0	Standard I/O /ETM	51	B23	XBR0	✓					ADC0.14 ADC1.14
PB1.6/ETM1	Standard I/O /ETM	50	A30	XBR0	✓					ADC0.15 ADC1.15
PB1.7/ETM2	Standard I/O /ETM	48	B22	XBR0	✓					ADC1.11 CS0.8
PB1.8/ETM3	Standard I/O /ETM	47	B21	XBR0	✓					ADC1.10 CS0.9

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB2.6	Standard I/O	29	B13	XBR1	✓	AD11m/ A3		Yes	INT0.6 INT1.6	
PB2.7	Standard I/O	28	A17	XBR1	✓	AD10m/ A2		Yes	INT0.7 INT1.7	
PB2.8	Standard I/O	27	B12	XBR1	✓	AD9m/ A1		Yes		
PB2.9	Standard I/O	26	A16	XBR1	✓	AD8m/ A0		Yes		
PB2.10	Standard I/O	25	B11	XBR1	✓	AD7m/ D7		Yes		
PB2.11	Standard I/O	24	A15	XBR1	✓	AD6m/ D6		Yes		CMP0P.0 CMP1P.0
PB2.12	Standard I/O	23	A14	XBR1	✓	AD5m/ D5		Yes		CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.13	Standard I/O	22	A13	XBR1	✓	AD4m/ D4		Yes		CMP0P.1 CMP1P.1
PB2.14	Standard I/O	21	D2	XBR1	✓	AD3m/ D3		Yes		CMP0N.1 CMP1N.1
PB3.0	5 V Tolerant I/O	20	A12	XBR1	✓	AD2m/ D2				CMP0P.2 CMP1P.2
PB3.1	5 V Tolerant I/O	19	A11	XBR1	✓	AD1m/ D1				CMP0N.2 CMP1N.2
PB3.2	5 V Tolerant I/O	18	A10	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0	CMP0P.3 CMP1P.3
PB3.3	5 V Tolerant I/O	17	B8	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.8 INT1.8	CMP0N.3 CMP1N.3

6.3. SiM3C1x4 Pin Definitions

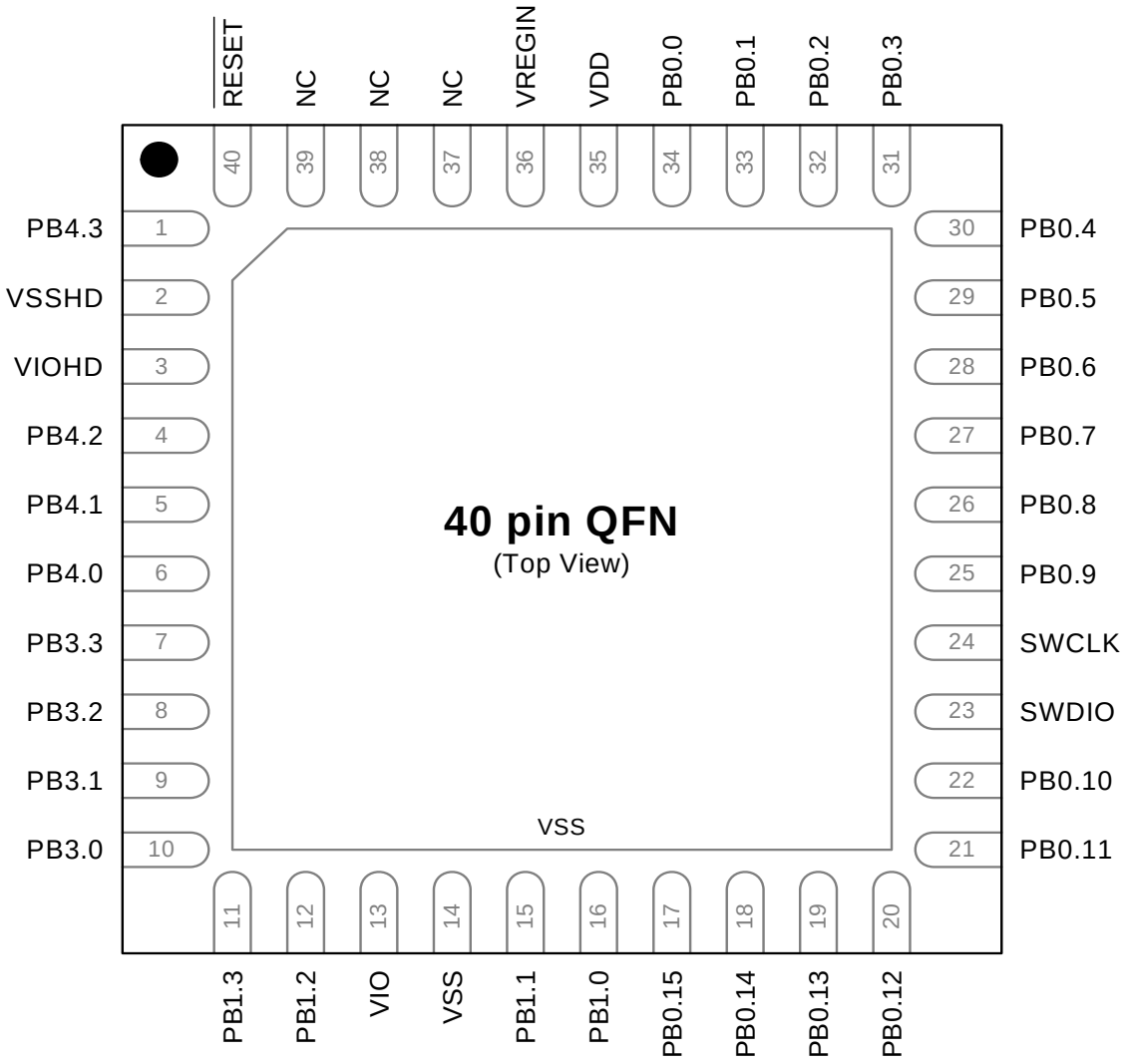


Figure 6.5. SiM3C1x4-GM Pinout

6.4.1. LGA-92 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.4.2. LGA-92 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 2 x 2 array of 1.25 mm square openings on 1.60 mm pitch should be used for the center ground pad.

6.4.3. LGA-92 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

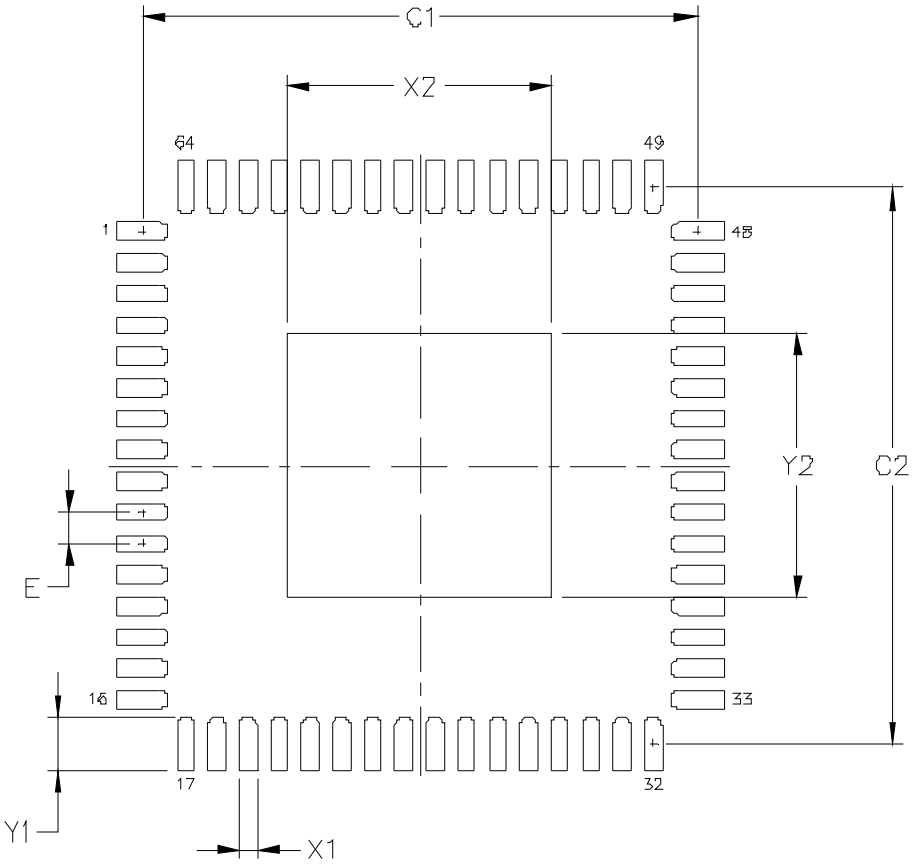


Figure 6.11. QFN-64 Landing Diagram

Table 6.9. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

7. Revision Specific Behavior

This chapter details any known differences from behavior as stated in the device datasheet and reference manual. All known errata for the current silicon revision are rolled into this section at the time of publication. Any errata found after publication of this document will initially be detailed in a separate errata document until this datasheet is revised.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, 7.3, and 7.4 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

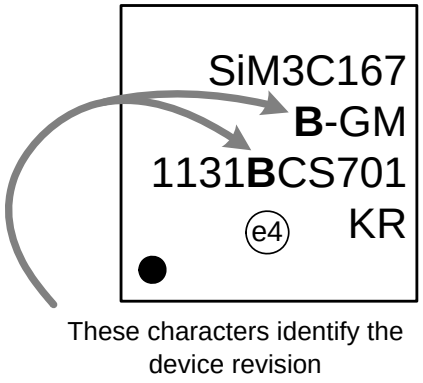


Figure 7.1. LGA-92 SiM3C1x7 Revision Information

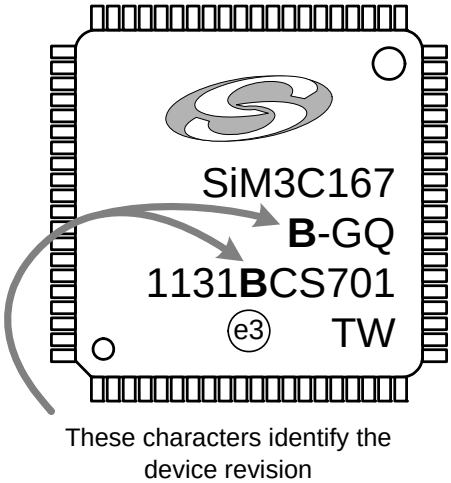


Figure 7.2. TQFP-80 SiM3C1x7 Revision Information