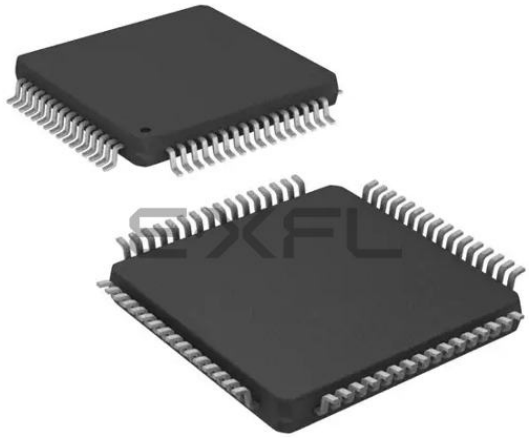

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u136-b-gq

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1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3C1xx device family.

1.1.1. SiM3U1xx/SiM3C1xx Reference Manual

The Silicon Laboratories SiM3U1xx/SiM3C1xx Reference Manual provides detailed functional descriptions for the SiM3C1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3C1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vector Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm.m3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

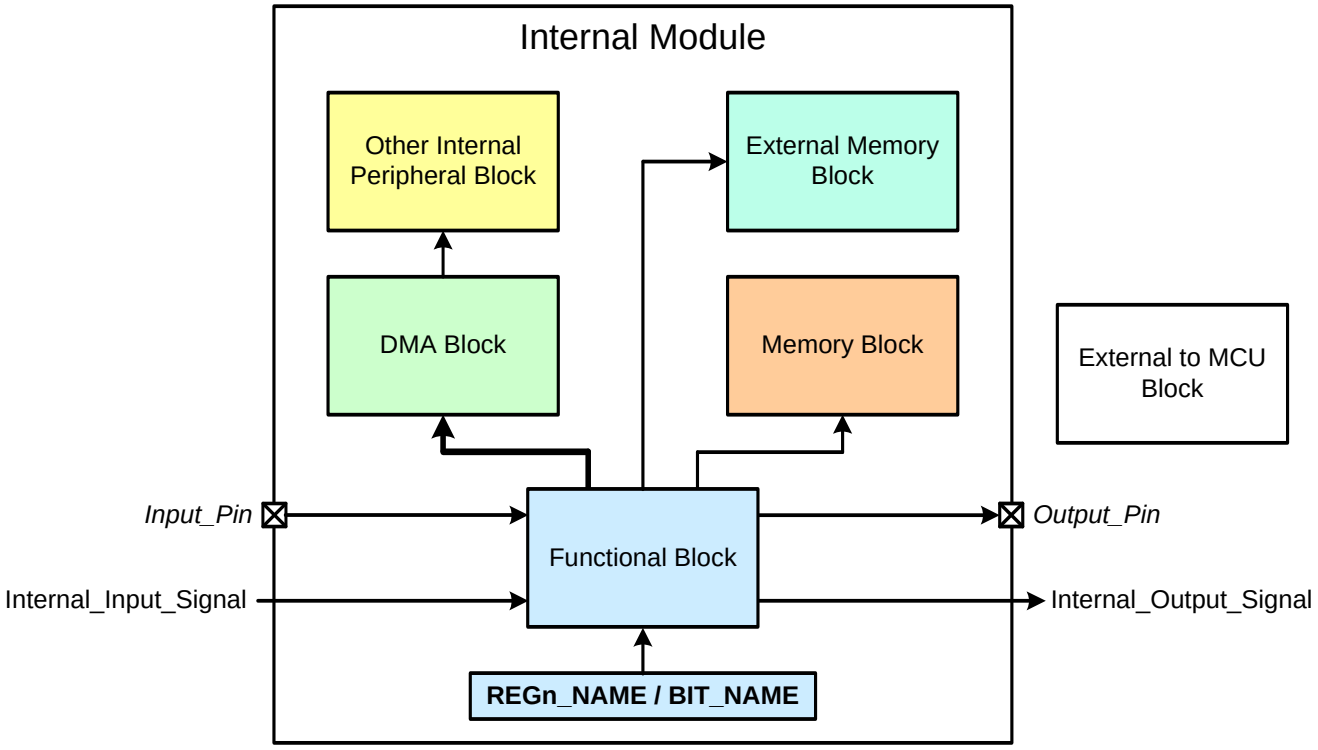

Figure 1.1. Block Diagram Conventions

5. Ordering Information

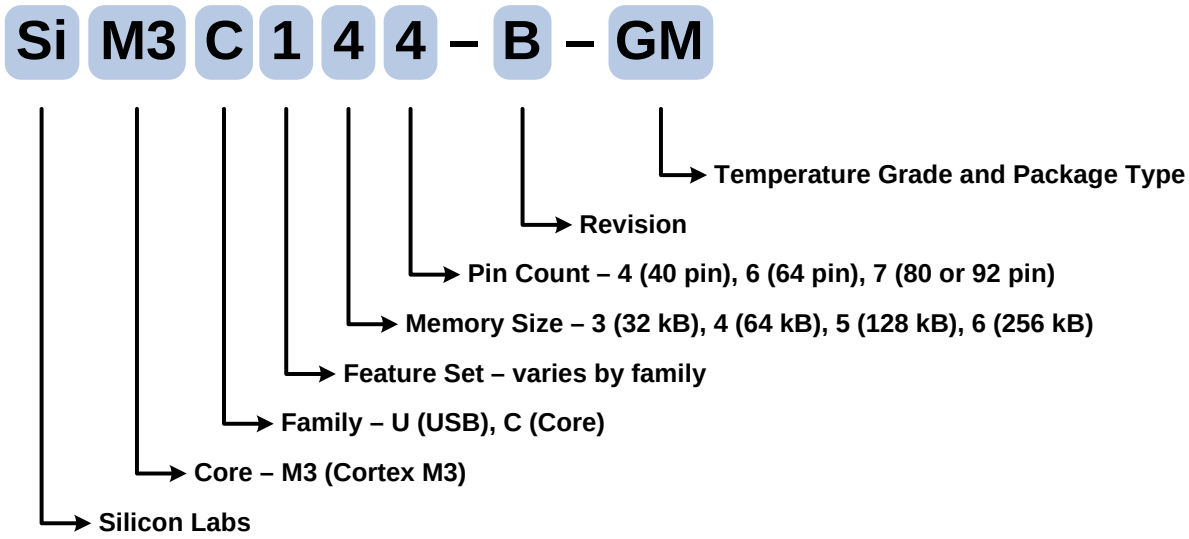

Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I^2S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.2	5 V Tolerant I/O	14	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0 WAKE.8	CMP0P.2 CMP1P.2
PB3.3	5 V Tolerant I/O	13	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.4 INT1.4 WAKE.9	CMP0N.2 CMP1N.2
PB3.4	5 V Tolerant I/O	12	XBR1	✓	$\overline{OE}$			INT0.5 INT1.5 WAKE.10	CMP0P.3 CMP1P.3
PB3.5	5 V Tolerant I/O	11	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.6 INT1.6 WAKE.11	CMP0N.3 CMP1N.3
PB3.6	5 V Tolerant I/O	10	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.7 INT1.7 WAKE.12	CMP0P.4 CMP1P.4 EXREGSP
PB3.7	5 V Tolerant I/O	9	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 INT0.8 INT1.8 WAKE.13	CMP0N.4 CMP1N.4 EXREGSN
PB3.8	5 V Tolerant I/O	8	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T1 INT0.9 INT1.9 WAKE.14	CMP0P.5 CMP1P.5 EXREGOUT

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	14					
VDD	Power (Core)	35					
VIO	Power (I/O)	13					
VREGIN	Power (Regulator)	36					
VSSHD	Ground (High Drive)	2					
VIOHD	Power (High Drive)	3					
$\overline{\text{RESET}}$	Active-low Reset	40					
SWCLK	Serial Wire	24					
SWDIO	Serial Wire	23					
PB0.0	Standard I/O	34	XBR0	✓			ADC0.8 CS0.7 RTC1
PB0.1	Standard I/O	33	XBR0	✓			RTC2
PB0.2	Standard I/O	32	XBR0	✓			ADC0.9 CS0.0 VREFGND
PB0.3	Standard I/O	31	XBR0	✓			ADC0.10 CS0.1 VREF
PB0.4	Standard I/O	30	XBR0	✓			ADC1.6 CS0.2 IDAC0
PB0.5	Standard I/O	29					IDAC1
PB0.6	Standard I/O	28	XBR0	✓			ADC0.0 CS0.3 XTAL1
PB0.7	Standard I/O	27	XBR0	✓			ADC0.1 CS0.4 XTAL2

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.1	5 V Tolerant I/O	9	XBR1	✓		DAC0T1 DAC1T1 LPT0T1 INT0.1 INT1.1 WAKE.13	CMP0N.1 CMP1N.1 EXREGSN
PB3.2	5 V Tolerant I/O	8	XBR1	✓		DAC0T2 DAC1T2 LPT0T2 INT0.2 INT1.3 WAKE.14	CMP0P.2 CMP1P.2 EXREGOUT
PB3.3	5 V Tolerant I/O	7	XBR1	✓		DAC0T3 DAC1T3 INT0.3 INT1.3 WAKE.15	CMP0N.2 CMP1N.2 EXREGBD
PB4.0	High Drive I/O	6					
PB4.1	High Drive I/O	5					
PB4.2	High Drive I/O	4					
PB4.3	High Drive I/O	1					

Table 6.6. TQFP-80 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
L	0.45	0.60	0.75
L1		1.00 Ref	
Θ	0°	3.5°	7°
aaa		0.20	
bbb		0.20	
ccc		0.08	
ddd		0.08	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Revision Specific Behavior

This chapter details any known differences from behavior as stated in the device datasheet and reference manual. All known errata for the current silicon revision are rolled into this section at the time of publication. Any errata found after publication of this document will initially be detailed in a separate errata document until this datasheet is revised.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, 7.3, and 7.4 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

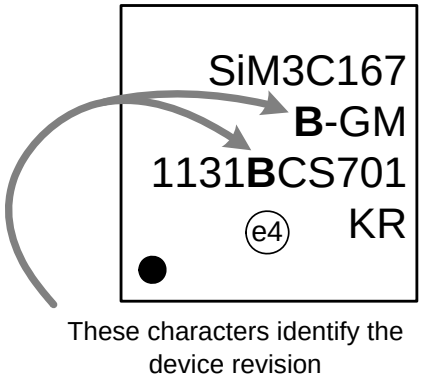

Figure 7.1. LGA-92 SiM3C1x7 Revision Information

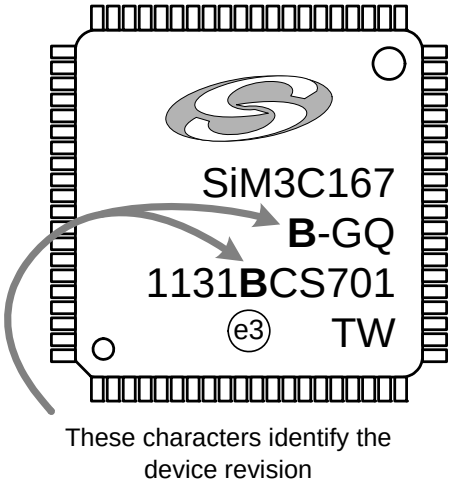

Figure 7.2. TQFP-80 SiM3C1x7 Revision Information