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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u144-b-gmr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit				
3.3 V Regulator Characteristics (VREG0, Supplied from VREGIN Pin)										
Output Voltage (at VDD pin)	V _{DDOUT}	$\begin{array}{c} 4 \leq V_{\text{REGIN}} \leq 5.5\\ \text{BGDIS} = 0, \text{ SUSEN} = 0 \end{array}$		3.3	3.4	V				
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = 1	3.15	3.3	3.4	V				
		$\begin{array}{l} 4 \leq V_{REGIN} \leq 5.5 \\ BGDIS = 1, SUSEN = X \\ I_{DDOUT} = 500 \; \mu A \end{array}$	2.3	2.8	3.6	V				
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X I _{DDOUT} = 5 mA	2.1	2.65	3.3	V				
Output Current (at VDD pin)*	IDDOUT	$4 \le V_{\text{REGIN}} \le 5.5$ BGDIS = 0, SUSEN = X	_		150	mA				
		$4 \le V_{\text{REGIN}} \le 5.5$ BGDIS = 1, SUSEN = X	_		5	mA				
Output Load Regulation	V _{DDLR}	BGDIS = 0	_	0.1	1	mV/mA				
Output Capacitance	C _{VDD}		1		10	μF				
*Note: Total current VREG0 is capable of p external devices powered from VDE	providing. A).	ny current consumed by the S	SiM3C1xx	reduces the	e current av	vailable to				

Table 3.5. On-Chip Regulators



Table 3.10. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Differential Nonlinearity	DNL	12 Bit Mode ²	-1	±0.7	1.8	LSB
(Guaranteed Monotonic)		10 Bit Mode	_	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E _{OFF}	12 Bit Mode, VREF =2.4 V	-2	0	2	LSB
		10 Bit Mode, VREF =2.4 V	-1	0	1	LSB
Offset Temperatue Coefficient	TC _{OFF}		_	0.004		LSB/°C
Slope Error ³	E _M	12 Bit Mode	-0.07	-0.02	0.02	%
Dynamic Performance with 10 k	Hz Sine Wav	/e Input 1 dB below full scale	, Max th	roughpu	ıt	
Signal-to-Noise	SNR	12 Bit Mode	62	66		dB
		10 Bit Mode	58	60		dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66		dB
		10 Bit Mode	58	60		dB
Total Harmonic Distortion	THD	12 Bit Mode	_	78		dB
(Up to 5th Harmonic)		10 Bit Mode	_	77	_	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	_	-79		dB
		10 Bit Mode	-	-74		dB
	1	<u>.</u>				

Notes:

1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.

2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.

3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.



Table 3.11. IDAC

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Static Performance						
Resolution	N _{bits}			10		Bits
Integral Nonlinearity	INL			±0.5	<u>+2</u>	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V _{OCR}		—		V _{DD} – 1.0	V
Full Scale Output Current	I _{OUT}	2 mA Range	2.0	2.046	2.10	mA
		1 mA Range	0.99	1.023	1.05	mA
		0.5 mA Range	493	511.5	525	μA
Offset Error	E _{OFF}			250	—	nA
Full Scale Error Tempco	TC _{FS}	2 mA Range	—	100	—	ppm/°C
VDD Power Supply Rejection Ratio		2 mA Range		-220		ppm/V
Test Load Impedance (to V _{SS})	R _{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	_	1.2	_	μs
Startup Time				3	—	μs



Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
P-Channel Source Current Limit	I _{SRCL}	Mode 0	_	0.8		mA
$(2.7 \text{ V} \leq \text{VIOHD} \leq 6 \text{ V},$		Mode 1		1.25		-
V _{OH} = VIOHD – 0.8 V)		Mode 2		1.75		-
See Figure 3.2		Mode 3		2.5		-
		Mode 4		3.5		-
		Mode 5		4.75		-
		Mode 6		7		-
		Mode 7	_	9.5		-
		Mode 8	_	14		-
		Mode 9	_	18.75		-
		Mode 10	_	28.25	_	-
		Mode 11	_	37.5		-
		Mode 12	_	56.25		-
		Mode 13	_	75	_	-
		Mode 14	_	112.5	_	-
		Mode 15	_	150	_	-
Total P-Channel Source Current on P4.0-P4.5 (DC)	I _{SRCLT}		_	_	400	mA
Pin Capacitance	C _{IO}		_	30		pF
Weak Pull-Up Current in Low Volt- age Mode	I _{PU}	V _{IOHD} = 1.8 V	-6	-3.5	-2	μA
		V _{IOHD} = 3.6 V	-30	-20	-10	μA
Weak Pull-Up Current in High Volt- age Mode	I _{PU}	V _{IOHD} = 2.7 V	-15	-10	-5	μA
		V _{IOHD} = 6 V	-30	-20	-10	μA
Input Leakage (Pullups off)	I _{LK}		-1	_	1	μA
*Note: RESET does not drive to logic h	igh. Specific	cations for RESET V _{OL} adhe	ere to the low d	rive setting.		



Table 3.19. Absolute	Maximum	Ratings	(Continued)
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Parameter	Symbol	Test Condition	Min	Мах	Unit
Power Dissipation at T _A = 85 °C	PD	LGA-92 Package		570	mW
		TQFP-80 Package	—	500	mW
		QFN-64 Package		800	mW
		TQFP-64 Package		650	mW
		QFN-40 Package	—	650	mW
*Note: VSS and VSSHD provide separate connected to the same potential on	return curre board.	ent paths for device supplies,	but are not isol	ated. They must al	ways be



4.1.5. Device Power Modes

The SiM3C1xx devices feature four low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low-Power Timer (LPT0), RTC0 (alarms and oscillator failure notification), Comparator 0, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0)

Normal Mode is the default mode of the device. The core and peripherals are fully operational, and instructions are executed from flash memory.

4.1.5.2. Power Mode 1

In Power Mode 1 the core and peripherals are fully operational, with instructions executing from RAM. Compared with Normal Mode, the active power consumption of the device in PM1 is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAM does not require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2

In Power Mode 2 the core halts and any enabled peripherals continue to run at the selected clock speed. The power consumption in PM2 corresponds to the AHB and APB clocks left enabled, thus the power can be tuned to the optimal level for the needs of the application. To place the device in PM2, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0 with the DMACTRL0 AHB clock disabled, PM2 can achieve similar power consumption to PM3, but with the ability to wake on APB-clocked interrupts. For example, enabling only the APB clock to the Ports will allow the firmware to wake on a PMATCH0, PBEXT0 or PBEXT1 interrupt with minimal impact on the supply current.

4.1.5.4. Power Mode 3

In Power Mode 3, the AHB and APB clocks are halted. The device may only wake from enabled interrupt sources which do not require the APB clock (RTC0ALRM, RTC0FAIL, LPTIMER0, VDDLOW and VREGLOW). A special fast wake option allows the device to operate at a very low level from the RTC0TCLK or LFOSC0 oscillator while in PM3, but quickly switch to the faster LPOSC0 when the wake event occurs. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

The device will enter PM3 on a WFI or WFE instruction. Because all AHB master clocks are disabled, the LPOSC will automatically halt and go into a low-power suspended state. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 9

In Power Mode 9, the core and all peripherals are halted, all clocks are stopped, and the pins and peripherals are set to a lower power mode. In addition, standard RAM contents are not preserved, though retention RAM contents are still available after exiting the power mode. This mode provides the lowest power consumption for the device, but requires an appropriate reset to exit. The available reset sources to wake from PM9 are controlled by the Power Management Unit (PMU).

Before entering PM9, the desired reset source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the RSTSRC0_CONFIG register must be set to indicate that PM9 is the desired power mode.

The device will enter PM9 on a WFI or WFE instruction, and remain in PM9 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.



4.2. I/O

4.2.1. General Features

The SiM3C1xx ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB2 only) to generate simple square waves.
- A subset of pins can also serve as inputs to the Port Mapped Level Shifters available on the High Drive Pins.

4.2.2. High Drive Pins (PB4)

The High Drive pins have the following additional features:

- Programmable safe state: high, low, or high impedance.
- Programmable drive strength and slew rates.
- Programmable hardware current limiting.
- Powered from a separate source (VIOHD, which can be up to 6 V) from the rest of the device.
- Supports various functions, including GPIO, UART1 pins, EPCA0 pins, or Port Mapped Level Shifting.

4.2.3. 5 V Tolerant Pins (PB3)

The 5 V tolerant pins can be connected to external circuitry operating at voltages above the device supply without needing extra components to shift the voltage level.

4.2.4. Crossbars

The SiM3C1xx devices have two Crossbars with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The Crossbars have a fixed priority for each I/O function and assign these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the Crossbars skip that pin when assigning the next selected resource. Additionally, the Crossbars will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.



4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.





4.7. Analog

4.7.1. 12-Bit Analog-to-Digital Converters (SARADC0, SARADC1)

The SARADC0 and SARADC1 modules on SiM3C1xx devices are Successive Approximation Register (SAR) Analog to Digital Converters (ADCs). The key features of the SARADC module are:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- Output data window comparator allows automatic range checking.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to 8 sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Multiple SARADC modules can work together synchronously or by interleaving samples.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.7.2. Sample Sync Generator (SSG0)

The SSG module includes a phase counter and a pulse generator. The phase counter is a 4-bit free-running counter clocked from the SARADC module clock. Counting-up from zero, the phase counter marks sixteen equally-spaced events for any number of SARADC modules. The ADCs can use this phase counter to start a conversion. The programmable pulse generator creates a 50% duty cycle pulse with a period of 16 phase counter ticks. Up to four programmable outputs available to external devices can be driven by the pulse generator with programmable polarity and a defined output setting when the pulse generator is stopped.

The Sample Sync Generator module has the following features:

- Connects multiple modules together to perform synchronized actions.
- Outputs a clock synchronized to the internal sampling clock used by any number of SARADC modules to pins for use by external devices.
- Includes a phase counter, pulse generator, and up to four programmable outputs.

4.7.3. 10-Bit Digital-to-Analog Converter (IDAC0, IDAC1)

The IDAC takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O, on demand, and SSG0 output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources (DACnTx).
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.



5. Ordering Information



Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- Core: ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- Flash Program Memory: 32-256 kB, in-system programmable.
- RAM: 8–32 kB SRAM, with 4 kB retention SRAM
- I/O: Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- Clock Sources: Internal and external oscillator options.
- 16-Channel DMA Controller.
- 128/192/256-bit AES.
- 16/32-bit CRC.
- **Timers:** 2 x 32-bit (4 x 16-bit).
- Real-Time Clock.
- Low-Power Timer.
- PCA: 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- ADC: 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- Temperature Sensor.
- Internal VREF.
- 16-channel Capacitive Sensing (CAPSENSE).
- **Comparator:** 2 x low current.
- Current to Voltage Converter (IVC).
- Serial Buses: 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I²S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.



Pin Name	Туре	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.4	5 V Tolerant I/O	16	A9	XBR1	~	ŌĒ			INT0.9 INT1.9 WAKE.8	CMP0P.4 CMP1P.4
PB3.5	5 V Tolerant I/O	15	B7	XBR1	>	ALEm			DAC0T2 DAC1T2 INT0.10 INT1.10 WAKE.9	CMP0N.4 CMP1N.4
PB3.6	5 V Tolerant I/O	14	A8	XBR1	~	CS0			DAC0T3 DAC1T3 INT0.11 INT1.11 WAKE.10	CMP0P.5 CMP1P.5
PB3.7	5 V Tolerant I/O	13	B6	XBR1	~	BE1			DAC0T4 DAC1T4 LPT0T1 INT0.12 INT1.12 WAKE.11	CMP0N.5 CMP1N.5
PB3.8	5 V Tolerant I/O	12	A7	XBR1	>	CS1			DAC0T5 DAC1T5 LPT0T2 INT0.13 INT1.13 WAKE.12	CMP0P.6 CMP1P.6 EXREGSP
PB3.9	5 V Tolerant I/O	11	B5	XBR1	~	BE0			DAC0T6 DAC1T6 INT0.14 INT1.14 WAKE.13	CMP0N.6 CMP1N.6 EXREGSN
PB3.10	5 V Tolerant I/O	10	B4	XBR1	~				INT0.15 INT1.15 WAKE.14	CMP0P.7 CMP1P.7 EXREGOUT
PB3.11	5 V Tolerant I/O	9	B3	XBR1	\checkmark				WAKE.15	CMP0N.7 CMP1N.7 EXREGBD

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)



6.2. SiM3C1x6 Pin Definitions





Pin Name	Туре	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	~	BE0			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)



Pin Name	Туре	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	26	XBR0	~			ADC0.14 ADC1.14
PB0.9	Standard I/O	25	XBR0	~			ADC0.15 ADC1.15
PB0.10	Standard I/O	22	XBR0	\checkmark		DMA0T1	ADC1.8
PB0.11	Standard I/O	21	XBR0	\checkmark		DMA0T0	ADC1.7
PB0.12	Standard I/O	20	XBR0	~		ADC0T15 WAKE.0	ADC1.5 CS0.10
PB0.13	Standard I/O	19	XBR0	~		ADC1T15 WAKE.1	ADC1.4 CS0.11
PB0.14	Standard I/O	18	XBR0	~		WAKE.2	ADC1.3 CS0.12
PB0.15	Standard I/O	17	XBR0	~		WAKE.3	ADC1.2 CS0.13
PB1.0	Standard I/O	16	XBR0	V		WAKE.4	ADC1.1 CS0.14
PB1.1	Standard I/O	15	XBR0	\checkmark		WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.2	Standard I/O	12	XBR0	~			CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB1.3	Standard I/O	11	XBR0	V			CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	10	XBR1	V		DAC0T0 DAC1T0 LPT0T0 INT0.0 INT1.0 WAKE.12	CMP0P.1 CMP1P.1 EXREGSP

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)



6.4.1. LGA-92 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

6.4.2. LGA-92 Stencil Design

- 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).
- 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
- 4. A 2 x 2 array of 1.25 mm square openings on 1.60 mm pitch should be used for the center ground pad.

6.4.3. LGA-92 Card Assembly

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. TQFP-80 Stencil Design

- 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).
- 3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.5.3. TQFP-80 Card Assembly

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.





6.6. QFN-64 Package Specifications



Dimension	Min	Nominal	Max				
Α	0.80	0.85	0.90				
A1	0.00	0.02	0.05				
b	0.18	0.25	0.30				
D		9.00 BSC					
D2	3.95	4.10	4.25				
е		0.50 BSC					
E		9.00 BSC					
E2	3.95	4.10	4.25				
L	0.30	0.40	0.50				
aaa		0.10					
bbb		0.10					
CCC	0.08						
ddd		0.10					
eee		0.05					
	·						

Table 6.8. QFN-64 Package Dimensions

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This package outline conforms to JEDEC MO-220.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.





Figure 6.13. TQFP-64 Landing Diagram

 Table 6.11. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Мах						
C1	11.30	11.40						
C2	11.30	11.40						
E	0.50 BSC							
X	0.20	0.30						
Y	1.40	1.50						
Notes: 1. All dimensions sh noted. 2. This land pattern	 Notes: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This land pattern design is based on the IPC-7351 guidelines. 							





Figure 6.15. QFN-40 Landing Diagram

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65
N. A.	

Table 6.13. QFN-40 Landing Diagram Dimensions

Notes:

- 1. All dimensions shown are in millimeters (mm).
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.
- **3.** All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a
 - Fabrication Allowance of 0.05 mm.





Figure 7.3. SiM3C1x6 Revision Information





7.2. Comparator Rising/Falling Edge Flags in Debug Mode (CMP0, CMP1)

7.2.1. Problem

On Revision A and Revision B devices, if the comparator output is high, the comparator rising and falling edge flags will both be set to 1 upon single-step or exit from debug mode.

7.2.2. Impacts

Firmware using the rising and falling edge flags to make decisions may see a false trigger of the comparator if the output of the comparator is high during a debug session. This does not impact the non-debug operation of the device.

7.2.3. Workaround

There is not a system-agnostic workaround for this issue.

7.2.4. Resolution

This issue exists on Revision A and Revision B devices. It may be corrected in a future device revision.

