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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	28
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u154-b-gmr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
V _{DD} High Supply Monitor Threshold	V _{VDDMH}	Early Warning	2.10	2.20	2.30	V
(VDDHITHEN = 1)		Reset	1.95	2.05	2.1	V
V _{DD} Low Supply Monitor Threshold	V_{VDDML}	Early Warning	1.81	1.85	1.88	V
(VDDHITHEN = 0)		Reset	1.70	1.74	1.77	V
V _{REGIN} Supply Monitor Threshold	V _{VREGM}	Early Warning	4.2	4.4	4.6	V
Power-On Reset (POR) Threshold	V _{POR}	Rising Voltage on V_{DD}		1.4	—	V
		Falling Voltage on V_{DD}	0.8	1	1.3	V
V _{DD} Ramp Time	t _{RMP}	Time to $V_{DD} \ge 1.8 V$	10		3000	μs
Reset Delay from POR	t _{POR}	Relative to V _{DD} ≥ V _{POR}	3		100	ms
Reset Delay from non-POR source	t _{RST}	Time between release of reset source and code execution	—	10		μs
RESET Low Time to Generate Reset	t _{RSTL}		50		_	ns
Missing Clock Detector Response Time (final rising edge to reset)	t _{MCD}	F _{AHB} > 1 MHz		0.4	1	ms
Missing Clock Detector Trigger Frequency	F _{MCD}			7.5	13	kHz
V _{DD} Supply Monitor Turn-On Time	t _{MON}		_	2		μs



Table 3.8. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit			
Low Power Oscillator (LPOSC0)									
Oscillator Frequency	f _{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz			
		T _A = 25 °C, V _{DD} = 3.3 V	19.5	20	20.5	MHz			
Divided Oscillator Frequency	f _{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz			
Power Supply Sensitivity	PSS _{LPOSC}	T _A = 25 °C	_	0.5		%/V			
Temperature Sensitivity	TS _{LPOSC}	V _{DD} = 3.3 V		55		ppm/°C			
Low Frequency Oscillator (LFOS	C0)								
Oscillator Frequency	f _{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz			
		T _A = 25 °C, V _{DD} = 3.3 V	15.8	16.4	17.3	kHz			
Power Supply Sensitivity	PSS _{LFOSC}	T _A = 25 °C		2.4	_	%/V			
Temperature Sensitivity	TS _{LFOSC}	V _{DD} = 3.3 V		0.2		%/°C			
RTC0 Oscillator (RTC0OSC)									
Missing Clock Detector Trigger Frequency	f _{RTCMCD}		_	8	15	kHz			
RTC Robust Duty Cycle Range	DC _{RTC}		25	_	55	%			
*Note: PLL0OSC in free-running oscill	ator mode.	·							

Table 3.9. External Oscillator

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
External Input CMOS Clock Frequency*	f _{CMOS}		0		50	MHz		
External Input CMOS Clock High Time	t _{CMOSH}		9		—	ns		
External Input CMOS Clock Low Time	t _{CMOSL}		9		—	ns		
External Crystal Clock Frequency	f _{XTAL}		0.01		30	MHz		
*Note: Minimum of 10 kHz during debug operations.								



Table 3.10. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Differential Nonlinearity	DNL	12 Bit Mode ²	-1	±0.7	1.8	LSB
(Guaranteed Monotonic)		10 Bit Mode	_	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E _{OFF}	12 Bit Mode, VREF =2.4 V	-2	0	2	LSB
		10 Bit Mode, VREF =2.4 V	-1	0	1	LSB
Offset Temperatue Coefficient	TC _{OFF}		_	0.004		LSB/°C
Slope Error ³	E _M	12 Bit Mode	-0.07	-0.02	0.02	%
Dynamic Performance with 10 k	Hz Sine Wav	/e Input 1 dB below full scale	, Max th	roughpu	ıt	
Signal-to-Noise	SNR	12 Bit Mode	62	66		dB
		10 Bit Mode	58	60		dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66		dB
		10 Bit Mode	58	60		dB
Total Harmonic Distortion	THD	12 Bit Mode	_	78		dB
(Up to 5th Harmonic)		10 Bit Mode	_	77	_	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	_	-79		dB
		10 Bit Mode	-	-74		dB
	1	<u>.</u>				

Notes:

1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.

2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.

3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.



Table 3.12. Capacitive Sense

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Single Conversion Time	t _{single}	12-bit Mode	—	25		μs
(Default Configuration)		13-bit Mode	—	27		μs
		14-bit Mode	—	29	_	μs
		16-bit Mode	—	33	_	μs
Maximum External Capacitive Load	CL	Highest Gain Setting (default)		45	—	pF
		Lowest Gain Setting		500		pF
Maximum External Series Impedance	CL	Highest Gain Setting (default)		50	—	kΩ

Table 3.13. Current-to-Voltage Converter (IVC)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply Voltage (VDD)	V _{DDIVC}		2.2	—	3.6	V
Input Pin Voltage	V _{IN}		2.2		VDD	V
Minimum Input Current (source)	I _{IN}		100		—	μA
Integral Nonlinearity	INL _{IVC}		-0.6		0.6	%
Full Scale Output	VIVCOUT			1.65		V
Slope	M _{IVC}	Input Range 1 mA (INxRANGE = 101)	1.55	1.65	1.75	V/mA
		Input Range 2 mA (INxRANGE = 100)	795	830	860	mV/mA
		Input Range 3 mA (INxRANGE = 011)	525	550	570	mV/mA
		Input Range 4 mA (INxRANGE = 010)	390	415	430	mV/mA
		Input Range 5 mA (INxRANGE = 001)	315	330	340	mV/mA
		Input Range 6 mA (INxRANGE = 000)	260	275	285	mV/mA
Settling Time to 0.1%	VIVCOUT				500	ns



Table 3.14. Voltage Reference Electrical Characteristics

 V_{DD} = 1.8 to 3.6 V, -40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit				
Internal Fast Settling Refere	Internal Fast Settling Reference									
Output Voltage	V _{REFFS}	-40 to +85 °C, V _{DD} = 1.8-3.6 V	1.62	1.65	1.68	V				
Temperature Coefficient	TC _{REFFS}			50	—	ppm/°C				
Turn-on Time	t _{REFFS}		—	_	1.5	μs				
Power Supply Rejection	PSRR _{REFFS}		_	400	—	ppm/V				
On-Chip Precision Referenc	e (VREF0)									
Valid Supply Range	V _{DD}	VREF2X = 0	1.8	_	3.6	V				
		VREF2X = 1	2.7		3.6	V				
Output Voltage	V _{REFP}	25 °C ambient, VREF2X = 0	1.195	1.2	1.205	V				
		25 °C ambient, VREF2X = 1	2.39	2.4	2.41	V				
Short-Circuit Current	I _{SC}		—		10	mA				
Temperature Coefficient	TC _{VREFP}		—	25	—	ppm/°C				
Load Regulation	LR _{VREFP}	Load = 0 to 200 µA to VREFGND		4.5	_	ppm/µA				
Load Capacitor	C _{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	_	—	μF				
Turn-on Time	t _{VREFPON}	4.7 μF tantalum, 0.1 μF ceramic bypass		3.8		ms				
		0.1 µF ceramic bypass		200	—	μs				
Power Supply Rejection	PSRR _{VREFP}	VREF2X = 0	—	320	—	ppm/V				
		VREF2X = 1	—	560	—	ppm/V				
External Reference	•									
Input Current	I _{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	μA				









Figure 3.2. Maximum Source Current vs. PB4.x Pin Voltage



3.2. Thermal Conditions

Table 3.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Thermal Resistance*	θ_{JA}	LGA-92 Packages		35		°C/W
		TQFP-80 Packages		40		°C/W
		QFN-64 Packages		25		°C/W
		TQFP-64 Packages		30		°C/W
		QFN-40 Packages		30		°C/W
*Note: Thermal resistance assumes a	multi-layer F	CB with any exposed pad sc	ldered to a PC	B pad.		

3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T _{BIAS}		-55	125	°C
Storage Temperature	T _{STG}		-65	150	°C
Voltage on VDD	V _{DD}		V _{SS} –0.3	4.2	V
Voltage on VREGIN	V _{REGIN}	EXTVREG0 Not Used	V _{SS} –0.3	6.0	V
		EXTVREG0 Used	V _{SS} –0.3	3.6	V
Voltage on VIO	V _{IO}		V _{SS} –0.3	4.2	V
Voltage on VIOHD	V _{IOHD}		V _{SS} –0.3	6.5	V
Voltage on I/O pins,	V _{IN}	RESET, V _{IO} ≥ 3.3 V	V _{SS} –0.3	5.8	V
		RESET, V _{IO} < 3.3 V	V _{SS} –0.3	V _{IO} +2.5	V
		Port Bank 0, 1, and 2 I/O	V _{SS} -0.3	V _{IO} +0.3	V
		Port Bank 4 I/O	V _{SSHD} -0.3	V _{IOHD} +0.3	V
	4	·			·

*Note: VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.



4.4. Data Peripherals

4.4.1. 16-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 16 channels.
- DMA crossbar supports SARADC0, SARADC1, IDAC0, IDAC1, I2C0, I2S0, SPI0, SPI1, USART0, USART1, AES0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

4.4.2. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for a set of 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Cipher-Block Chaining (CBC) and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

4.4.3. 16/32-bit CRC (CRC0)

The CRC module is designed to provide hardware calculations for Flash memory verification and communications protocols.

The CRC module supports four common polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The three supported 16-bit polynomials are 0x1021 (CCITT-16), 0x3D65 (IEC16-MBus), and 0x8005 (ZigBee, 802.15.4, and USB).

The CRC module includes the following features:

- Support for four common polynomials (one 32-bit and three 16-bit options).
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32- or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Support for DMA writes using firmware request mode.



4.5.3. Real-Time Clock (RTC0)

The RTC0 module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC0 provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3C1xx devices.

The RTC0 module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC0 output can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal low frequency oscillator (LFOSC0), an external 32.768 kHz crystal (no additional resistors or capacitors necessary), or with an external CMOS clock.
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- Operates directly from VDD and remains operational even when the device goes into its lowest power down mode.
- The RTC timer clock (RTC0TCLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.

4.5.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER0) module runs from the clock selected by the RTC0 module, allowing the LPTIMER0 to operate even if the AHB and APB clocks are disabled. The LPTIMER0 counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on a low-frequency clock (RTC0TCLK)
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection, which can generate an interrupt, reset the timer, or wake some devices from low power modes.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.

4.5.5. Watchdog Timer (WDTIMER0)

The WDTIMER0 module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.



4.6. Communications Peripherals

4.6.1. External Memory Interface (EMIF0)

The External Memory Interface (EMIF0) allows external parallel asynchronous devices, like SRAMs and LCD controllers, to appear as part of the system memory map. The EMIF0 module includes the following features:

- Provides a memory mapped view of multiple external devices.
- Support for byte, half-word and word accesses regardless of external device data-width.
- Error indicator for certain invalid transfers.
- Minimum external timing allows for 3 clocks per write or 4 clocks per read.
- Output bus can be shared between non-muxed and muxed devices.
- Available extended address output allows for up to 24-bit address with 8-bit parallel devices.
- Support for 8-bit and 16-bit (muxed-mode only) devices with up to two chip-select signals.
- Support for internally muxed devices with dynamic address shifting.
- Fully programmable control signal waveforms.

4.6.2. USART (USART0, USART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device. In addition to these signals, the USART0 module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.6.3. UART (UART0, UART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device.

The UART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud-rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX) or 1 Mbaud Smartcard (TX or RX).



• Spike suppression up to 2 times the APB period.

4.6.6. I²S (I2S0)

The I²S module receives digital data from an external source over a data line in the standard I²S, left-justified, rightjustified, or time domain multiplexing format, de-serializes the data, and generates requests to transfer the data using the DMA. The module also reads stereo audio samples from the DMA, serializes the data, and sends it out of the chip on a data line in the same standard serial format for digital audio. The I²S receive interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync), and SD (data input). The block's transmit interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync) and SD (data output).

The I²S module includes the following features:

- Master or slave capability.
- Flexible 10-bit clock divider with 8-bit fractional clock divider provides support for various common sampling frequencies (16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz) for up to two 32-bit channels.
- Support for DMA data transfers.
- Support for various data formats.
- Time Division Multiplexing



4.7.4. 16-Channel Capacitance-to-Digital Converter (CAPSENSE0)

The Capacitance Sensing module measures capacitance on external pins and converts it to a digital value. The CAPSENSE module has the following features:

- Multiple start-of-conversion sources (CSnTx).
- Option to convert to 12, 13, 14, or 16 bits.
- Automatic threshold comparison with programmable polarity ("less than or equal" or "greater than").
- Four operation modes: single conversion, single scan, continuous single conversion, and continuous scan.
- Auto-accumulate mode that will take and average multiple samples together from a single start of conversion signal.
- Single bit retry options available to reduce the effect of noise during a conversion.
- Supports channel bonding to monitor multiple channels connected together with a single conversion.
- Scanning option allows the module to convert a single or series of channels and compare against the threshold while the AHB clock is stopped and the core is in a low power mode.

4.7.5. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The Low Power Comparator module includes the following features:

- Multiple sources for the positive and negative poles, including VDD, VREF, and 8 I/O pins.
- Two outputs are available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.

4.7.6. Current-to-Voltage Converter (IVC0)

The IVC module provides inputs to the SARADCn modules so the input current can be measured. The IVC module has the following features:

- Two independent channels.
- Programmable input ranges (1–6 mA full-scale).



4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.



4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabilites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.



Table 6.1. Pin Definitions and alternate	e functions for SiM3C1x7	(Continued)
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Pin Name	Туре	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.9/ TRACECLK	Standard I/O /ETM	46	A28	XBR0	\checkmark					ADC1.9
PB1.10	Standard I/O	43	A26	XBR0	\checkmark	A23m/ A15			DMA0T1	ADC1.8
PB1.11	Standard I/O	42	A25	XBR0	\checkmark	A22m/ A14			DMA0T0	ADC1.7
PB1.12	Standard I/O	41	D3	XBR0	~	A21m/ A13				ADC1.6
PB1.13	Standard I/O	40	A24	XBR0	~	A20m/ A12			ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.14	Standard I/O	39	A23	XBR0	~	A19m/ A11			ADC1T15 WAKE.1	ADC1.4 CS0.11
PB1.15	Standard I/O	38	A22	XBR0	~	A18m/ A10			WAKE.2	ADC1.3 CS0.12
PB2.0	Standard I/O	37	B17	XBR1	~	A17m/ A9	LSI0	Yes	INT0.0 INT1.0 WAKE.3	ADC1.2 CS0.13
PB2.1	Standard I/O	36	A21	XBR1	\checkmark	A16m/ A8	LSI1	Yes	INT0.1 INT1.1 WAKE.4	ADC1.1 CS0.14
PB2.2	Standard I/O	35	B16	XBR1	~	AD15m/ A7	LSI2	Yes	INT0.2 INT1.2 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB2.3	Standard I/O	34	A20	XBR1	\checkmark	AD14m/ A6	LSI3	Yes	INT0.3 INT1.3 WAKE.6	
PB2.4	Standard I/O	31	B14	XBR1	V	AD13m/ A5	LSI4	Yes	INT0.4 INT1.4 WAKE.7	
PB2.5	Standard I/O	30	A18	XBR1	\checkmark	AD12m / A4	LSI5	Yes	INT0.5 INT1.5	







Pin Name	Туре	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	~	BE0			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)



Pin Name	Туре	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	26	XBR0	~			ADC0.14 ADC1.14
PB0.9	Standard I/O	25	XBR0	~			ADC0.15 ADC1.15
PB0.10	Standard I/O	22	XBR0	\checkmark		DMA0T1	ADC1.8
PB0.11	Standard I/O	21	XBR0	\checkmark		DMA0T0	ADC1.7
PB0.12	Standard I/O	20	XBR0	~		ADC0T15 WAKE.0	ADC1.5 CS0.10
PB0.13	Standard I/O	19	XBR0	~		ADC1T15 WAKE.1	ADC1.4 CS0.11
PB0.14	Standard I/O	18	XBR0	~		WAKE.2	ADC1.3 CS0.12
PB0.15	Standard I/O	17	XBR0	~		WAKE.3	ADC1.2 CS0.13
PB1.0	Standard I/O	16	XBR0	V		WAKE.4	ADC1.1 CS0.14
PB1.1	Standard I/O	15	XBR0	\checkmark		WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.2	Standard I/O	12	XBR0	~			CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB1.3	Standard I/O	11	XBR0	V			CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	10	XBR1	V		DAC0T0 DAC1T0 LPT0T0 INT0.0 INT1.0 WAKE.12	CMP0P.1 CMP1P.1 EXREGSP

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)





Figure 6.7. LGA-92 Landing Diagram

ension	Typical	Мах			
21	6.50	_			
22	6.50	—			
e	0.50				
f	—	0.35			
P1	—	3.20			
2	—	3.20			
 Notes: All dimensions shown are in millimeters (mm) unless otherwise noted. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed. 					
	ension 21 22 e f 21 22 dimensions shed. eature sizes s a card fabric: onsionica on	Image: sensionTypicalC16.50C26.50e0.50f—P1—P2—dimensions shown are in millimeters (med.eature sizes shown are at Maximum Ma card fabrication tolerance of 0.05 monsigning and Telerancing is part to A			

- Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 4. This land pattern design is based on the IPC-7351 guidelines.







Figure 6.8. TQFP-80 Package Drawing

Table 6.6.	TQFP-80	Package	Dimensions
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Dimension	Min Nominal		Max		
Α	_	—	1.20		
A1	0.05	—	0.15		
A2	0.95	1.00	1.05		
b	0.17	0.20	0.27		
С	0.09	—	0.20		
D	14.00 BSC				
D1	12.00 BSC				
е	e 0.50 BSC				
E	14.00 BSC				
E1	12.00 BSC				





6.6. QFN-64 Package Specifications



Dimension	Min	Max			
Α	0.80	0.85	0.90		
A1	0.00	0.02	0.05		
b	0.18	0.25	0.30		
D	9.00 BSC				
D2	3.95 4.10 4.25				
е	0.50 BSC				
E	9.00 BSC				
E2	3.95 4.10 4.25				
L	0.30 0.40 0.5				
aaa	0.10				
bbb	0.10				
CCC	0.08				
ddd	0.10				
eee	0.05				
	÷				

Table 6.8. QFN-64 Package Dimensions

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This package outline conforms to JEDEC MO-220.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

