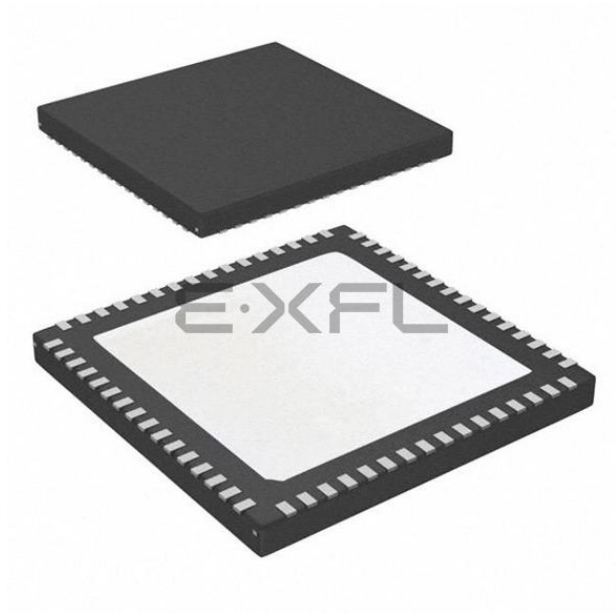

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u156-b-gmr

1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3C1xx device family.

1.1.1. SiM3U1xx/SiM3C1xx Reference Manual

The Silicon Laboratories SiM3U1xx/SiM3C1xx Reference Manual provides detailed functional descriptions for the SiM3C1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3C1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vector Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm.m3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

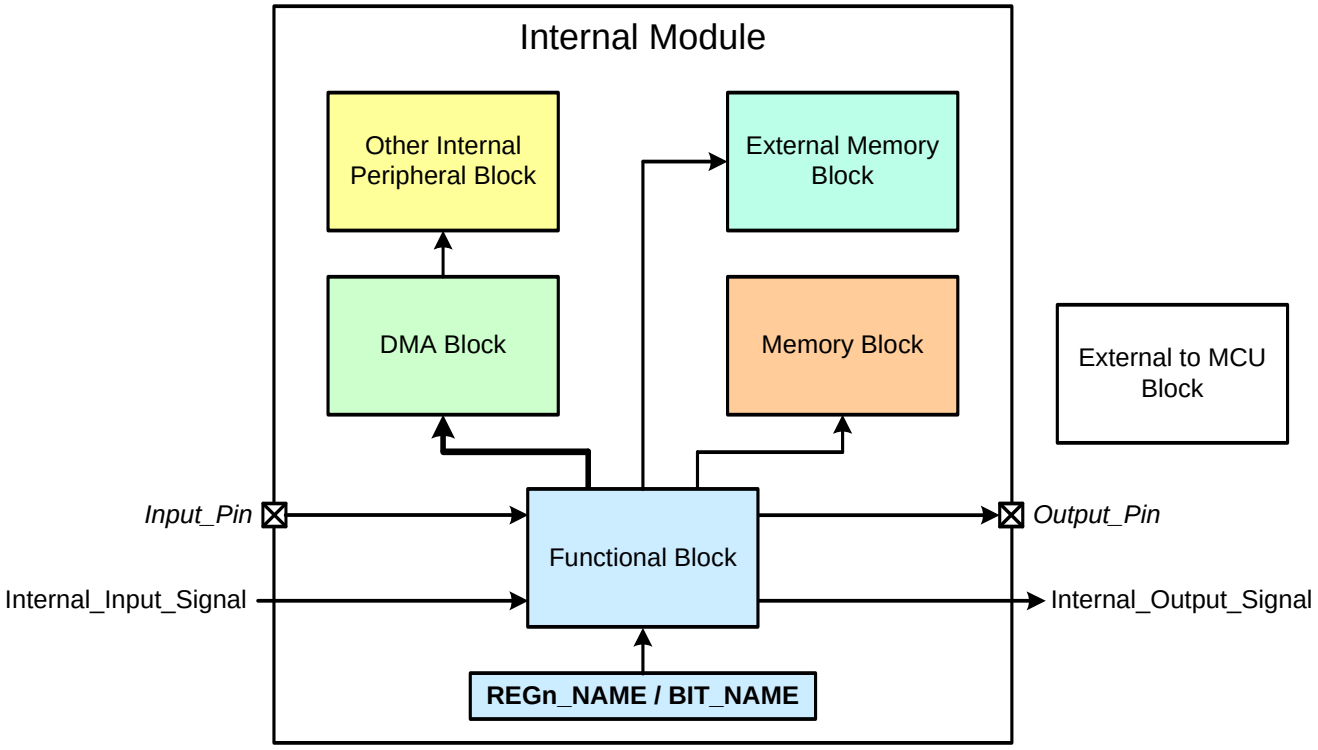


Figure 1.1. Block Diagram Conventions

2. Typical Connection Diagrams

This section provides typical connection diagrams for SiM3C1xx devices.

2.1. Power

Figure 2.1 shows a typical connection diagram for the power pins of the SiM3C1xx devices when the internal regulator is in use.

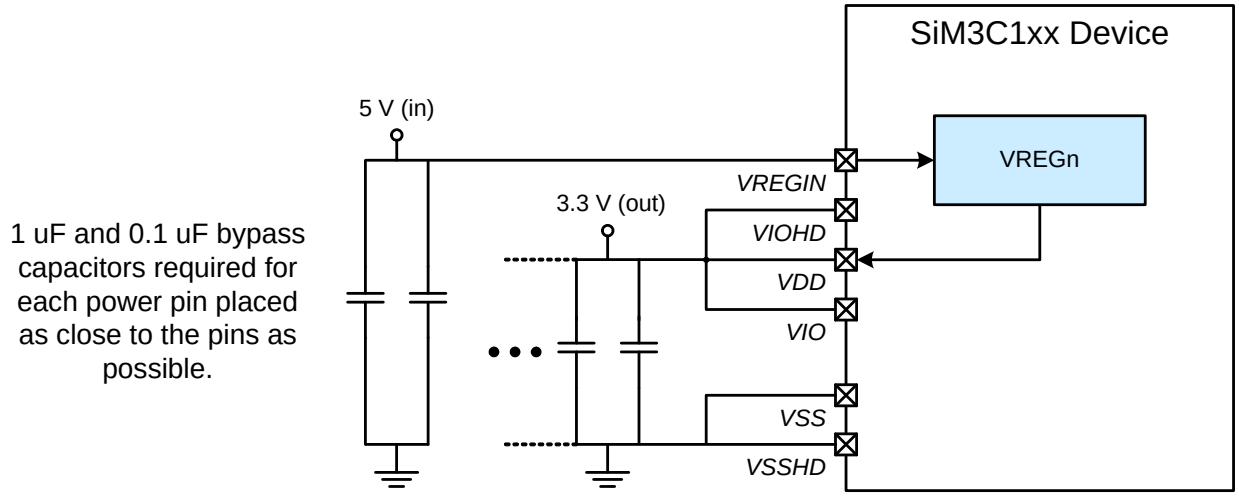


Figure 2.1. Connection Diagram with Voltage Regulator Used

Figure 2.2 shows a typical connection diagram for the power pins of the SiM3C1xx devices when the internal regulator is not used.

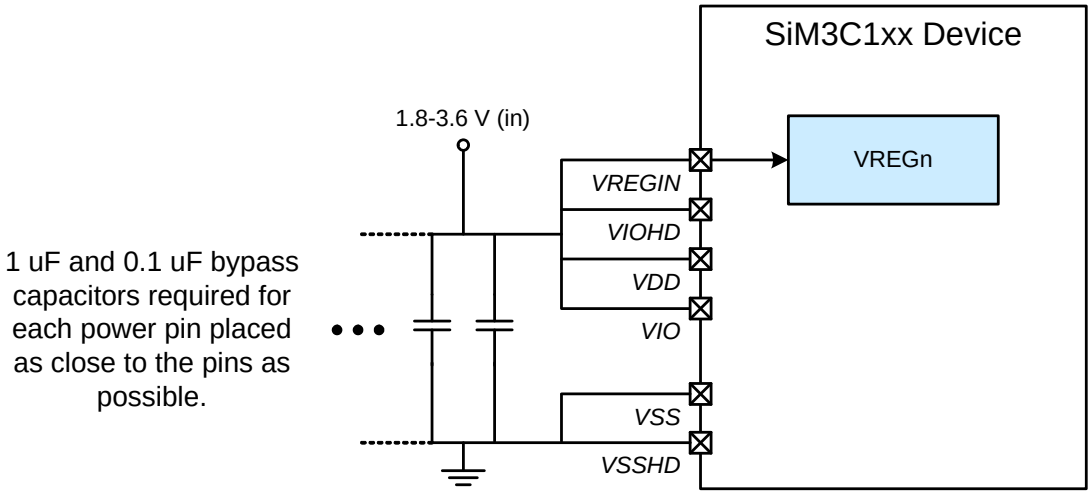


Figure 2.2. Connection Diagram with Voltage Regulator Not Used

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 9[2,3]—Low Power Shutdown with VREG0 disabled, powered through VDD and VIO	I_{DD}	RTC Disabled, V_{DD} = 1.8 V, T_A = 25 °C	—	85	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 1.8 V, T_A = 25 °C	—	350	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 1.8 V, T_A = 25 °C	—	620	—	nA
		RTC Disabled, V_{DD} = 3.0 V, T_A = 25 °C	—	145	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 3.0 V, T_A = 25 °C	—	500	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 3.0 V, T_A = 25 °C	—	800	—	nA
Power Mode 9[2,3]—Low Power Shutdown with VREG0 in low-power mode, VDD and VIO powered through VREG0 (Includes VREG0 current)	I_{VREGIN}	RTC Disabled, VREGIN = 5 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, VREGIN = 5 V, T_A = 25 °C	—	650	—	nA
		RTC w/ 32.768 kHz Crystal, VREGIN = 5 V, T_A = 25 °C	—	950	—	nA
VIOHD Current (High-drive I/O disabled)	I_{VIOHD}	HV Mode (default)	—	2.5	5	µA
		LV Mode	—	2	—	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.6. External Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range (at VREGIN)	V_{REGIN}		3.0	—	3.6	V
Output Voltage (at EXREGOUT)	$V_{EXREGOUT}$	Programmable in 100 mV steps	1.8	—	3.6	V
NPN Current Drive	I_{NPN}	400 mV Dropout	12	—	—	mA
PNP Current Drive	I_{PNP}	$V_{EXREGBD} > V_{REGIN}$- 1.5 V	–6	—	—	mA
EXREGBD Voltage (PNP Mode)	$V_{EXREGBD}$	V_{REGIN} >= 3.5 V	V_{REGIN} – 2.0	—	—	V
		V_{REGIN} < 3.5 V	1.5	—	—	V
Standalone Mode Output Current	$I_{EXTREGBD}$	400 mV Dropout	—	—	11.5	mA
External Capacitance with External BJT	C_{BJT}		4.7	—	—	µF
Standalone Mode Load Regulation	$LR_{STAND-ALONE}$		—	1	—	mV/mA
Standalone Mode External Capacitance	$C_{STAND-ALONE}$		47	—	—	nF
Current Limit Range	I_{LIMIT}	1 Ω Sense Resistor	10	—	720	mA
Current Limit Accuracy			—	—	10	%
Foldback Limit Accuracy			—	—	20	%
Current Sense Resistor	R_{SENSE}		—	—	1	Ω
Internal Pull-Down	R_{PD}		—	5	—	kΩ
Internal Pull-Up	R_{PU}		—	10	—	kΩ
Current Sensor						
Sensing Pin Voltage	$V_{EXTREGSP}$ $V_{EXTREGSN}$	Measured at EXTREGSP or EXTREGSN pin	2.2	—	V_{REGIN}	V
Differential Sensing Voltage	V_{DIFF}	($V_{EXTREGSP}$ – $V_{EXTREGSN}$)	10	—	1600	mV
Current at EXTREGSN Pin	$I_{EXTREGSN}$		—	8	—	µA
Current at EXTREGSP Pin	$I_{EXTREGSP}$		—	V_{DIFF} x 200 + 12	—	µA

Table 3.7. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
V_{DD} Voltage During Programming	V_{PROG}		1.8	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During a sequential write operation, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 3.8. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency*	$f_{PLL0OSC}$	Full Temperature and Supply Range	77	79	80	MHz
Power Supply Sensitivity*	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 79 MHz	—	430	—	ppm/V
Temperature Sensitivity*	$TS_{PLL0OSC}$	V_{DD} = 3.3 V, Fout = 79 MHz	—	95	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	80	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 80 MHz, M=24, N=99, LOCKTH = 0	—	1.7	—	µs
		f_{REF} = 32 kHz, $f_{PLL0OSC}$ = 80 MHz, M=0, N=2440, LOCKTH = 0	—	91	—	µs

***Note:** PLL0OSC in free-running oscillator mode.

Table 3.10. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode[2]	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF =2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF =2.4 V	–1	0	1	LSB
Offset Temperatue Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error[3]	E_M	12 Bit Mode	–0.07	–0.02	0.02	%
Dynamic Performance with 10 kHz Sine Wave Input 1 dB below full scale, Max throughput						
Signal-to-Noise	SNR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	78	—	dB
		10 Bit Mode	—	77	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

Table 3.11. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{DD} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range	2.0	2.046	2.10	mA
		1 mA Range	0.99	1.023	1.05	mA
		0.5 mA Range	493	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VDD Power Supply Rejection Ratio		2 mA Range	—	-220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Table 3.17. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard I/O (PB0, PB1, and PB2), 5 V Tolerant I/O (PB3), and $\overline{\text{RESET}}$						
Output High Voltage*	V_{OH}	Low Drive, I_{OH} = –2 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –5 mA	V_{IO} – 0.7	—	—	V
Output Low Voltage*	V_{OL}	Low Drive, I_{OL} = 3 mA	—	—	0.6	V
		High Drive, I_{OL} = 12.5 mA	—	—	0.6	V
Input High Voltage	V_{IH}	1.8 ≤ V_{IO} ≤ 2.0	0.7 x V_{IO}	—	—	V
		2.0 ≤ V_{IO} ≤ 3.6	V_{IO} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}	PB0, PB1 and PB2 Pins	—	4	—	pF
		PB3 Pins	—	7	—	pF
Weak Pull-Up Current (Input Voltage = 0 V)	I_{PU}	V_{IO} = 1.8	–6	–3.5	–2	µA
		V_{IO} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	0 ≤ V_{IN} ≤ V_{IO}	–1	—	1	µA
Input Leakage Current of Port Bank 3 I/O, V_{IN} above V_{IO}	I_L	V_{IO} < V_{IN} < V_{IO}+2.0 V (pins without EXREG functions)	0	5	150	µA
		V_{IO} < V_{IN} < V_{REGIN} (pins with EXREG functions)	0	5	150	µA
High Drive I/O (PB4)						
Output High Voltage	V_{OH}	Standard Mode, Low Drive, I_{OH} = –3 mA	V_{IOHD} – 0.7	—	—	V
		Standard Mode, High Drive, I_{OH} = –10 mA	V_{IOHD} – 0.7	—	—	V
Output Low Voltage	V_{OL}	Standard Mode, Low Drive, I_{OH} = 3 mA	—	—	0.6	V
		Standard Mode, High Drive, I_{OH} = 12.5 mA	—	—	0.6	V
Output Rise Time	t_R	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

3.2. Thermal Conditions

Table 3.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	LGA-92 Packages	—	35	—	°C/W
		TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		V_{SS}–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	V_{SS}–0.3	6.0	V
		EXTVREG0 Used	V_{SS}–0.3	3.6	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIOHD	V_{IOHD}		V_{SS}–0.3	6.5	V
Voltage on I/O pins, non Port Bank 3 I/O	V_{IN}	$\overline{\text{RESET}}$, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$\overline{\text{RESET}}$, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		Port Bank 0, 1, and 2 I/O	V_{SS}–0.3	V_{IO}+0.3	V
		Port Bank 4 I/O	V_{SSHD}–0.3	V_{IOHD}+0.3	V
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Five output ranges with output frequencies ranging from 23 to 80 MHz.
- Multiple reference frequency inputs.
- Three output modes: free-running DCO, frequency-locked, and phase-locked.
- Ability to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.
- Ability to suspend all output frequency updates (including dithering and spectrum spreading) using the STALL bit during jitter-sensitive operations.

4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3C1xx devices and enables or disables automatically, as needed.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC0) provides a low power internal clock source running at approximately 16.4 kHz for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator

4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, RC, C, or CMOS oscillators.
- Support external CMOS frequencies from 10 kHz to 50 MHz and external crystal frequencies from 10 kHz to 30 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

4.5.3. Real-Time Clock (RTC0)

The RTC0 module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC0 provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3C1xx devices.

The RTC0 module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC0 output can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal low frequency oscillator (LFOSC0), an external 32.768 kHz crystal (no additional resistors or capacitors necessary), or with an external CMOS clock.
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- Operates directly from VDD and remains operational even when the device goes into its lowest power down mode.
- The RTC timer clock (RTC0TCLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.

4.5.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER0) module runs from the clock selected by the RTC0 module, allowing the LPTIMER0 to operate even if the AHB and APB clocks are disabled. The LPTIMER0 counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on a low-frequency clock (RTC0TCLK)
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection, which can generate an interrupt, reset the timer, or wake some devices from low power modes.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.

4.5.5. Watchdog Timer (WDTIMER0)

The WDTIMER0 module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

4.7.4. 16-Channel Capacitance-to-Digital Converter (CAPSENSE0)

The Capacitance Sensing module measures capacitance on external pins and converts it to a digital value. The CAPSENSE module has the following features:

- Multiple start-of-conversion sources (CSnTx).
- Option to convert to 12, 13, 14, or 16 bits.
- Automatic threshold comparison with programmable polarity (“less than or equal” or “greater than”).
- Four operation modes: single conversion, single scan, continuous single conversion, and continuous scan.
- Auto-accumulate mode that will take and average multiple samples together from a single start of conversion signal.
- Single bit retry options available to reduce the effect of noise during a conversion.
- Supports channel bonding to monitor multiple channels connected together with a single conversion.
- Scanning option allows the module to convert a single or series of channels and compare against the threshold while the AHB clock is stopped and the core is in a low power mode.

4.7.5. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The Low Power Comparator module includes the following features:

- Multiple sources for the positive and negative poles, including VDD, VREF, and 8 I/O pins.
- Two outputs are available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.

4.7.6. Current-to-Voltage Converter (IVC0)

The IVC module provides inputs to the SARADCn modules so the input current can be measured. The IVC module has the following features:

- Two independent channels.
- Programmable input ranges (1–6 mA full-scale).

6.2. SiM3C1x6 Pin Definitions

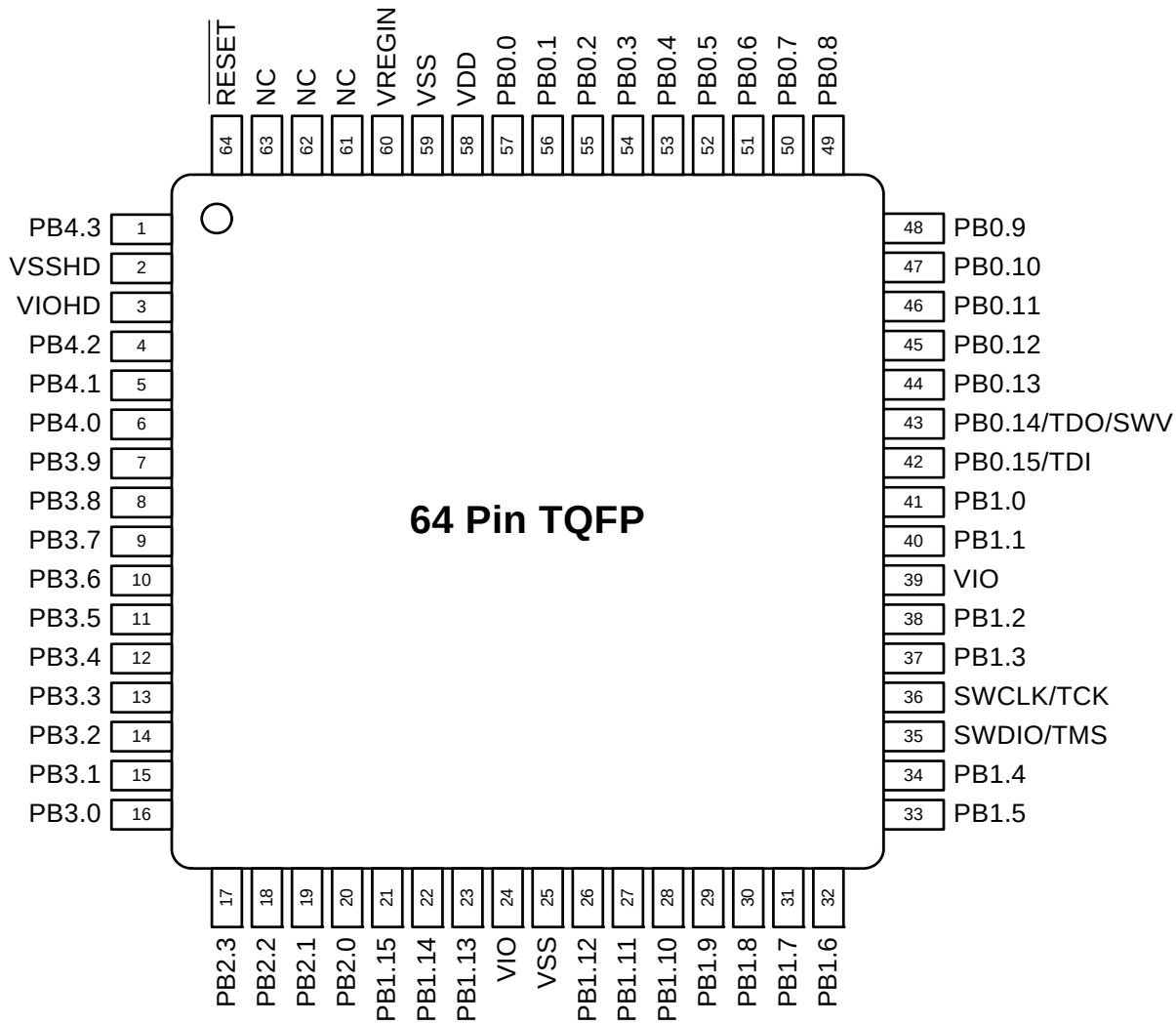


Figure 6.3. SiM3C1x6-GQ Pinout

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.1	5 V Tolerant I/O	9	XBR1	✓		DAC0T1 DAC1T1 LPT0T1 INT0.1 INT1.1 WAKE.13	CMP0N.1 CMP1N.1 EXREGSN
PB3.2	5 V Tolerant I/O	8	XBR1	✓		DAC0T2 DAC1T2 LPT0T2 INT0.2 INT1.3 WAKE.14	CMP0P.2 CMP1P.2 EXREGOUT
PB3.3	5 V Tolerant I/O	7	XBR1	✓		DAC0T3 DAC1T3 INT0.3 INT1.3 WAKE.15	CMP0N.2 CMP1N.2 EXREGBD
PB4.0	High Drive I/O	6					
PB4.1	High Drive I/O	5					
PB4.2	High Drive I/O	4					
PB4.3	High Drive I/O	1					

6.4. LGA-92 Package Specifications

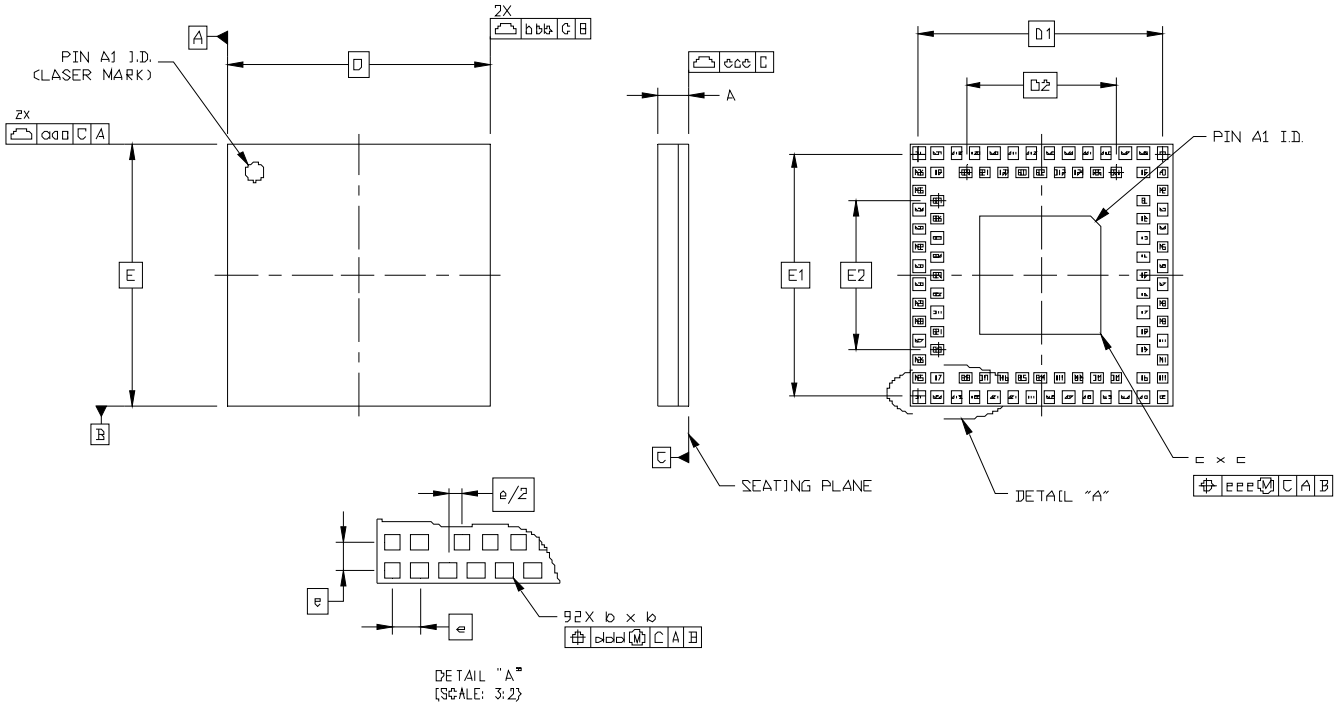


Figure 6.6. LGA-92 Package Drawing

Table 6.4. LGA-92 Package Dimensions

Dimension	Min	Nominal	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
c	3.15	3.20	3.25
D		7.00 BSC	
D1		6.50 BSC	
D2		4.00 BSC	
e		0.50 BSC	
E		7.00 BSC	
E1		6.50 BSC	
E2		4.00 BSC	
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

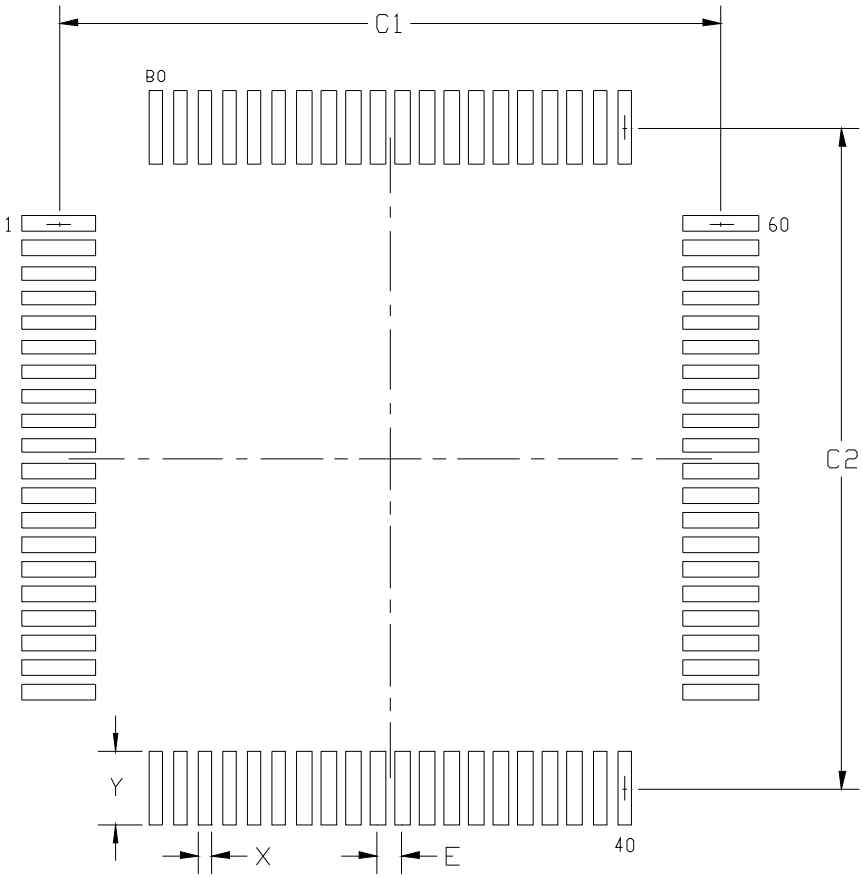


Figure 6.9. TQFP-80 Landing Diagram

Table 6.7. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.7. TQFP-64 Package Specifications

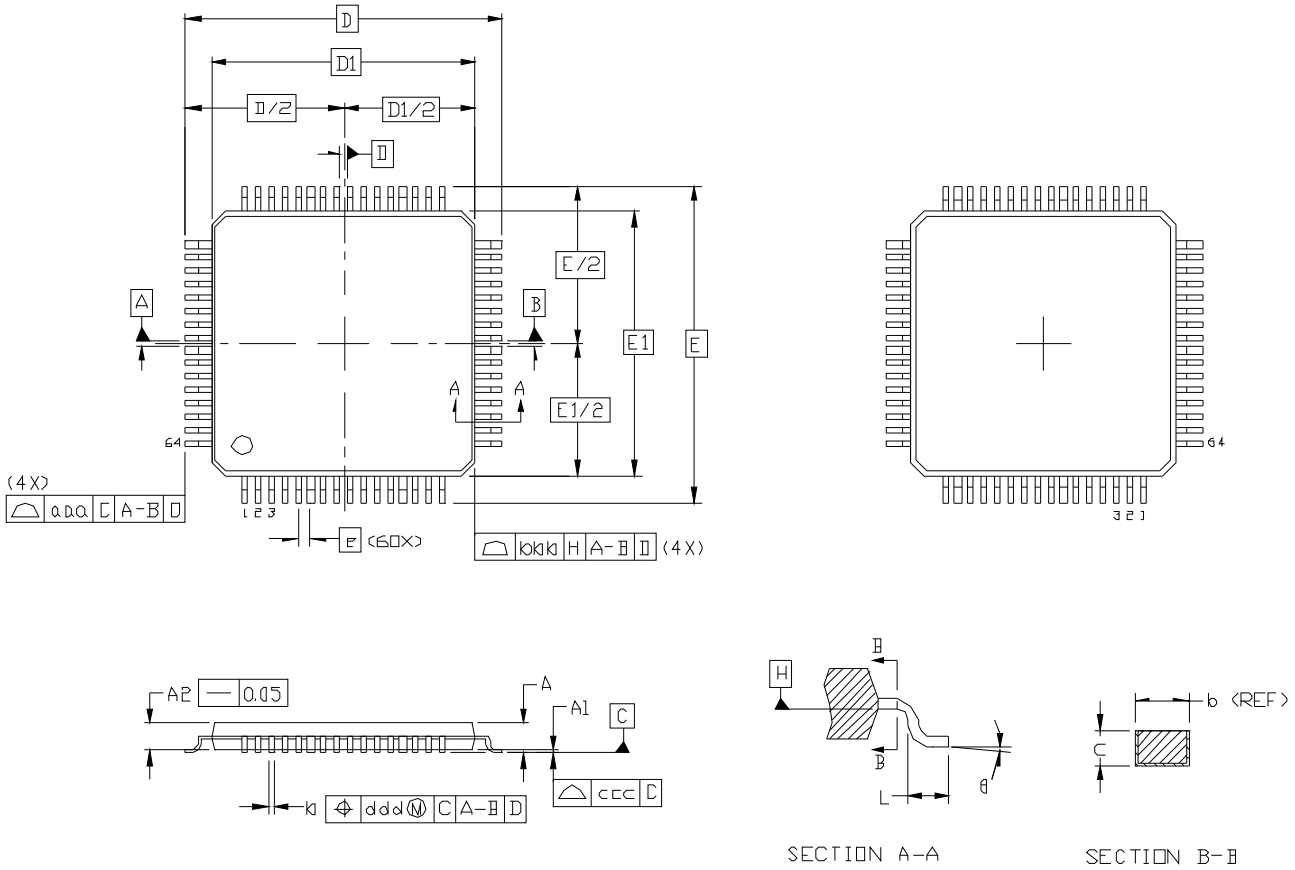


Figure 6.12. TQFP-64 Package Drawing

Table 6.10. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°

7. Revision Specific Behavior

This chapter details any known differences from behavior as stated in the device datasheet and reference manual. All known errata for the current silicon revision are rolled into this section at the time of publication. Any errata found after publication of this document will initially be detailed in a separate errata document until this datasheet is revised.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, 7.3, and 7.4 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

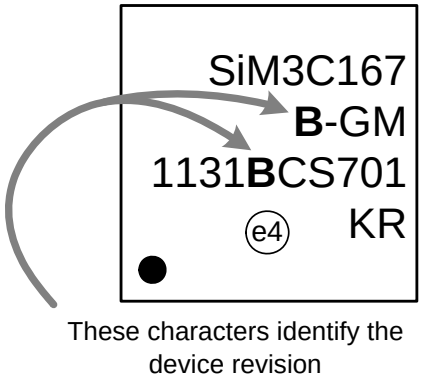


Figure 7.1. LGA-92 SiM3C1x7 Revision Information

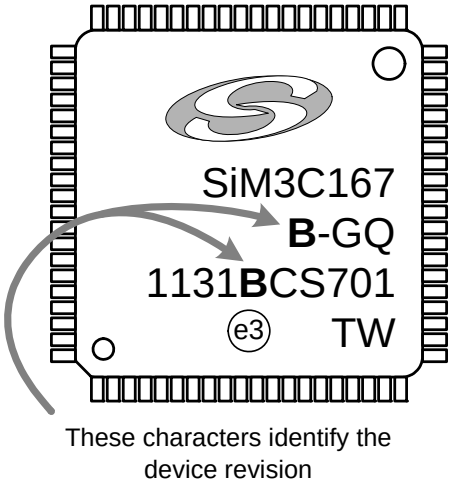
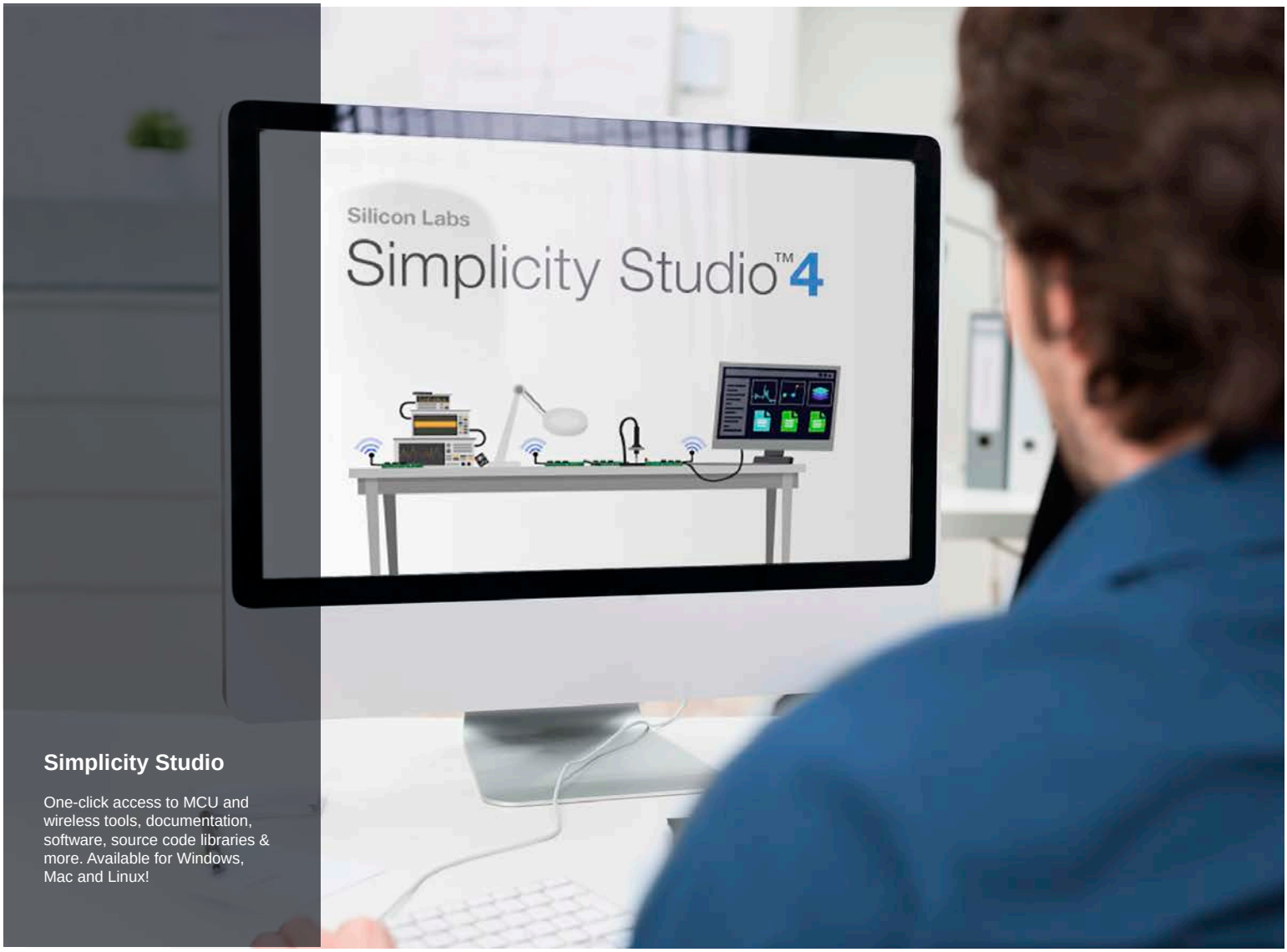


Figure 7.2. TQFP-80 SiM3C1x7 Revision Information



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