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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 32x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u157-b-gq

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	33	36.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	10.5	13.3	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	2.0	3.8	mA
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	22	24.9	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	10	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.2	3	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	30.5	35.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	8.5	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.7	—	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	20	23	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	5.3	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.0	—	mA
Power Mode 2[2,3,4]—Core halted with peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	19	22	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.3	—	mA
Power Mode 3[2,3]	I_{DD}	V_{DD} = 1.8 V, T_A = 25 °C	—	175	—	µA
		V_{DD} = 3.0 V, T_A = 25 °C	—	250	—	µA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Peripheral Supply Currents						
Voltage Regulator (VREG0)	I_{VREGIN}	Normal Mode, T_A = 25 °C BGDIS = 0, SUSEN = 0	—	300	—	µA
		Normal Mode, T_A = 85 °C BGDIS = 0, SUSEN = 0	—	—	650	µA
		Suspend Mode, T_A = 25 °C BGDIS = 0, SUSEN = 1	—	75	—	µA
		Suspend Mode, T_A = 85 °C BGDIS = 0, SUSEN = 1	—	—	115	µA
		Sleep Mode, T_A = 25 °C BGDIS = 1, SUSEN = X	—	90	—	nA
		Sleep Mode, T_A = 85 °C BGDIS = 1, SUSEN = X	—	—	500	nA
Voltage Regulator (VREG0) Sense	$I_{VRSENSE}$	SENSEEN = 1	—	3	—	µA
External Regulator (EXTVREG0)	$I_{EXTVREG}$	Regulator	—	215	250	µA
		Current Sensor	—	7	—	µA
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 80 MHz	—	1.75	1.86	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	190	—	µA
		Operating at 2.5 MHz	—	40	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz, T_A = 25 °C	—	215	—	nA
		Operating at 16.4 kHz, T_A = 85 °C	—	—	500	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.11. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{DD} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range	2.0	2.046	2.10	mA
		1 mA Range	0.99	1.023	1.05	mA
		0.5 mA Range	493	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VDD Power Supply Rejection Ratio		2 mA Range	—	-220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Table 3.12. Capacitive Sense

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single Conversion Time (Default Configuration)	t_{single}	12-bit Mode	—	25	—	µs
		13-bit Mode	—	27	—	µs
		14-bit Mode	—	29	—	µs
		16-bit Mode	—	33	—	µs
Maximum External Capacitive Load	C_L	Highest Gain Setting (default)	—	45	—	pF
		Lowest Gain Setting	—	500	—	pF
Maximum External Series Impedance	C_L	Highest Gain Setting (default)	—	50	—	kΩ

Table 3.13. Current-to-Voltage Converter (IVC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (VDD)	V_{DDIVC}		2.2	—	3.6	V
Input Pin Voltage	V_{IN}		2.2	—	VDD	V
Minimum Input Current (source)	I_{IN}		100	—	—	µA
Integral Nonlinearity	INL_{IVC}		–0.6	—	0.6	%
Full Scale Output	V_{IVCOUT}		—	1.65	—	V
Slope	M_{IVC}	Input Range 1 mA (INxRANGE = 101)	1.55	1.65	1.75	V/mA
		Input Range 2 mA (INxRANGE = 100)	795	830	860	mV/mA
		Input Range 3 mA (INxRANGE = 011)	525	550	570	mV/mA
		Input Range 4 mA (INxRANGE = 010)	390	415	430	mV/mA
		Input Range 5 mA (INxRANGE = 001)	315	330	340	mV/mA
		Input Range 6 mA (INxRANGE = 000)	260	275	285	mV/mA
Settling Time to 0.1%	V_{IVCOUT}		—	—	500	ns

Table 3.14. Voltage Reference Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{DD} = 1.8–3.6 V	1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-Chip Precision Reference (VREF0)						
Valid Supply Range	V_{DD}	VREF2X = 0	1.8	—	3.6	V
		VREF2X = 1	2.7	—	3.6	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.195	1.2	1.205	V
		25 °C ambient, VREF2X = 1	2.39	2.4	2.41	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	25	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 3.16. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.4	—	mV
		CMPHYP = 01	—	4	—	mV
		CMPHYP = 10	—	8	—	mV
		CMPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.4	—	mV
		CMPHYN = 01	—	–4	—	mV
		CMPHYN = 10	—	–8	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}	PB2 Pins	—	7.5	—	pF
		PB3 Pins	—	10.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}		–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
P-Channel Source Current Limit (2.7 V ≤ VIOHD ≤ 6 V, V_{OH} = VIOHD – 0.8 V) See Figure 3.2	I_{SRCL}	Mode 0	—	0.8	—	mA
		Mode 1	—	1.25	—	
		Mode 2	—	1.75	—	
		Mode 3	—	2.5	—	
		Mode 4	—	3.5	—	
		Mode 5	—	4.75	—	
		Mode 6	—	7	—	
		Mode 7	—	9.5	—	
		Mode 8	—	14	—	
		Mode 9	—	18.75	—	
		Mode 10	—	28.25	—	
		Mode 11	—	37.5	—	
		Mode 12	—	56.25	—	
		Mode 13	—	75	—	
		Mode 14	—	112.5	—	
		Mode 15	—	150	—	
Total P-Channel Source Current on P4.0-P4.5 (DC)	I_{SRCLT}		—	—	400	mA
Pin Capacitance	C_{IO}		—	30	—	pF
Weak Pull-Up Current in Low Voltage Mode	I_{PU}	V_{IOHD} = 1.8 V	–6	–3.5	–2	µA
		V_{IOHD} = 3.6 V	–30	–20	–10	µA
Weak Pull-Up Current in High Voltage Mode	I_{PU}	V_{IOHD} = 2.7 V	–15	–10	–5	µA
		V_{IOHD} = 6 V	–30	–20	–10	µA
Input Leakage (Pullups off)	I_{LK}		–1	—	1	µA

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

Table 3.19. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Power Dissipation at T_A = 85 °C	P_D	LGA-92 Package	—	570	mW
		TQFP-80 Package	—	500	mW
		QFN-64 Package	—	800	mW
		TQFP-64 Package	—	650	mW
		QFN-40 Package	—	650	mW
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and RESET pins are powered from the IO supply voltage. The SiM3C1xx devices are available in 40-pin or 64-pin QFN, 64-pin or 80-pin TQFP, or 92-pin LGA packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

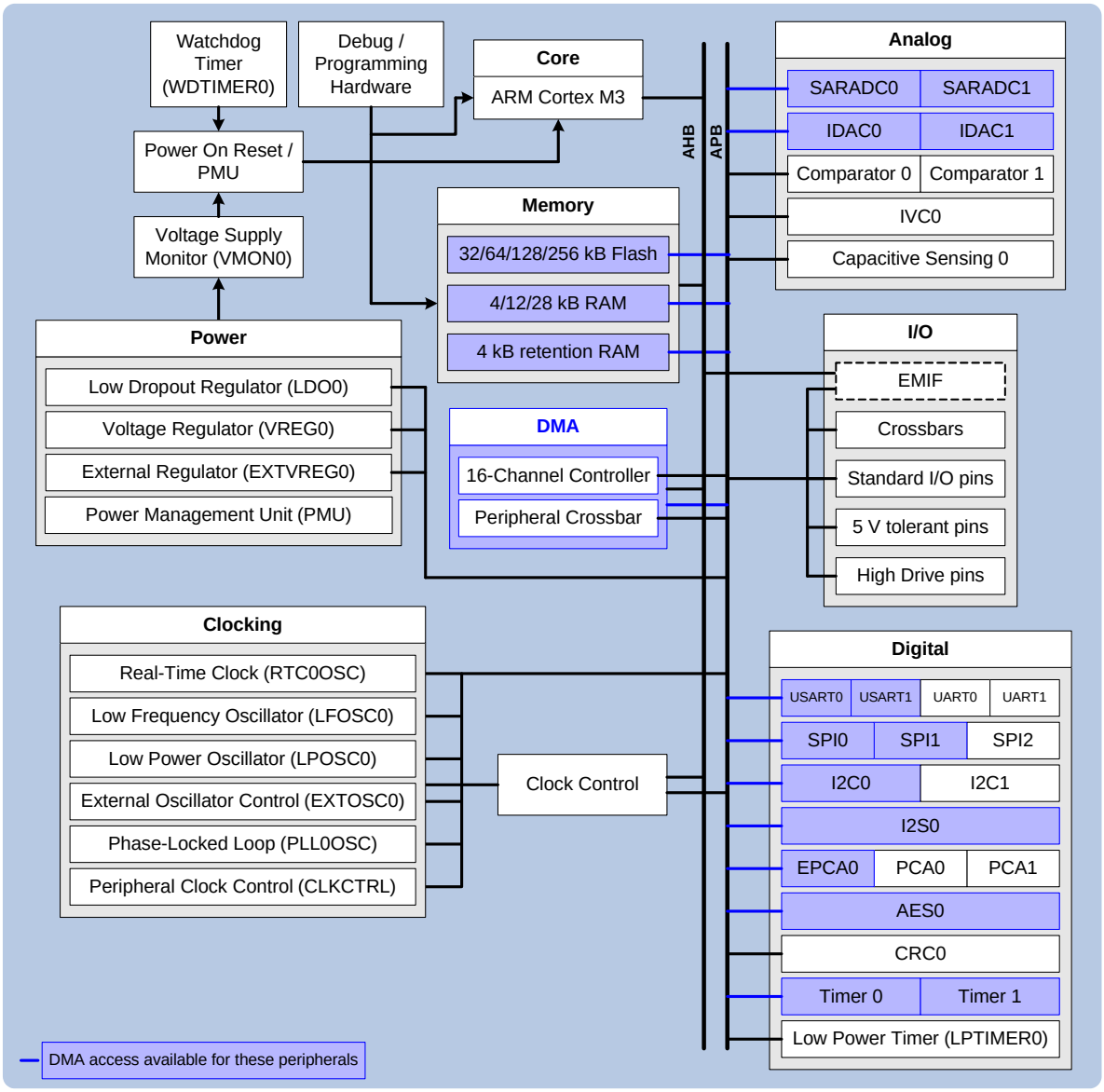

Figure 4.1. Precision32™ SiM3C1xx Family Block Diagram

4.1. Power

4.1.1. LDO and Voltage Regulator (VREG0)

The SiM3C1xx devices include two internal regulators: the core LDO Regulator and the Voltage Regulator (VREG0).

The LDO Regulator converts a 1.8–3.6 V supply to the core operating voltage of 1.8 V. This LDO consumes little power and provides flexibility in choosing a power supply for the system.

The Voltage Regulator regulates from 5.5 to 2.7 V and can serve as an input to the LDO. This allows the device to be powered from up to a 5.5 V supply without any external components other than bypass capacitors.

4.1.2. Voltage Supply Monitor (VMON0)

The SiM3C1xx devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware. The supply monitor includes additional circuitry that can monitor the main supply voltage and the VREGIN input voltage divided by 4 (VREGIN / 4).

The supply monitor module includes the following features:

- Main supply “VDD Low” (VDD below the early warning threshold) notification.
- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.
- VREGIN divided by 4 (VREGIN / 4) supply “VREGIN Low” notification.

4.1.3. External Regulator (EXTVREG0)

The External Regulator provides all the circuitry needed for a high-power regulator except the power transistor (NPN or PNP) and current sensing resistor (if current limiting is enabled).

The External Regulator module has the following features:

- Interfaces with either an NPN or PNP external transistor that serves as the pass device for the high current regulator.
- Automatic current limiting.
- Automatic foldback limiting.
- Sources up to 1 A for use by external circuitry.
- Variable output voltage from 1.8–3.6 V in 100 mV steps.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3C1xx manages the power systems of the device. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins. It also recognizes and manages the various wake sources for low-power modes of the device.

The PMU module includes the following features:

- Up to 16 pin wake inputs can wake the device from Power Mode 9.
- The Low Power Timer, RTC0 (alarms and oscillator fail), Comparator 0, and the $\overline{\text{RESET}}$ pin can also serve as wake sources for Power Mode 9.
- All PM9 wake sources (except for the $\overline{\text{RESET}}$ pin) can also reset the Low Power Timer or RTC0 modules.
- Disables the level shifters to pins and peripherals to further reduce power usage in PM9. These level shifters must be re-enabed by firmware after exiting PM9.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM9.

4.5. Counters/Timers and PWM

4.5.1. Programmable Counter Array (EPCA0, PCA0, PCA1)

The SiM3C1xx devices include two types of PCA module: Enhanced and Standard.

The Enhanced Programmable Counter Array (EPCA0) and Standard Programmable Counter Array (PCA0, PCA1) modules are timer/counter systems allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

The Enhanced PCA module is multi-purpose, but is optimized for motor control applications. The EPCA module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never both active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers and outputs.
- Pulse-Width Modulation (PWM) waveform generation.
- High-speed square wave generation.
- Input capture mode.
- DMA capability for both input capture and waveform generation.
- PWM generation halt input.

The Standard PCA module (PCA) includes the following features:

- Two independent channels.
- Center- and edge-aligned waveform generation.
- Programmable clock divisor and multiple options for clock source selection.
- Pulse-Width Modulation waveform generation.

4.5.2. 32-bit Timer (TIMER0, TIMER1)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.
- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB2.6	Standard I/O	29	B13	XBR1	✓	AD11m/ A3		Yes	INT0.6 INT1.6	
PB2.7	Standard I/O	28	A17	XBR1	✓	AD10m/ A2		Yes	INT0.7 INT1.7	
PB2.8	Standard I/O	27	B12	XBR1	✓	AD9m/ A1		Yes		
PB2.9	Standard I/O	26	A16	XBR1	✓	AD8m/ A0		Yes		
PB2.10	Standard I/O	25	B11	XBR1	✓	AD7m/ D7		Yes		
PB2.11	Standard I/O	24	A15	XBR1	✓	AD6m/ D6		Yes		CMP0P.0 CMP1P.0
PB2.12	Standard I/O	23	A14	XBR1	✓	AD5m/ D5		Yes		CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.13	Standard I/O	22	A13	XBR1	✓	AD4m/ D4		Yes		CMP0P.1 CMP1P.1
PB2.14	Standard I/O	21	D2	XBR1	✓	AD3m/ D3		Yes		CMP0N.1 CMP1N.1
PB3.0	5 V Tolerant I/O	20	A12	XBR1	✓	AD2m/ D2				CMP0P.2 CMP1P.2
PB3.1	5 V Tolerant I/O	19	A11	XBR1	✓	AD1m/ D1				CMP0N.2 CMP1N.2
PB3.2	5 V Tolerant I/O	18	A10	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0	CMP0P.3 CMP1P.3
PB3.3	5 V Tolerant I/O	17	B8	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.8 INT1.8	CMP0N.3 CMP1N.3

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.7	Standard I/O	50	XBR0	✓					RTC2
PB0.8	Standard I/O	49	XBR0	✓					ADC0.9 VREFGND
PB0.9	Standard I/O	48	XBR0	✓					ADC0.10 VREF
PB0.10	Standard I/O	47	XBR0	✓					ADC1.6 IDAC0
PB0.11	Standard I/O	46	XBR0	✓					IDAC1
PB0.12	Standard I/O	45	XBR0	✓					XTAL1
PB0.13	Standard I/O	44	XBR0	✓					XTAL2
PB0.14/TDO/ SWV	Standard I/O / JTAG / Serial Wire Viewer	43	XBR0	✓					ADC0.12 ADC1.12
PB0.15/TDI	Standard I/O / JTAG	42	XBR0	✓					ADC0.13 ADC1.13
PB1.0	Standard I/O	41	XBR0	✓					ADC0.14 ADC1.14
PB1.1	Standard I/O	40	XBR0	✓					ADC0.15 ADC1.15
PB1.2	Standard I/O	38	XBR0	✓					ADC1.11 CS0.8
PB1.3	Standard I/O	37	XBR0	✓					ADC1.10 CS0.9
PB1.4	Standard I/O	34	XBR0	✓					ADC1.8
PB1.5	Standard I/O	33	XBR0	✓					ADC1.7
PB1.6	Standard I/O	32	XBR0	✓				ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.7	Standard I/O	31	XBR0	✓	AD15m/ A7			ADC1T15 WAKE.1	ADC1.4 CS0.11

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.2	5 V Tolerant I/O	14	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0 WAKE.8	CMP0P.2 CMP1P.2
PB3.3	5 V Tolerant I/O	13	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.4 INT1.4 WAKE.9	CMP0N.2 CMP1N.2
PB3.4	5 V Tolerant I/O	12	XBR1	✓	$\overline{OE}$			INT0.5 INT1.5 WAKE.10	CMP0P.3 CMP1P.3
PB3.5	5 V Tolerant I/O	11	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.6 INT1.6 WAKE.11	CMP0N.3 CMP1N.3
PB3.6	5 V Tolerant I/O	10	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.7 INT1.7 WAKE.12	CMP0P.4 CMP1P.4 EXREGSP
PB3.7	5 V Tolerant I/O	9	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 INT0.8 INT1.8 WAKE.13	CMP0N.4 CMP1N.4 EXREGSN
PB3.8	5 V Tolerant I/O	8	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T1 INT0.9 INT1.9 WAKE.14	CMP0P.5 CMP1P.5 EXREGOUT

6.3. SiM3C1x4 Pin Definitions

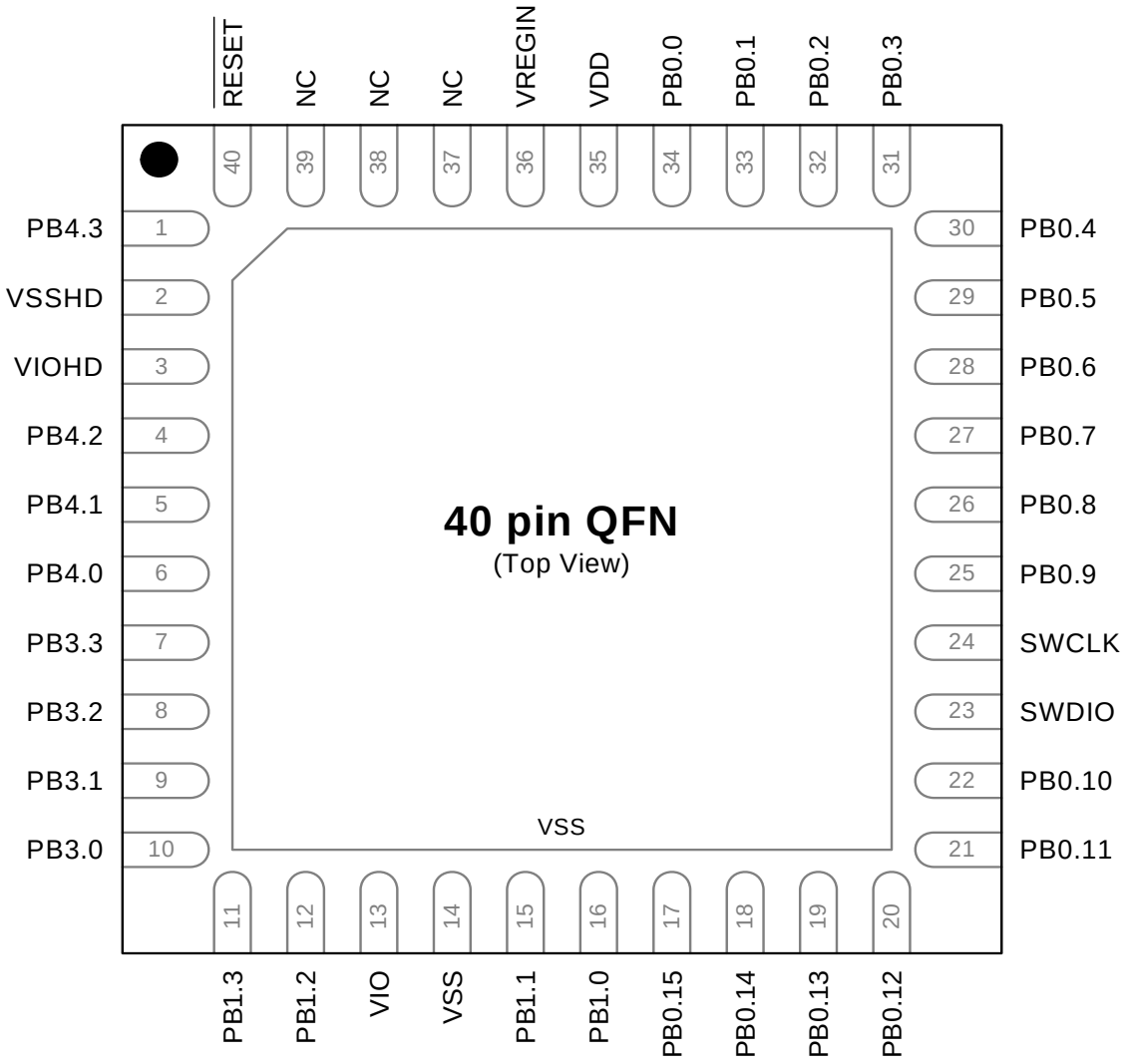

Figure 6.5. SiM3C1x4-GM Pinout

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	26	XBR0	✓			ADC0.14 ADC1.14
PB0.9	Standard I/O	25	XBR0	✓			ADC0.15 ADC1.15
PB0.10	Standard I/O	22	XBR0	✓		DMA0T1	ADC1.8
PB0.11	Standard I/O	21	XBR0	✓		DMA0T0	ADC1.7
PB0.12	Standard I/O	20	XBR0	✓		ADC0T15 WAKE.0	ADC1.5 CS0.10
PB0.13	Standard I/O	19	XBR0	✓		ADC1T15 WAKE.1	ADC1.4 CS0.11
PB0.14	Standard I/O	18	XBR0	✓		WAKE.2	ADC1.3 CS0.12
PB0.15	Standard I/O	17	XBR0	✓		WAKE.3	ADC1.2 CS0.13
PB1.0	Standard I/O	16	XBR0	✓		WAKE.4	ADC1.1 CS0.14
PB1.1	Standard I/O	15	XBR0	✓		WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.2	Standard I/O	12	XBR0	✓			CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB1.3	Standard I/O	11	XBR0	✓			CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	10	XBR1	✓		DAC0T0 DAC1T0 LPT0T0 INT0.0 INT1.0 WAKE.12	CMP0P.1 CMP1P.1 EXREGSP

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.1	5 V Tolerant I/O	9	XBR1	✓		DAC0T1 DAC1T1 LPT0T1 INT0.1 INT1.1 WAKE.13	CMP0N.1 CMP1N.1 EXREGSN
PB3.2	5 V Tolerant I/O	8	XBR1	✓		DAC0T2 DAC1T2 LPT0T2 INT0.2 INT1.3 WAKE.14	CMP0P.2 CMP1P.2 EXREGOUT
PB3.3	5 V Tolerant I/O	7	XBR1	✓		DAC0T3 DAC1T3 INT0.3 INT1.3 WAKE.15	CMP0N.2 CMP1N.2 EXREGBD
PB4.0	High Drive I/O	6					
PB4.1	High Drive I/O	5					
PB4.2	High Drive I/O	4					
PB4.3	High Drive I/O	1					

Table 6.10. TQFP-64 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.8. QFN-40 Package Specifications

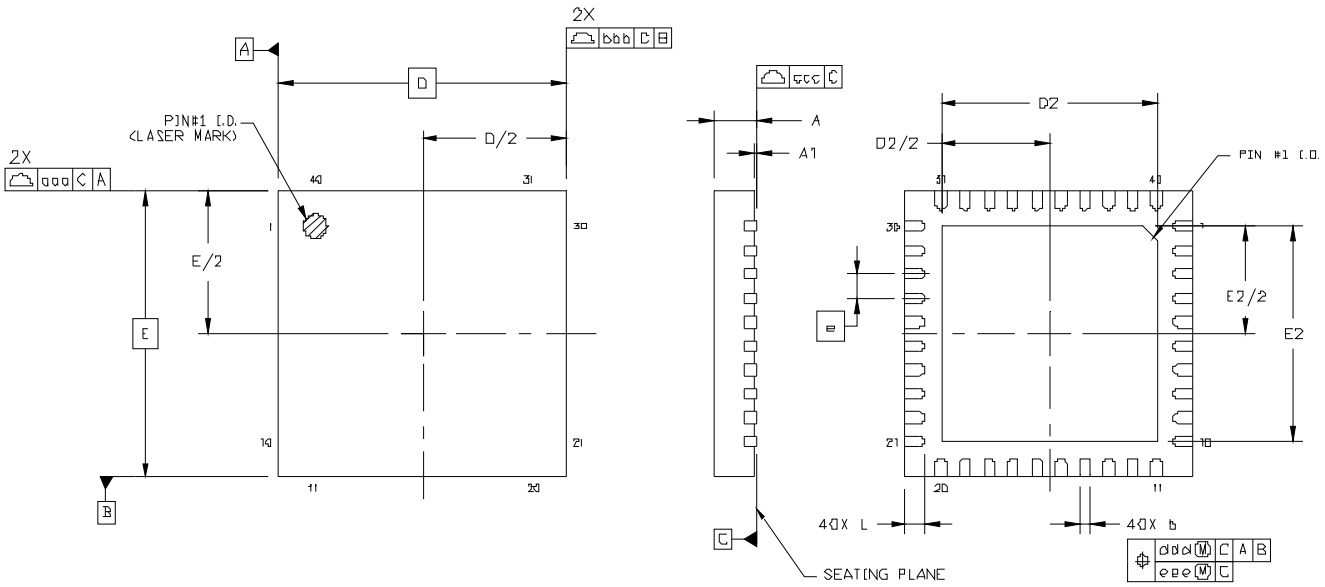

Figure 6.14. QFN-40 Package Drawing

Table 6.12. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.