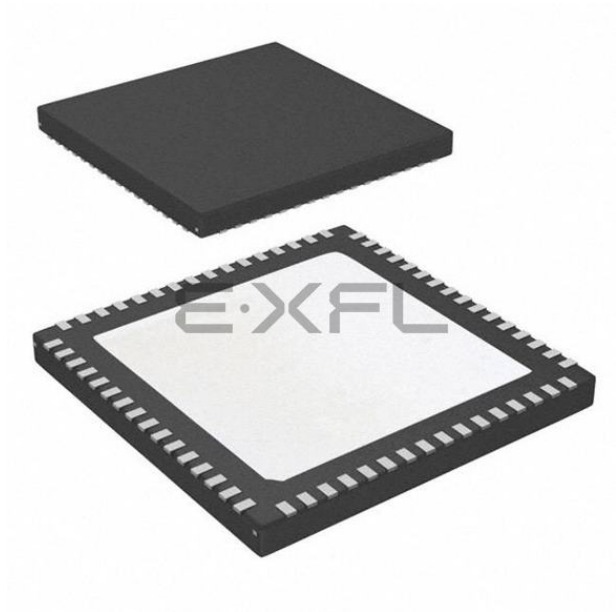


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u166-b-gmr

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	33	36.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	10.5	13.3	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	2.0	3.8	mA
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	22	24.9	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	10	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.2	3	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	30.5	35.5	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	8.5	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.7	—	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	20	23	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	5.3	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.0	—	mA
Power Mode 2[2,3,4]—Core halted with peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	19	22	mA
		$F_{AHB} = F_{APB}$ = 20 MHz	—	7.8	—	mA
		$F_{AHB} = F_{APB}$ = 2.5 MHz	—	1.3	—	mA
Power Mode 3[2,3]	I_{DD}	V_{DD} = 1.8 V, T_A = 25 °C	—	175	—	µA
		V_{DD} = 3.0 V, T_A = 25 °C	—	250	—	µA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 9[2,3]—Low Power Shutdown with VREG0 disabled, powered through VDD and VIO	I_{DD}	RTC Disabled, V_{DD} = 1.8 V, T_A = 25 °C	—	85	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 1.8 V, T_A = 25 °C	—	350	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 1.8 V, T_A = 25 °C	—	620	—	nA
		RTC Disabled, V_{DD} = 3.0 V, T_A = 25 °C	—	145	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 3.0 V, T_A = 25 °C	—	500	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 3.0 V, T_A = 25 °C	—	800	—	nA
Power Mode 9[2,3]—Low Power Shutdown with VREG0 in low-power mode, VDD and VIO powered through VREG0 (Includes VREG0 current)	I_{VREGIN}	RTC Disabled, VREGIN = 5 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, VREGIN = 5 V, T_A = 25 °C	—	650	—	nA
		RTC w/ 32.768 kHz Crystal, VREGIN = 5 V, T_A = 25 °C	—	950	—	nA
VIOHD Current (High-drive I/O disabled)	I_{VIOHD}	HV Mode (default)	—	2.5	5	µA
		LV Mode	—	2	—	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.7. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
V_{DD} Voltage During Programming	V_{PROG}		1.8	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During a sequential write operation, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 3.8. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency*	$f_{PLL0OSC}$	Full Temperature and Supply Range	77	79	80	MHz
Power Supply Sensitivity*	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 79 MHz	—	430	—	ppm/V
Temperature Sensitivity*	$TS_{PLL0OSC}$	V_{DD} = 3.3 V, Fout = 79 MHz	—	95	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	80	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 80 MHz, M=24, N=99, LOCKTH = 0	—	1.7	—	µs
		f_{REF} = 32 kHz, $f_{PLL0OSC}$ = 80 MHz, M=0, N=2440, LOCKTH = 0	—	91	—	µs

***Note:** PLL0OSC in free-running oscillator mode.

Table 3.10. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VDD)	V_{ADC}	High Speed Mode	2.2	—	3.6	V
		Low Power Mode	1.8	—	3.6	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode[2]	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

Table 3.10. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode[2]	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF =2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF =2.4 V	–1	0	1	LSB
Offset Temperatue Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error[3]	E_M	12 Bit Mode	–0.07	–0.02	0.02	%
Dynamic Performance with 10 kHz Sine Wave Input 1 dB below full scale, Max throughput						
Signal-to-Noise	SNR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	78	—	dB
		10 Bit Mode	—	77	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

Table 3.15. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	760	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	±14	—	mV
Slope	M		—	2.8	—	mV/°C
Slope Error*	E_M		—	±120	—	µV/°C
Linearity			—	1	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
P-Channel Source Current Limit (2.7 V ≤ VIOHD ≤ 6 V, V_{OH} = VIOHD – 0.8 V) See Figure 3.2	I_{SRCL}	Mode 0	—	0.8	—	mA
		Mode 1	—	1.25	—	
		Mode 2	—	1.75	—	
		Mode 3	—	2.5	—	
		Mode 4	—	3.5	—	
		Mode 5	—	4.75	—	
		Mode 6	—	7	—	
		Mode 7	—	9.5	—	
		Mode 8	—	14	—	
		Mode 9	—	18.75	—	
		Mode 10	—	28.25	—	
		Mode 11	—	37.5	—	
		Mode 12	—	56.25	—	
		Mode 13	—	75	—	
		Mode 14	—	112.5	—	
		Mode 15	—	150	—	
Total P-Channel Source Current on P4.0-P4.5 (DC)	I_{SRCLT}		—	—	400	mA
Pin Capacitance	C_{IO}		—	30	—	pF
Weak Pull-Up Current in Low Voltage Mode	I_{PU}	V_{IOHD} = 1.8 V	–6	–3.5	–2	µA
		V_{IOHD} = 3.6 V	–30	–20	–10	µA
Weak Pull-Up Current in High Voltage Mode	I_{PU}	V_{IOHD} = 2.7 V	–15	–10	–5	µA
		V_{IOHD} = 6 V	–30	–20	–10	µA
Input Leakage (Pullups off)	I_{LK}		–1	—	1	µA

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

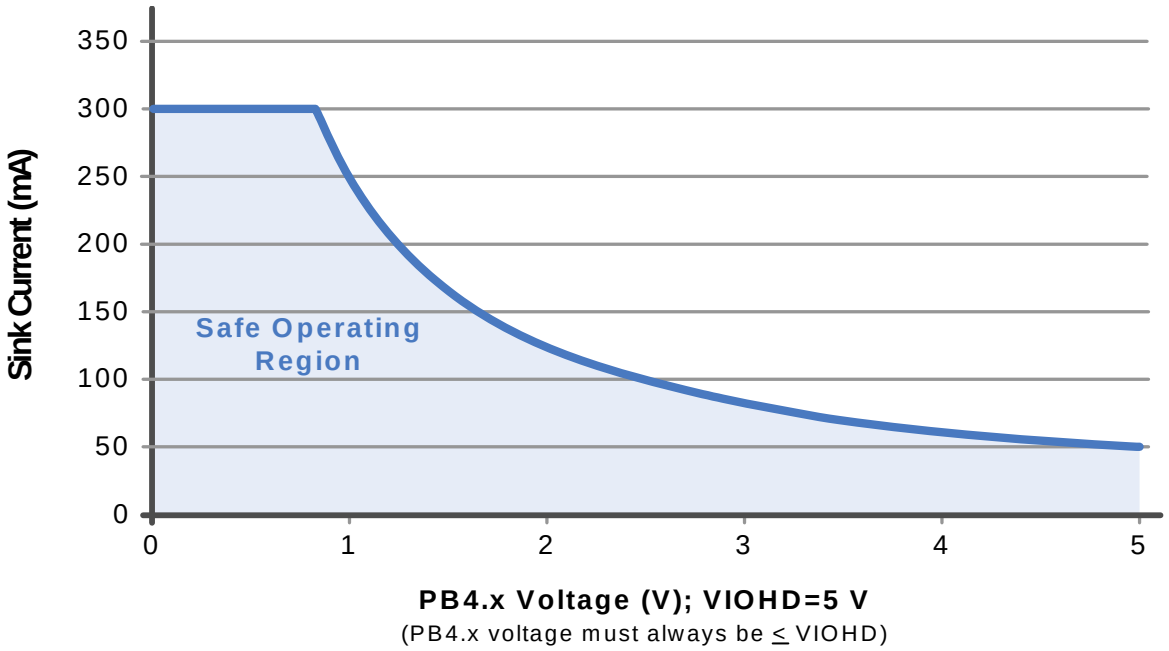


Figure 3.1. Maximum Sink Current vs. PB4.x Pin Voltage

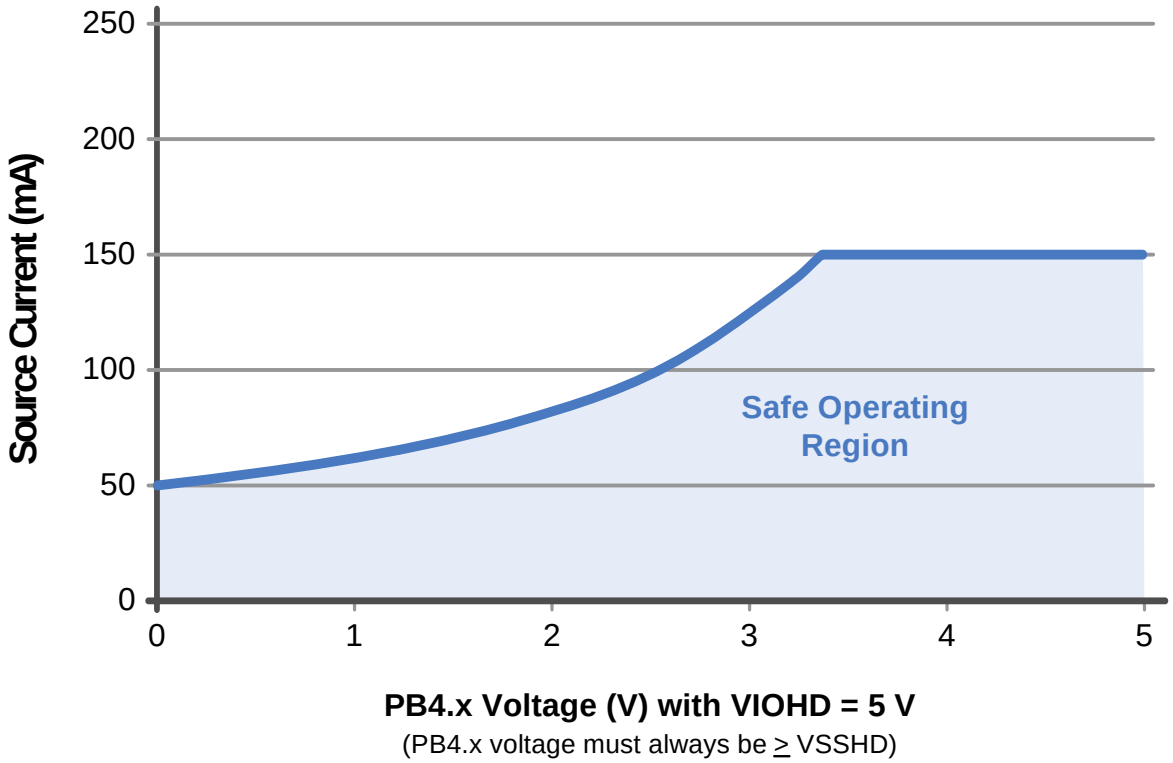


Figure 3.2. Maximum Source Current vs. PB4.x Pin Voltage

volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and RESET pins are powered from the IO supply voltage. The SiM3C1xx devices are available in 40-pin or 64-pin QFN, 64-pin or 80-pin TQFP, or 92-pin LGA packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

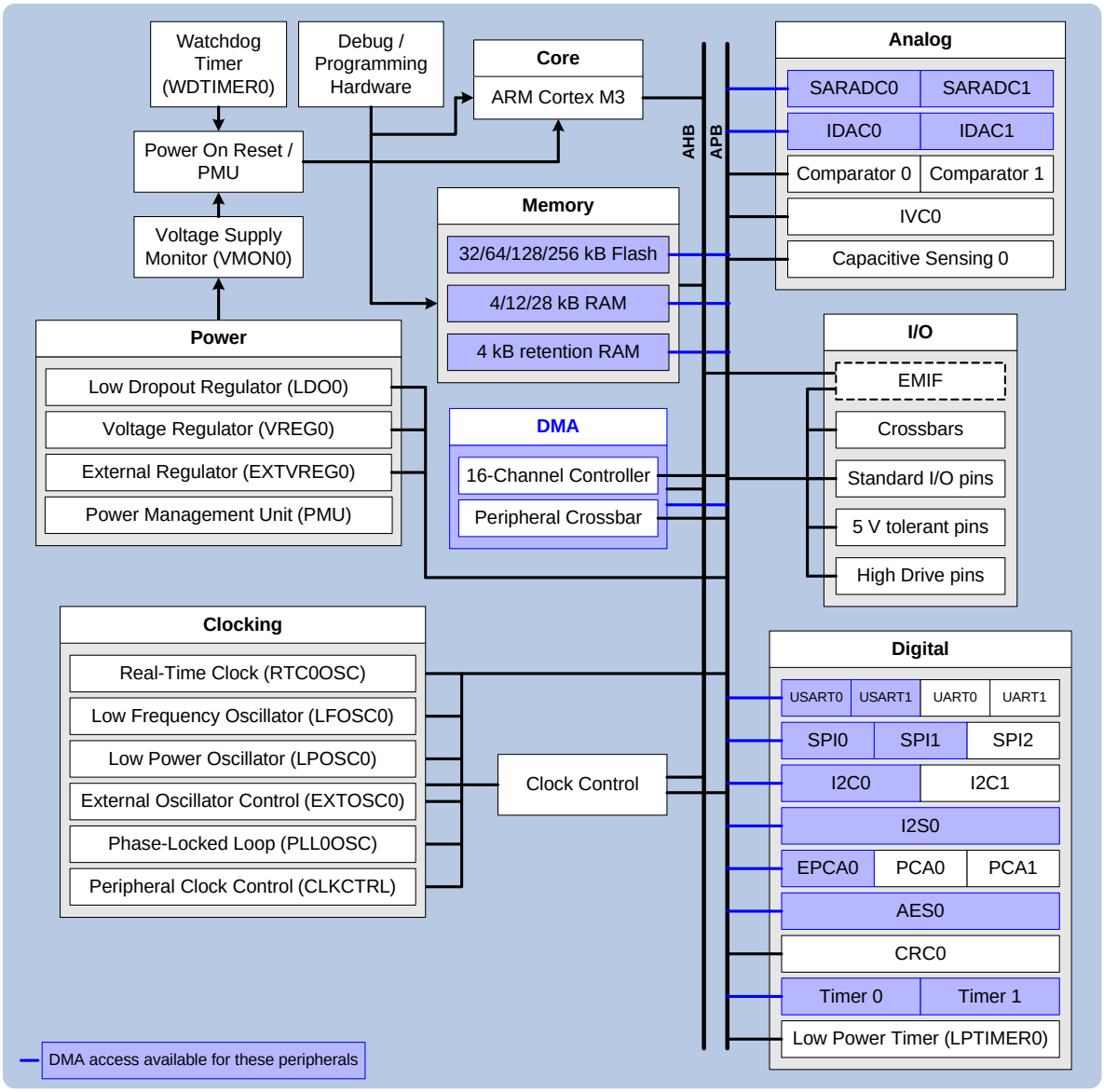
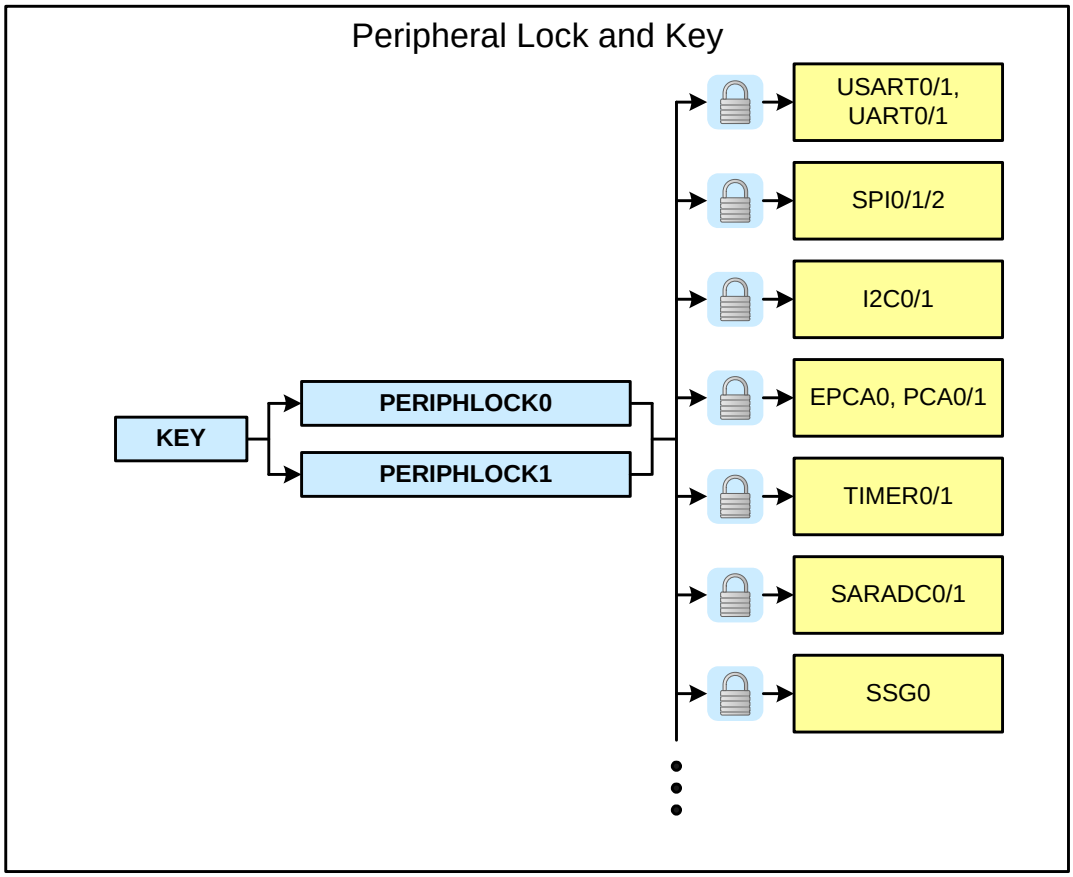


Figure 4.1. Precision32™ SiM3C1xx Family Block Diagram

4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.



4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabiites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.9/ TRACECLK	Standard I/O /ETM	46	A28	XBR0	✓					ADC1.9
PB1.10	Standard I/O	43	A26	XBR0	✓	A23m/ A15			DMA0T1	ADC1.8
PB1.11	Standard I/O	42	A25	XBR0	✓	A22m/ A14			DMA0T0	ADC1.7
PB1.12	Standard I/O	41	D3	XBR0	✓	A21m/ A13				ADC1.6
PB1.13	Standard I/O	40	A24	XBR0	✓	A20m/ A12			ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.14	Standard I/O	39	A23	XBR0	✓	A19m/ A11			ADC1T15 WAKE.1	ADC1.4 CS0.11
PB1.15	Standard I/O	38	A22	XBR0	✓	A18m/ A10			WAKE.2	ADC1.3 CS0.12
PB2.0	Standard I/O	37	B17	XBR1	✓	A17m/ A9	LSI0	Yes	INT0.0 INT1.0 WAKE.3	ADC1.2 CS0.13
PB2.1	Standard I/O	36	A21	XBR1	✓	A16m/ A8	LSI1	Yes	INT0.1 INT1.1 WAKE.4	ADC1.1 CS0.14
PB2.2	Standard I/O	35	B16	XBR1	✓	AD15m/ A7	LSI2	Yes	INT0.2 INT1.2 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB2.3	Standard I/O	34	A20	XBR1	✓	AD14m/ A6	LSI3	Yes	INT0.3 INT1.3 WAKE.6	
PB2.4	Standard I/O	31	B14	XBR1	✓	AD13m/ A5	LSI4	Yes	INT0.4 INT1.4 WAKE.7	
PB2.5	Standard I/O	30	A18	XBR1	✓	AD12m / A4	LSI5	Yes	INT0.5 INT1.5	

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.4	5 V Tolerant I/O	16	A9	XBR1	✓	$\overline{OE}$			INT0.9 INT1.9 WAKE.8	CMP0P.4 CMP1P.4
PB3.5	5 V Tolerant I/O	15	B7	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.10 INT1.10 WAKE.9	CMP0N.4 CMP1N.4
PB3.6	5 V Tolerant I/O	14	A8	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.11 INT1.11 WAKE.10	CMP0P.5 CMP1P.5
PB3.7	5 V Tolerant I/O	13	B6	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 LPT0T1 INT0.12 INT1.12 WAKE.11	CMP0N.5 CMP1N.5
PB3.8	5 V Tolerant I/O	12	A7	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T2 INT0.13 INT1.13 WAKE.12	CMP0P.6 CMP1P.6 EXREGSP
PB3.9	5 V Tolerant I/O	11	B5	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 INT0.14 INT1.14 WAKE.13	CMP0N.6 CMP1N.6 EXREGSN
PB3.10	5 V Tolerant I/O	10	B4	XBR1	✓				INT0.15 INT1.15 WAKE.14	CMP0P.7 CMP1P.7 EXREGOUT
PB3.11	5 V Tolerant I/O	9	B3	XBR1	✓				WAKE.15	CMP0N.7 CMP1N.7 EXREGBD

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB4.0	High Drive I/O	8	A6				LSO0			
PB4.1	High Drive I/O	7	A5				LSO1			
PB4.2	High Drive I/O	6	A4				LSO2			
PB4.3	High Drive I/O	3	A2				LSO3			
PB4.4	High Drive I/O	2	A1				LSO4			
PB4.5	High Drive I/O	1	D1				LSO5			

Note: All unnamed pins on the LGA-92 package are no-connect pins. They should be soldered to the PCB for mechanical stability, but have no internal connections to the device.

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.7	Standard I/O	50	XBR0	✓					RTC2
PB0.8	Standard I/O	49	XBR0	✓					ADC0.9 VREFGND
PB0.9	Standard I/O	48	XBR0	✓					ADC0.10 VREF
PB0.10	Standard I/O	47	XBR0	✓					ADC1.6 IDAC0
PB0.11	Standard I/O	46	XBR0	✓					IDAC1
PB0.12	Standard I/O	45	XBR0	✓					XTAL1
PB0.13	Standard I/O	44	XBR0	✓					XTAL2
PB0.14/TDO/ SWV	Standard I/O / JTAG / Serial Wire Viewer	43	XBR0	✓					ADC0.12 ADC1.12
PB0.15/TDI	Standard I/O / JTAG	42	XBR0	✓					ADC0.13 ADC1.13
PB1.0	Standard I/O	41	XBR0	✓					ADC0.14 ADC1.14
PB1.1	Standard I/O	40	XBR0	✓					ADC0.15 ADC1.15
PB1.2	Standard I/O	38	XBR0	✓					ADC1.11 CS0.8
PB1.3	Standard I/O	37	XBR0	✓					ADC1.10 CS0.9
PB1.4	Standard I/O	34	XBR0	✓					ADC1.8
PB1.5	Standard I/O	33	XBR0	✓					ADC1.7
PB1.6	Standard I/O	32	XBR0	✓				ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.7	Standard I/O	31	XBR0	✓	AD15m/ A7			ADC1T15 WAKE.1	ADC1.4 CS0.11

6.4. LGA-92 Package Specifications

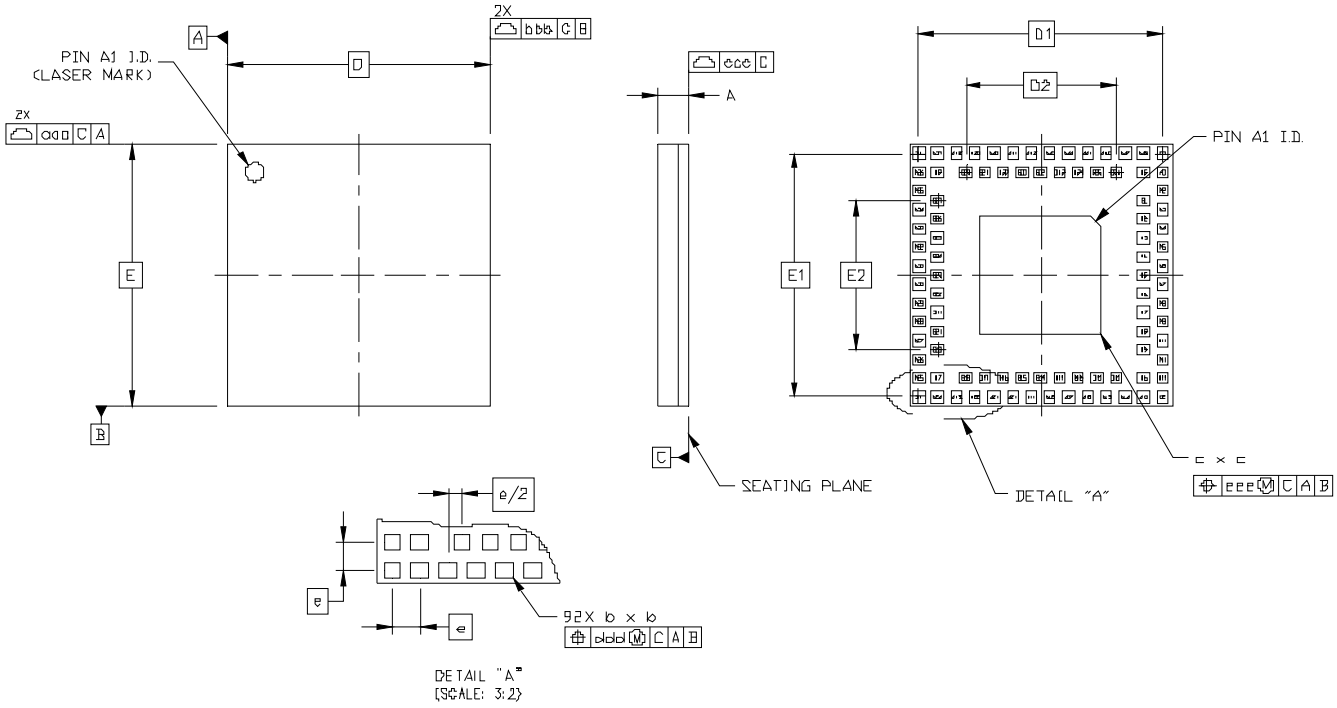


Figure 6.6. LGA-92 Package Drawing

Table 6.4. LGA-92 Package Dimensions

Dimension	Min	Nominal	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
c	3.15	3.20	3.25
D		7.00 BSC	
D1		6.50 BSC	
D2		4.00 BSC	
e		0.50 BSC	
E		7.00 BSC	
E1		6.50 BSC	
E2		4.00 BSC	
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

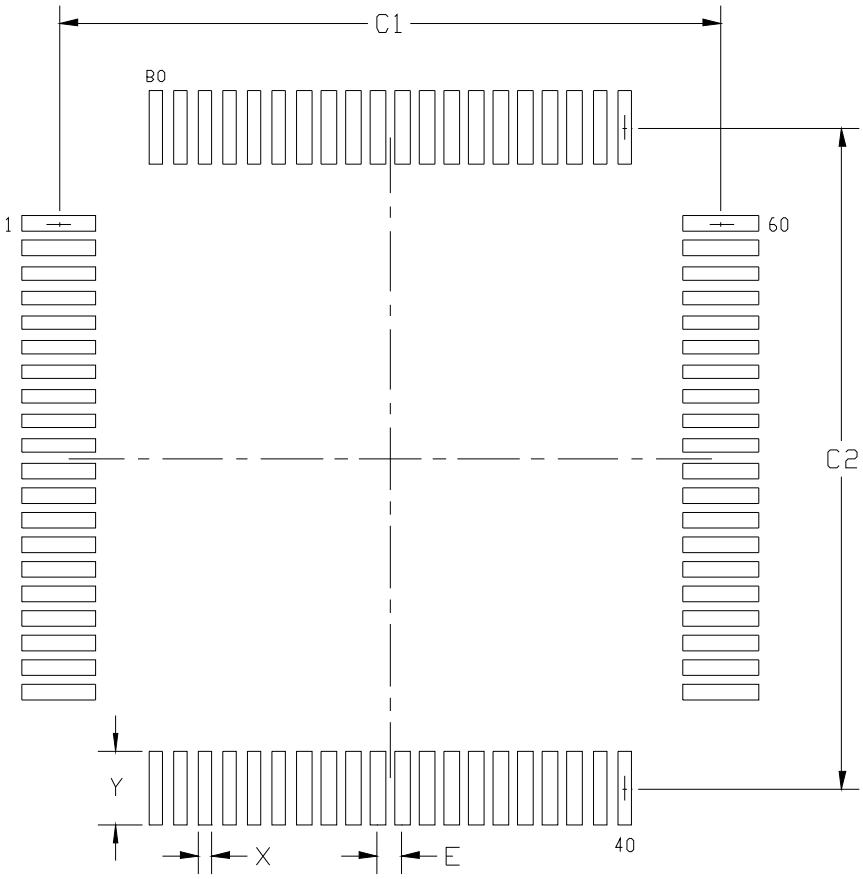


Figure 6.9. TQFP-80 Landing Diagram

Table 6.7. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.6. QFN-64 Package Specifications

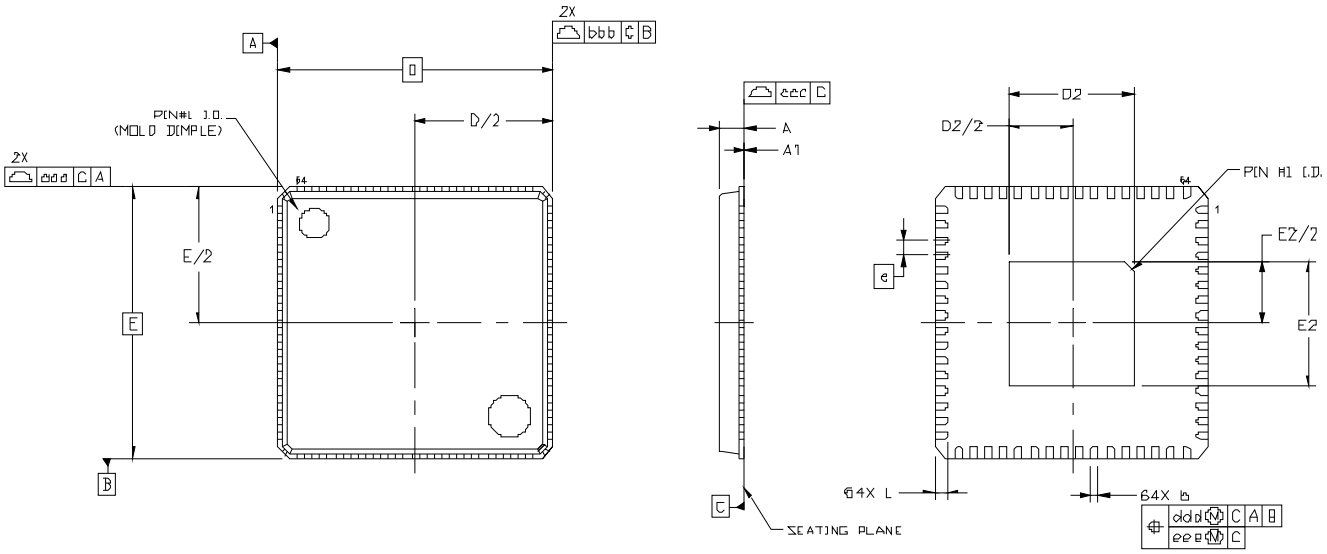


Figure 6.10. QFN-64 Package Drawing

Table 6.8. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

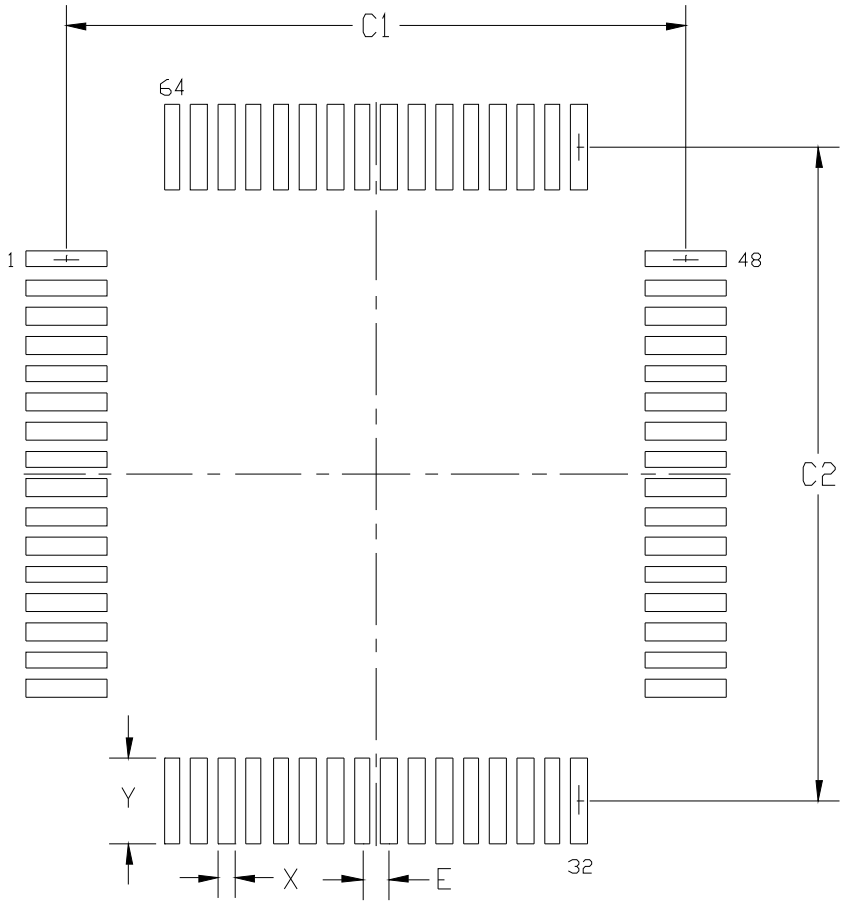


Figure 6.13. TQFP-64 Landing Diagram

Table 6.11. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.8. QFN-40 Package Specifications

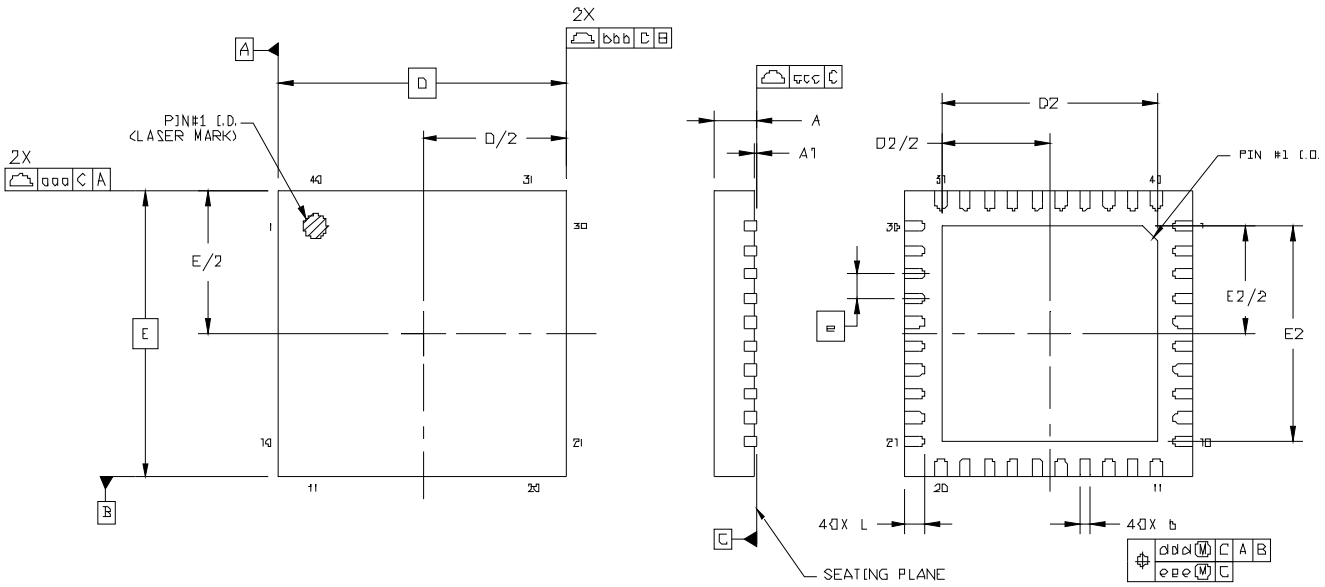


Figure 6.14. QFN-40 Package Drawing

Table 6.12. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.