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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 32x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3u167-b-gq

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 9[2,3]—Low Power Shutdown with VREG0 disabled, powered through VDD and VIO	I_{DD}	RTC Disabled, V_{DD} = 1.8 V, T_A = 25 °C	—	85	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 1.8 V, T_A = 25 °C	—	350	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 1.8 V, T_A = 25 °C	—	620	—	nA
		RTC Disabled, V_{DD} = 3.0 V, T_A = 25 °C	—	145	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 3.0 V, T_A = 25 °C	—	500	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 3.0 V, T_A = 25 °C	—	800	—	nA
Power Mode 9[2,3]—Low Power Shutdown with VREG0 in low-power mode, VDD and VIO powered through VREG0 (Includes VREG0 current)	I_{VREGIN}	RTC Disabled, VREGIN = 5 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, VREGIN = 5 V, T_A = 25 °C	—	650	—	nA
		RTC w/ 32.768 kHz Crystal, VREGIN = 5 V, T_A = 25 °C	—	950	—	nA
VIOHD Current (High-drive I/O disabled)	I_{VIOHD}	HV Mode (default)	—	2.5	5	µA
		LV Mode	—	2	—	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Peripheral Supply Currents						
Voltage Regulator (VREG0)	I_{VREGIN}	Normal Mode, T_A = 25 °C BGDIS = 0, SUSEN = 0	—	300	—	µA
		Normal Mode, T_A = 85 °C BGDIS = 0, SUSEN = 0	—	—	650	µA
		Suspend Mode, T_A = 25 °C BGDIS = 0, SUSEN = 1	—	75	—	µA
		Suspend Mode, T_A = 85 °C BGDIS = 0, SUSEN = 1	—	—	115	µA
		Sleep Mode, T_A = 25 °C BGDIS = 1, SUSEN = X	—	90	—	nA
		Sleep Mode, T_A = 85 °C BGDIS = 1, SUSEN = X	—	—	500	nA
Voltage Regulator (VREG0) Sense	$I_{VRSENSE}$	SENSEEN = 1	—	3	—	µA
External Regulator (EXTVREG0)	$I_{EXTVREG}$	Regulator	—	215	250	µA
		Current Sensor	—	7	—	µA
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 80 MHz	—	1.75	1.86	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	190	—	µA
		Operating at 2.5 MHz	—	40	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz, T_A = 25 °C	—	215	—	nA
		Operating at 16.4 kHz, T_A = 85 °C	—	—	500	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Regulator Characteristics (VREG0, Supplied from VREGIN Pin)						
Output Voltage (at VDD pin)	V_{DDOUT}	$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = 0	3.15	3.3	3.4	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = 1	3.15	3.3	3.4	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X I_{DDOUT} = 500 µA	2.3	2.8	3.6	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X I_{DDOUT} = 5 mA	2.1	2.65	3.3	V
Output Current (at VDD pin)*	I_{DDOUT}	$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = X	—	—	150	mA
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X	—	—	5	mA
Output Load Regulation	V_{DDLR}	BGDIS = 0	—	0.1	1	mV/mA
Output Capacitance	C_{VDD}		1	—	10	µF

***Note:** Total current VREG0 is capable of providing. Any current consumed by the SiM3C1xx reduces the current available to external devices powered from VDD.

Table 3.16. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.4	—	mV
		CMPHYP = 01	—	4	—	mV
		CMPHYP = 10	—	8	—	mV
		CMPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.4	—	mV
		CMPHYN = 01	—	–4	—	mV
		CMPHYN = 10	—	–8	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}	PB2 Pins	—	7.5	—	pF
		PB3 Pins	—	10.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}		–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

4.1.5. Device Power Modes

The SiM3C1xx devices feature four low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low-Power Timer (LPT0), RTC0 (alarms and oscillator failure notification), Comparator 0, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0)

Normal Mode is the default mode of the device. The core and peripherals are fully operational, and instructions are executed from flash memory.

4.1.5.2. Power Mode 1

In Power Mode 1 the core and peripherals are fully operational, with instructions executing from RAM. Compared with Normal Mode, the active power consumption of the device in PM1 is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAM does not require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2

In Power Mode 2 the core halts and any enabled peripherals continue to run at the selected clock speed. The power consumption in PM2 corresponds to the AHB and APB clocks left enabled, thus the power can be tuned to the optimal level for the needs of the application. To place the device in PM2, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0 with the DMACTRL0 AHB clock disabled, PM2 can achieve similar power consumption to PM3, but with the ability to wake on APB-clocked interrupts. For example, enabling only the APB clock to the Ports will allow the firmware to wake on a PMATCH0, PBEXT0 or PBEXT1 interrupt with minimal impact on the supply current.

4.1.5.4. Power Mode 3

In Power Mode 3, the AHB and APB clocks are halted. The device may only wake from enabled interrupt sources which do not require the APB clock (RTC0ALRM, RTC0FAIL, LPTIMER0, VDDLOW and VREGLOW). A special fast wake option allows the device to operate at a very low level from the RTC0TCLK or LFOSC0 oscillator while in PM3, but quickly switch to the faster LPOSC0 when the wake event occurs. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

The device will enter PM3 on a WFI or WFE instruction. Because all AHB master clocks are disabled, the LPOSC will automatically halt and go into a low-power suspended state. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 9

In Power Mode 9, the core and all peripherals are halted, all clocks are stopped, and the pins and peripherals are set to a lower power mode. In addition, standard RAM contents are not preserved, though retention RAM contents are still available after exiting the power mode. This mode provides the lowest power consumption for the device, but requires an appropriate reset to exit. The available reset sources to wake from PM9 are controlled by the Power Management Unit (PMU).

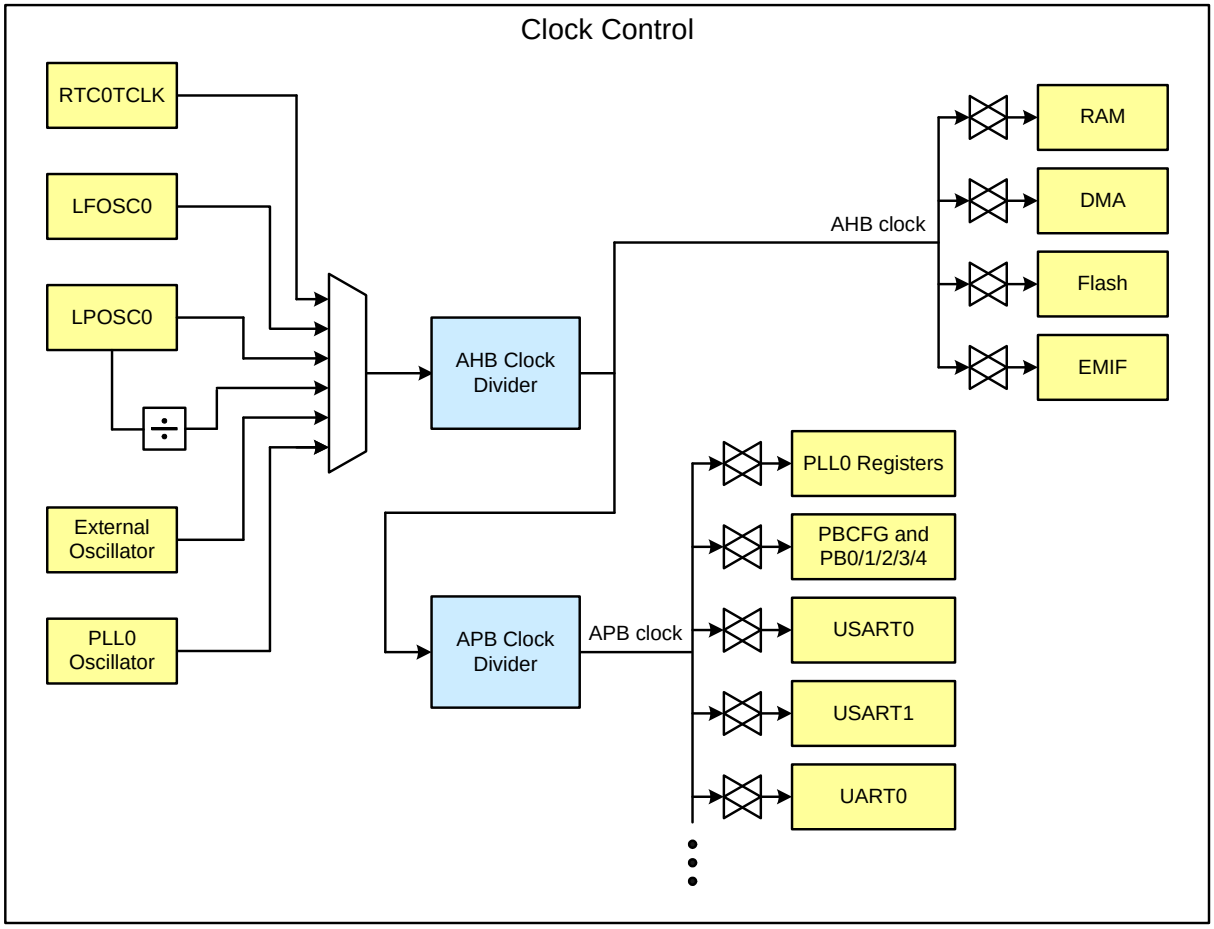
Before entering PM9, the desired reset source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the RSTSRC0_CONFIG register must be set to indicate that PM9 is the desired power mode.

The device will enter PM9 on a WFI or WFE instruction, and remain in PM9 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.



4.5. Counters/Timers and PWM

4.5.1. Programmable Counter Array (EPCA0, PCA0, PCA1)

The SiM3C1xx devices include two types of PCA module: Enhanced and Standard.

The Enhanced Programmable Counter Array (EPCA0) and Standard Programmable Counter Array (PCA0, PCA1) modules are timer/counter systems allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

The Enhanced PCA module is multi-purpose, but is optimized for motor control applications. The EPCA module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never both active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers and outputs.
- Pulse-Width Modulation (PWM) waveform generation.
- High-speed square wave generation.
- Input capture mode.
- DMA capability for both input capture and waveform generation.
- PWM generation halt input.

The Standard PCA module (PCA) includes the following features:

- Two independent channels.
- Center- and edge-aligned waveform generation.
- Programmable clock divisor and multiple options for clock source selection.
- Pulse-Width Modulation waveform generation.

4.5.2. 32-bit Timer (TIMER0, TIMER1)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.
- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

- Spike suppression up to 2 times the APB period.

4.6.6. I²S (I2S0)

The I²S module receives digital data from an external source over a data line in the standard I²S, left-justified, right-justified, or time domain multiplexing format, de-serializes the data, and generates requests to transfer the data using the DMA. The module also reads stereo audio samples from the DMA, serializes the data, and sends it out of the chip on a data line in the same standard serial format for digital audio. The I²S receive interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync), and SD (data input). The block's transmit interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync) and SD (data output).

The I²S module includes the following features:

- Master or slave capability.
- Flexible 10-bit clock divider with 8-bit fractional clock divider provides support for various common sampling frequencies (16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz) for up to two 32-bit channels.
- Support for DMA data transfers.
- Support for various data formats.
- Time Division Multiplexing

4.7. Analog

4.7.1. 12-Bit Analog-to-Digital Converters (SARADC0, SARADC1)

The SARADC0 and SARADC1 modules on SiM3C1xx devices are Successive Approximation Register (SAR) Analog to Digital Converters (ADCs). The key features of the SARADC module are:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- Output data window comparator allows automatic range checking.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to 8 sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Multiple SARADC modules can work together synchronously or by interleaving samples.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.7.2. Sample Sync Generator (SSG0)

The SSG module includes a phase counter and a pulse generator. The phase counter is a 4-bit free-running counter clocked from the SARADC module clock. Counting-up from zero, the phase counter marks sixteen equally-spaced events for any number of SARADC modules. The ADCs can use this phase counter to start a conversion. The programmable pulse generator creates a 50% duty cycle pulse with a period of 16 phase counter ticks. Up to four programmable outputs available to external devices can be driven by the pulse generator with programmable polarity and a defined output setting when the pulse generator is stopped.

The Sample Sync Generator module has the following features:

- Connects multiple modules together to perform synchronized actions.
- Outputs a clock synchronized to the internal sampling clock used by any number of SARADC modules to pins for use by external devices.
- Includes a phase counter, pulse generator, and up to four programmable outputs.

4.7.3. 10-Bit Digital-to-Analog Converter (IDAC0, IDAC1)

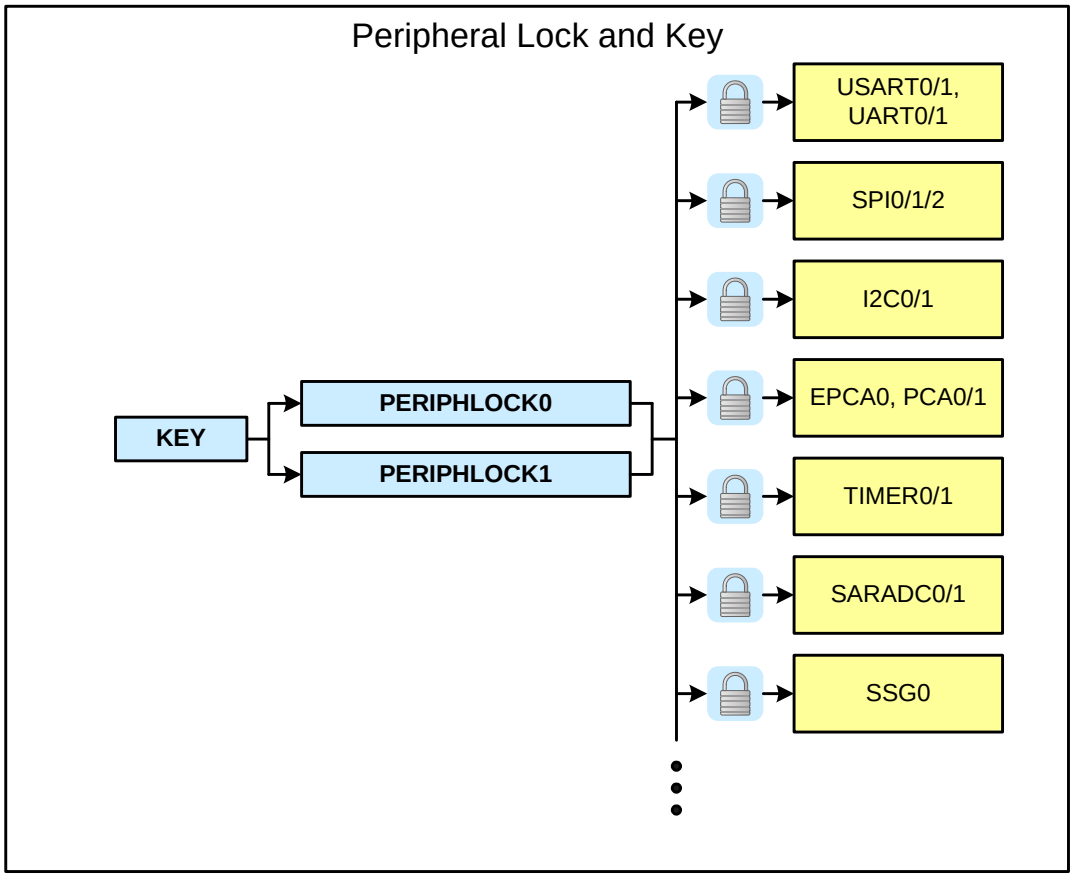
The IDAC takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O, on demand, and SSG0 output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources (DACnTx).
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.



4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabiites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.

5. Ordering Information

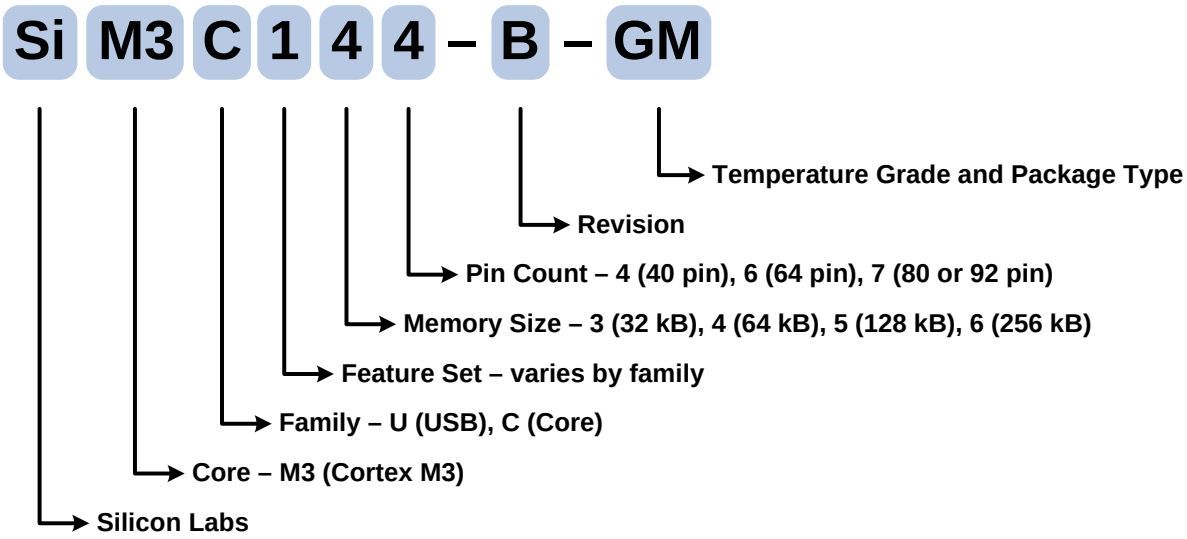


Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I^2S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	26	XBR0	✓			ADC0.14 ADC1.14
PB0.9	Standard I/O	25	XBR0	✓			ADC0.15 ADC1.15
PB0.10	Standard I/O	22	XBR0	✓		DMA0T1	ADC1.8
PB0.11	Standard I/O	21	XBR0	✓		DMA0T0	ADC1.7
PB0.12	Standard I/O	20	XBR0	✓		ADC0T15 WAKE.0	ADC1.5 CS0.10
PB0.13	Standard I/O	19	XBR0	✓		ADC1T15 WAKE.1	ADC1.4 CS0.11
PB0.14	Standard I/O	18	XBR0	✓		WAKE.2	ADC1.3 CS0.12
PB0.15	Standard I/O	17	XBR0	✓		WAKE.3	ADC1.2 CS0.13
PB1.0	Standard I/O	16	XBR0	✓		WAKE.4	ADC1.1 CS0.14
PB1.1	Standard I/O	15	XBR0	✓		WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.2	Standard I/O	12	XBR0	✓			CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB1.3	Standard I/O	11	XBR0	✓			CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	10	XBR1	✓		DAC0T0 DAC1T0 LPT0T0 INT0.0 INT1.0 WAKE.12	CMP0P.1 CMP1P.1 EXREGSP

6.4. LGA-92 Package Specifications

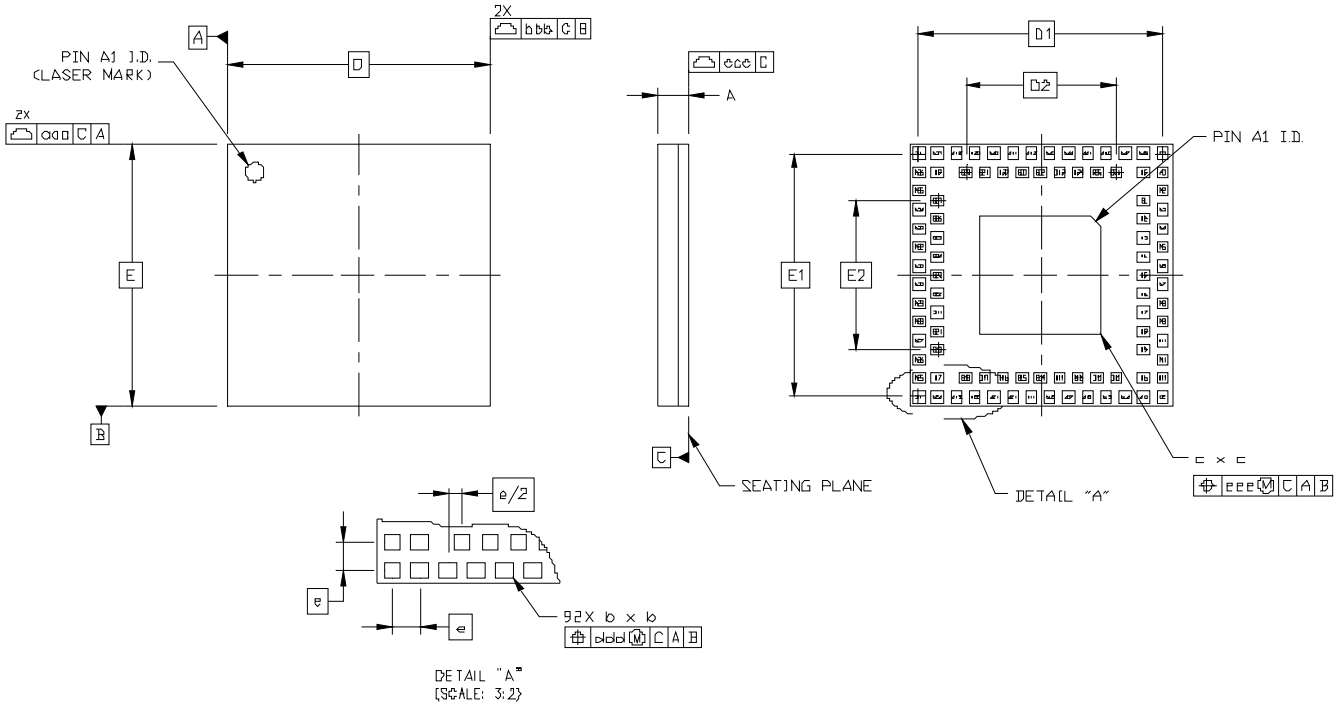


Figure 6.6. LGA-92 Package Drawing

Table 6.4. LGA-92 Package Dimensions

Dimension	Min	Nominal	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
c	3.15	3.20	3.25
D		7.00 BSC	
D1		6.50 BSC	
D2		4.00 BSC	
e		0.50 BSC	
E		7.00 BSC	
E1		6.50 BSC	
E2		4.00 BSC	
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

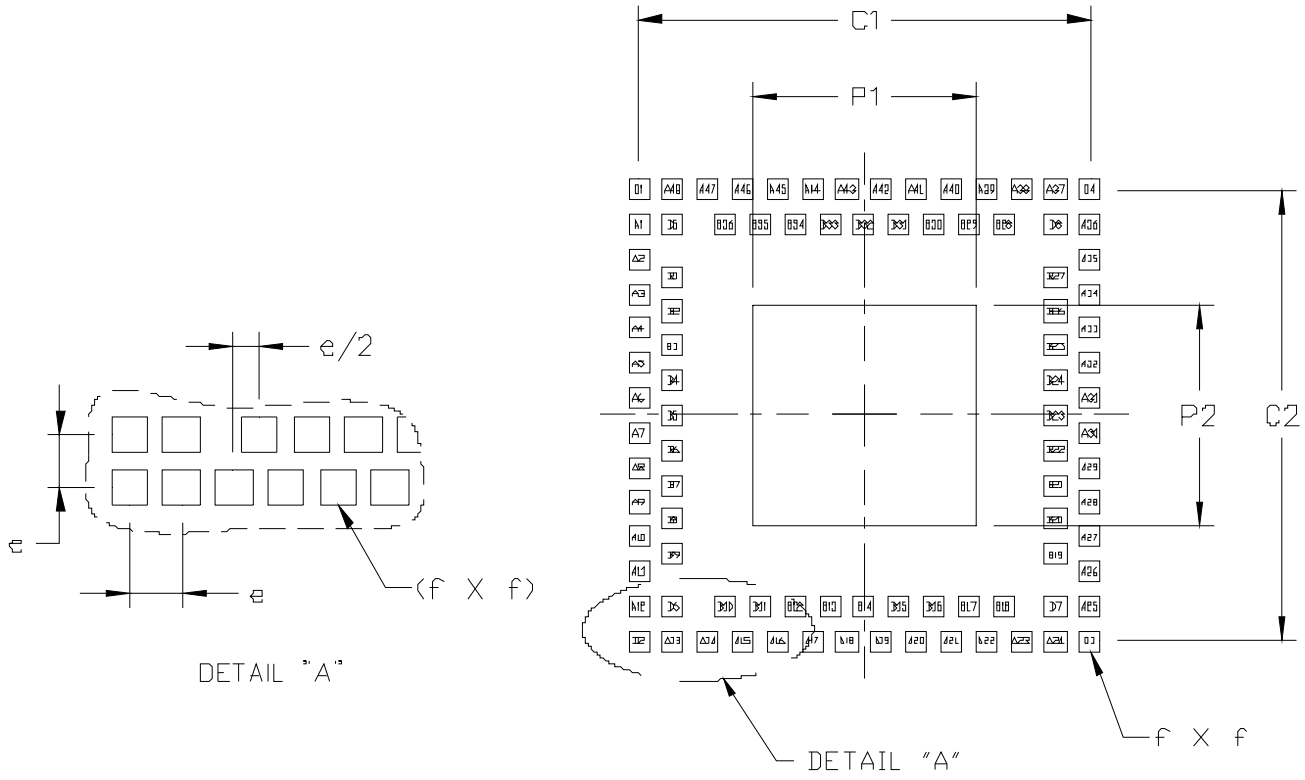


Figure 6.7. LGA-92 Landing Diagram

Table 6.5. LGA-92 Landing Diagram Dimensions

Dimension	Typical	Max
C1	6.50	—
C2	6.50	—
e	0.50	—
f	—	0.35
P1	—	3.20
P2	—	3.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
3. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
4. This land pattern design is based on the IPC-7351 guidelines.

6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

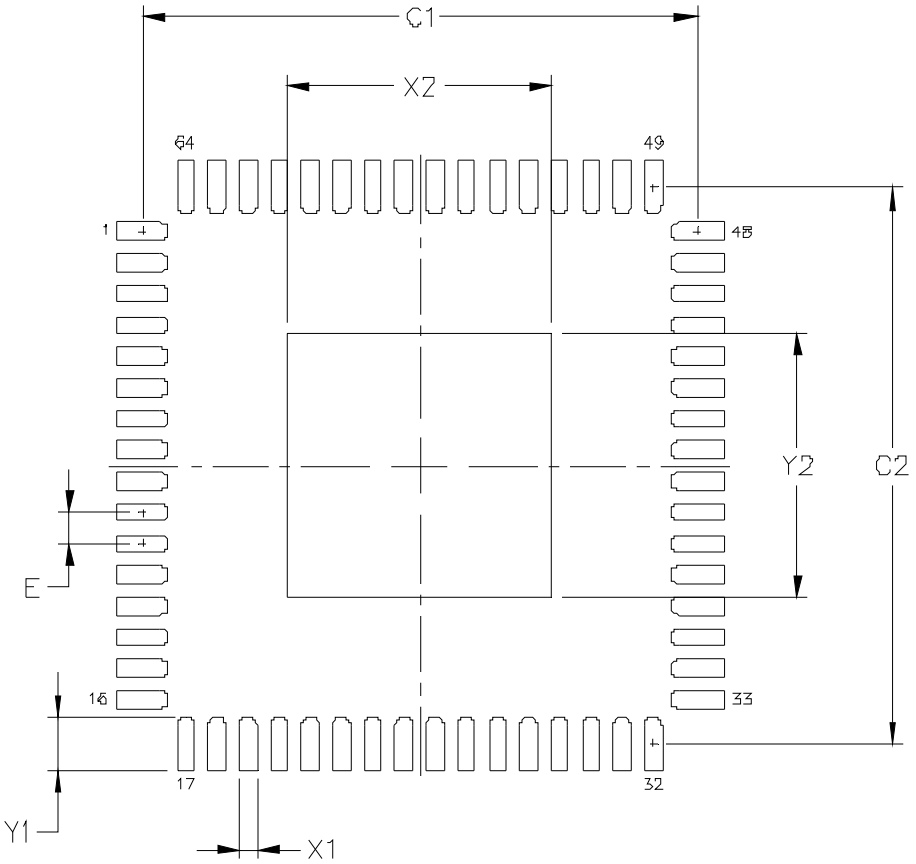


Figure 6.11. QFN-64 Landing Diagram

Table 6.9. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

6.6.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

6.6.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.7.1. TQFP-64 Solder Mask Design

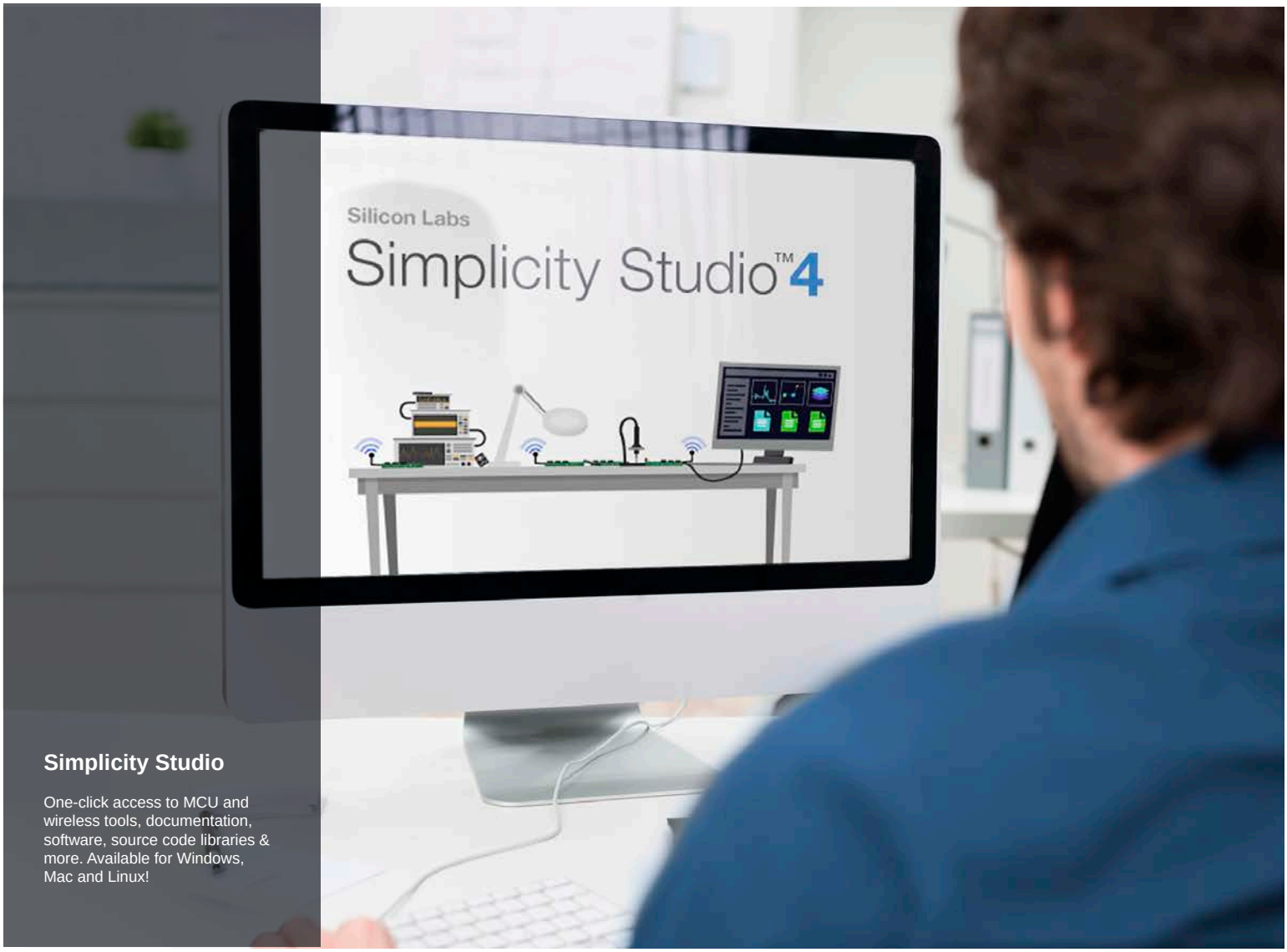
All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.7.2. TQFP-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.7.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



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