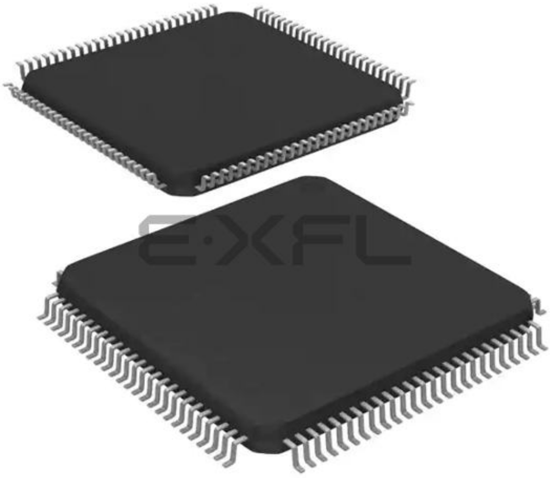
# Silicon Labs - EFM32WG380F64-QFP100T Datasheet



## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 50 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32wg380f64-qfp100t |

# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32WG380 devices.

*Table 1.1. Ordering Information*

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32WG380F64-QFP100 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG380F128-QFP100 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32WG380F256-QFP100 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |

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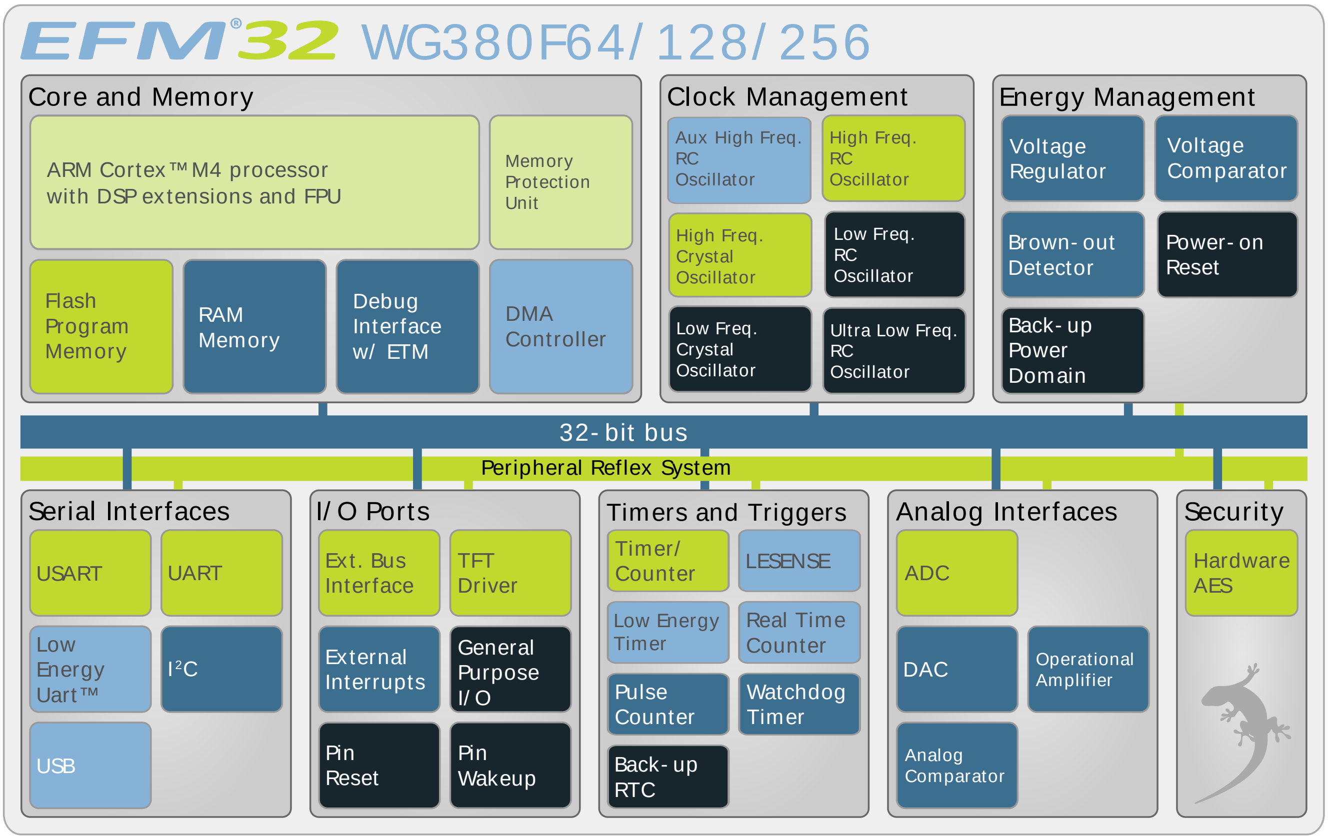
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4, with DSP instruction support and floating-point unit, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG380 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32WG Reference Manual*.

A block diagram of the EFM32WG380 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***



### 2.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor, with DSP instruction support and floating-point unit, which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M4 is described in detail in *ARM Cortex-M4 Devices Generic User Guide*.

### 2.1.2 Debug Interface (DBG)

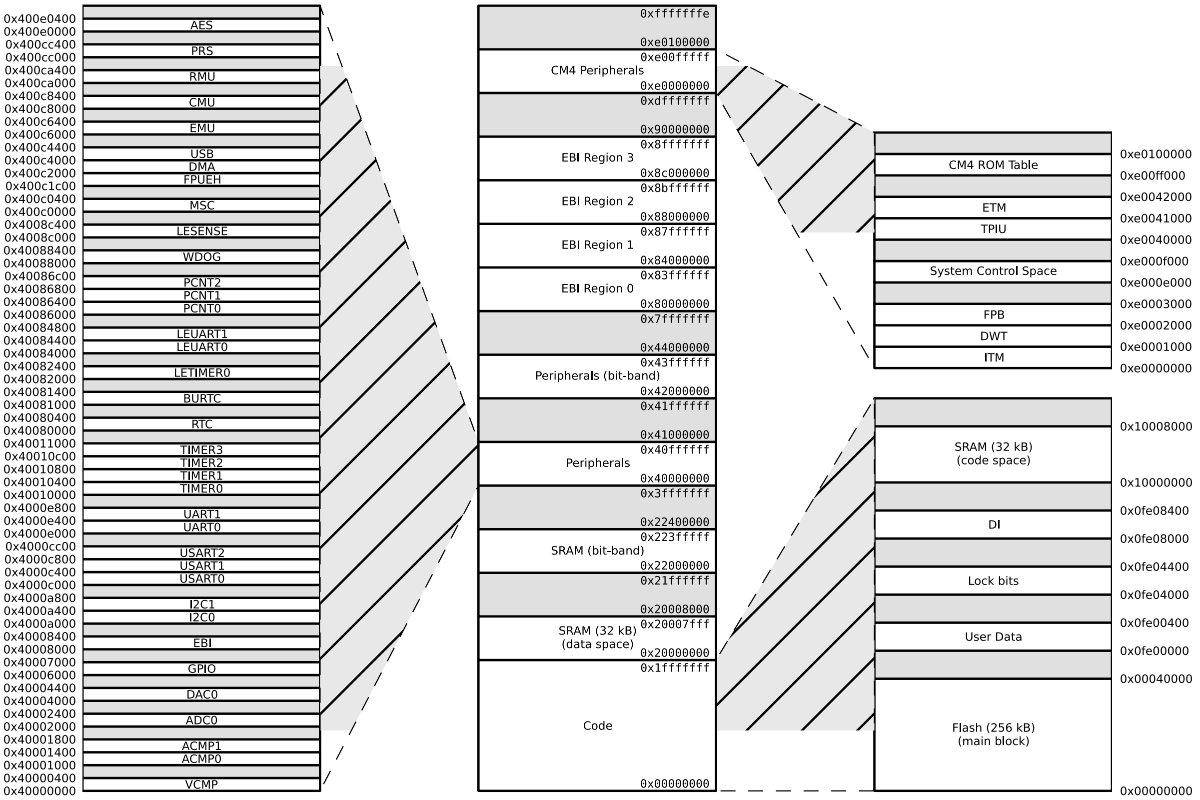
This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 81 pins | Available pins are shown in Table 4.3 (p. 67) |

## 2.3 Memory Map

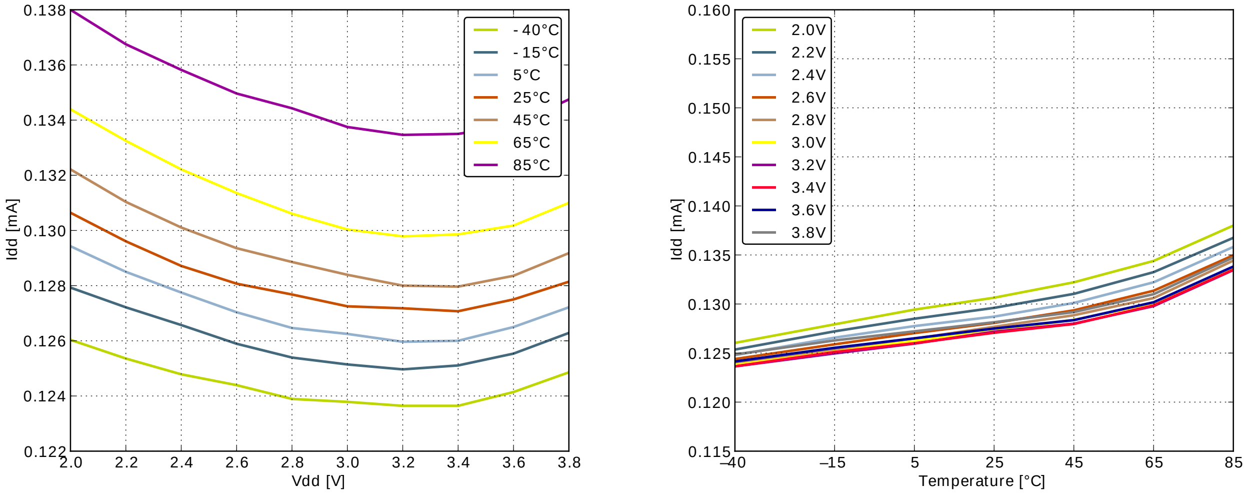
The *EFM32WG380* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

*Figure 2.2. EFM32WG380 Memory Map with largest RAM and Flash sizes*



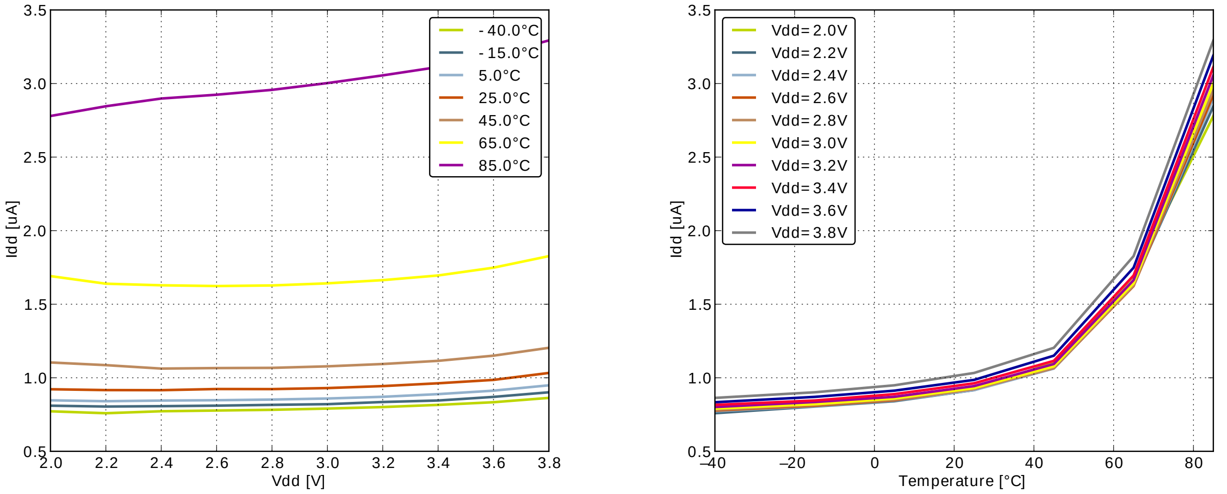
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 271 | 286 | µA/ MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 275 | | µA/ MHz |
| $I_{EM1}$ | EM1 current (Production test condition = 14 MHz) | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 63 | 75 | µA/ MHz |
| | | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 65 | 76 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 64 | 75 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 65 | 77 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 65 | 76 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 66 | 78 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 67 | 79 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 68 | 82 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 68 | 81 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 70 | 83 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 74 | 87 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 76 | 89 | µA/ MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 106 | 120 | µA/ MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 112 | 129 | µA/ MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.95[1] | 1.7[1] | µA |

*Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 1.2MHz*



## 3.4.2 EM2 Current Consumption

*Figure 3.8. EM2 current consumption. RTC[1] prescaled to 1kHz, 32.768 kHz LFRCO.*



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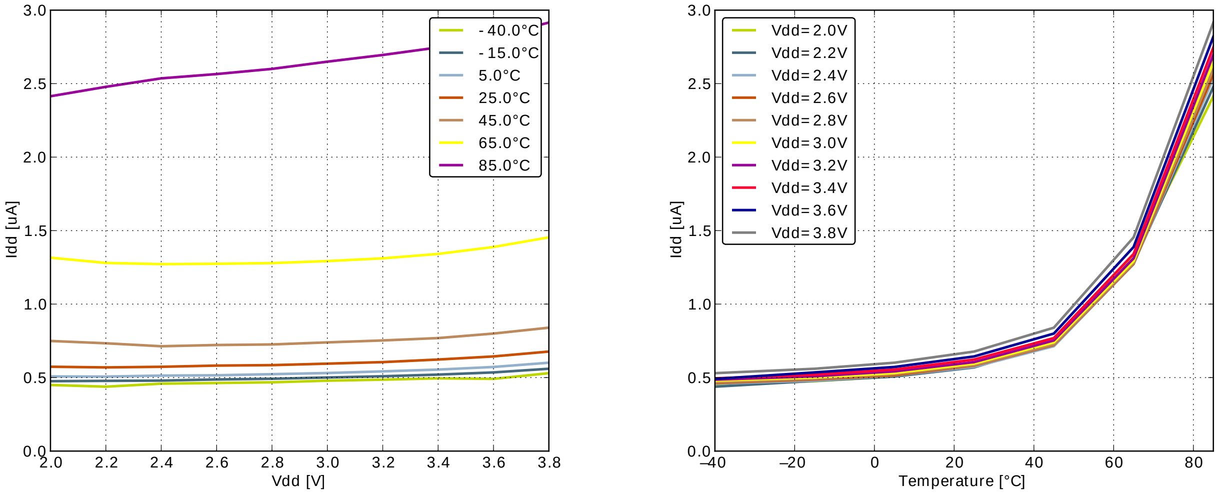
[1] Using backup RTC.

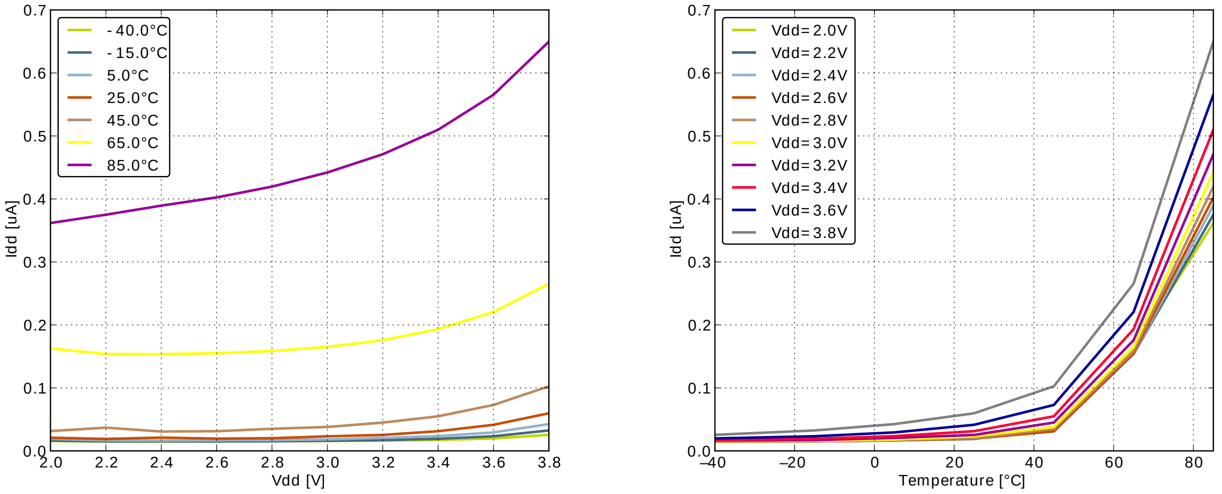
## 3.4.3 EM3 Current Consumption

*Figure 3.9. EM3 current consumption.*



## 3.4.4 EM4 Current Consumption

*Figure 3.10. EM4 current consumption.*



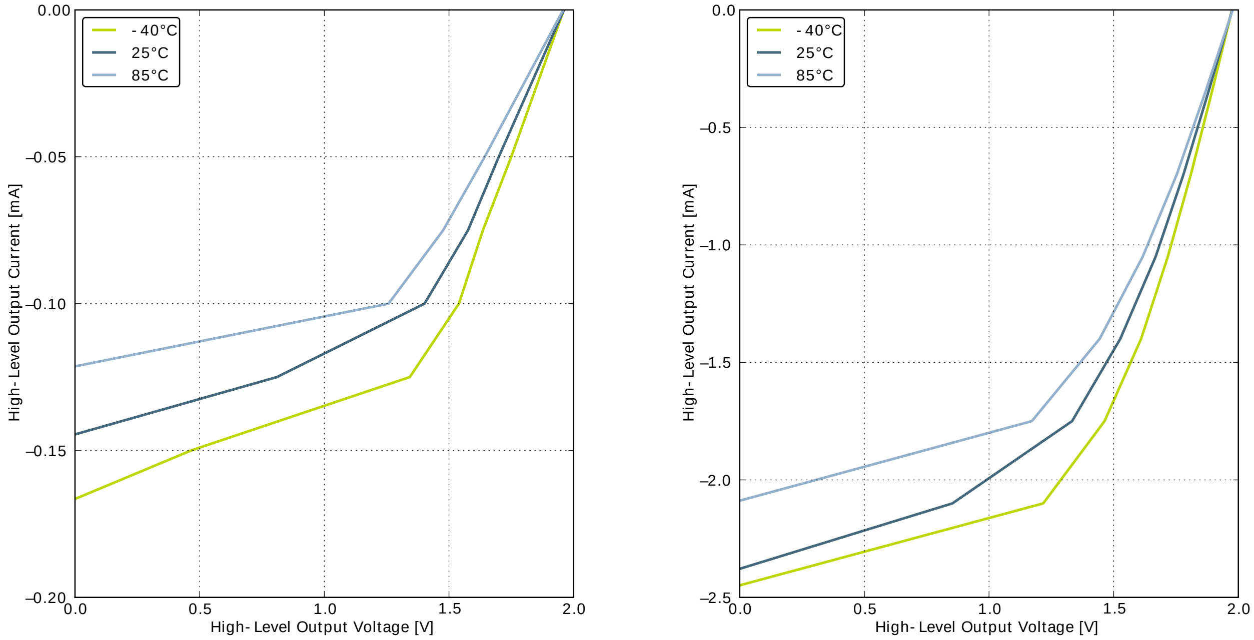
# 3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

*Table 3.5. Energy Modes Transitions*

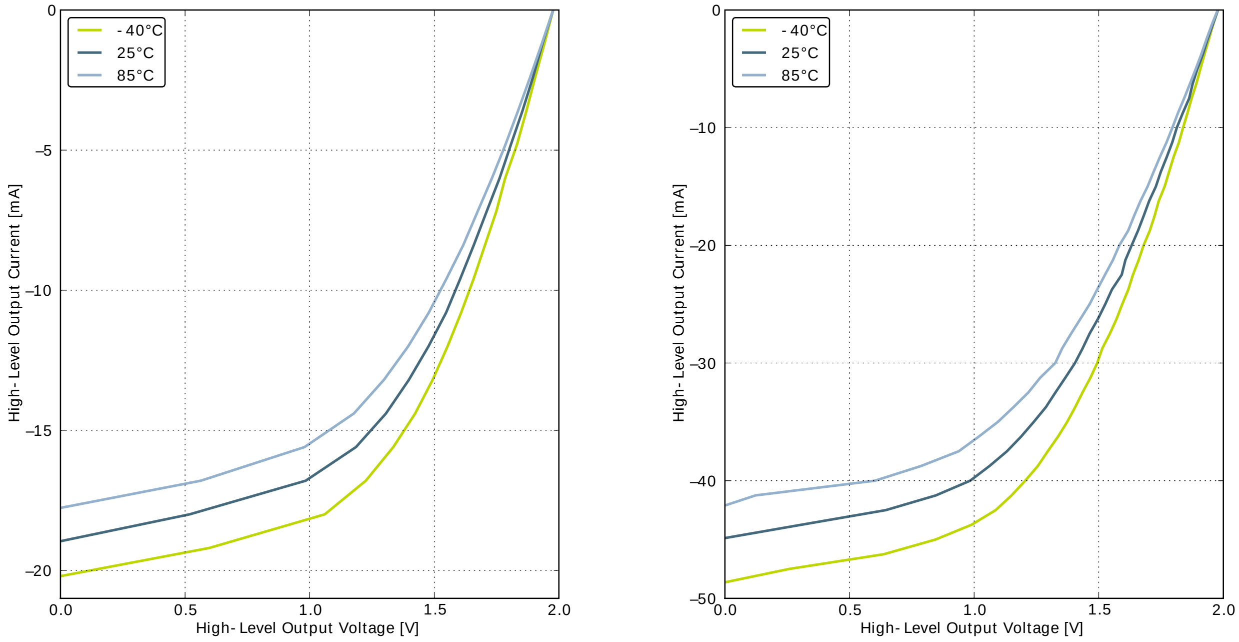
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{EM10}$ | Transition time from EM1 to EM0 | | 0 | | HF-CORE-CLK cycles |
| $t_{EM20}$ | Transition time from EM2 to EM0 | | 2 | | µs |
| $t_{EM30}$ | Transition time from EM3 to EM0 | | 2 | | µs |
| $t_{EM40}$ | Transition time from EM4 to EM0 | | 163 | | µs |

*Figure 3.12. Typical High-Level Output Current, 2V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

# 3.9 Oscillators

## 3.9.1 LFXO

*Table 3.9. LFXO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFXO}$ | Supported nominal crystal frequency | | | 32.768 | | kHz |
| $ESR_{LFXO}$ | Supported crystal equivalent series resistance (ESR) | | | 30 | 120 | kOhm |
| $C_{LFXOL}$ | Supported crystal external load range | | X[1] | | 25 | pF |
| $I_{LFXO}$ | Current consumption for core and buffer after startup. | ESR=30 kOhm, $C_L$=10 pF, LFXOBOOST in CMU_CTRL is 1 | | 190 | | nA |
| $t_{LFXO}$ | Start- up time. | ESR=30 kOhm, $C_L$=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1 | | 400 | | ms |

[1] See Minimum Load Capacitance ($C_{LFXOL}$) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

## 3.9.2 HFXO

*Table 3.10. HFXO*

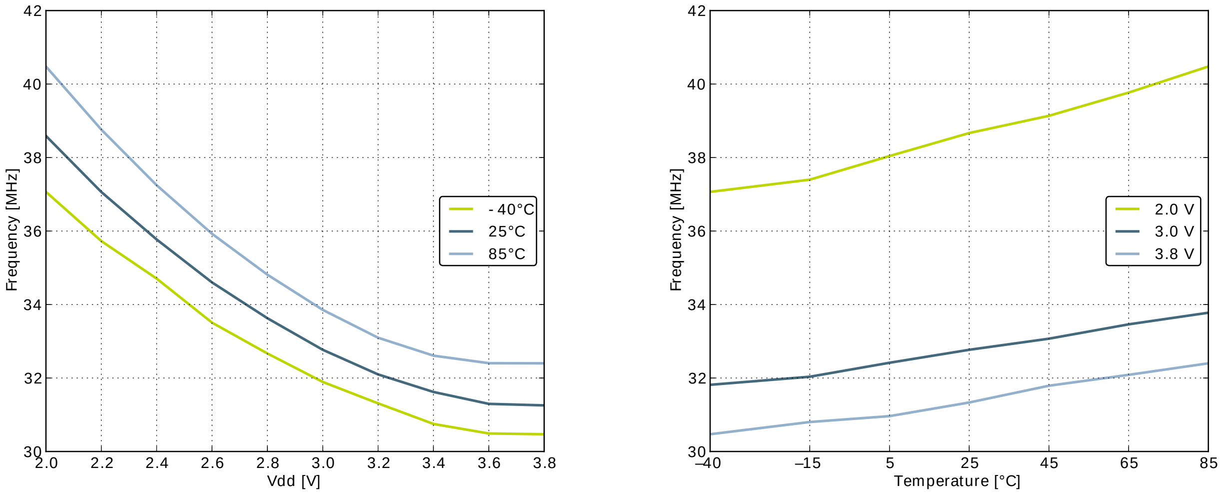
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFXO}$ | Supported nominal crystal Frequency | | 4 | | 48 | MHz |
| $ESR_{HFXO}$ | Supported crystal equivalent series resistance (ESR) | Crystal frequency 48 MHz | | | 50 | Ohm |
| | | Crystal frequency 32 MHz | | 30 | 60 | Ohm |
| | | Crystal frequency 4 MHz | | 400 | 1500 | Ohm |
| $g_{mHFXO}$ | The transconductance of the HFXO input transistor at crystal startup | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | | | mS |
| $C_{HFXOL}$ | Supported crystal external load range | | 5 | | 25 | pF |
| $I_{HFXO}$ | Current consumption for HFXO after startup | 4 MHz: ESR=400 Ohm, $C_L$=20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 85 | | µA |
| | | 32 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 165 | | µA |
| $t_{HFXO}$ | Startup time | 32 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 400 | | µs |

### 3.9.3 LFRCO

*Table 3.11. LFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFRCO}$ | Oscillation frequency , $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 31.29 | 32.768 | 34.28 | kHz |
| $t_{LFRCO}$ | Startup time not including software calibration | | | 150 | | µs |
| $I_{LFRCO}$ | Current consumption | | | 300 | | nA |
| $TUNESTEP_{LFRCO}$ | Frequency step for LSB change in TUNING value | | | 1.5 | | % |

*Figure 3.17.  Calibrated LFRCO Frequency vs Temperature and Supply Voltage*



### 3.9.5 AUXHFRCO

**Table 3.13. AUXHFRCO**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48 | 6.60 | 6.72 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $DC_{AUXHFRCO}$ | Duty cycle | $f_{AUXHFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[1] | | % |

[1] The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### 3.9.6 ULFRCO

**Table 3.14. ULFRCO**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ULFRCO}$ | Oscillation frequency | 25°C, 3V | 0.7 | | 1.75 | kHz |
| $TC_{ULFRCO}$ | Temperature coefficient | | | 0.05 | | %/°C |
| $VC_{ULFRCO}$ | Supply voltage coefficient | | | -18.2 | | %/V |

## 3.10 Analog Digital Converter (ADC)

**Table 3.15. ADC**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCIN}$ | Input voltage range | Single ended | 0 | | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN\_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN\_CH6}$ | Input range of external positive ref- | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 59 | | dB |
| $SNDR_{DAC}$ | Signal to Noise-pulse Distortion Ratio (SNDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 57 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 54 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 56 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 53 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 55 | | dB |
| $SFDR_{DAC}$ | Spurious-Free Dynamic Range(SFDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dBc |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 56 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 61 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 55 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 60 | | dBc |
| $V_{DACOFFSET}$ | Offset voltage | After calibration, single ended | | 2 | 9 | mV |
| | | After calibration, differential | | 2 | | mV |
| $DNL_{DAC}$ | Differential non-linearity | | | ±1 | | LSB |
| $INL_{DAC}$ | Integral non-linearity | | | ±5 | | LSB |
| $MC_{DAC}$ | No missing codes | | | 12 | | bits |

[1] Measured with a static input code and no loading on the output.

## 3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

***Table 3.17. OPAMP***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OPAMP}$ | Active Current | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain | | 370 | 460 | µA |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain | | 95 | 135 | µA |

*Figure 3.34. OPAMP Negative Power Supply Rejection Ratio*

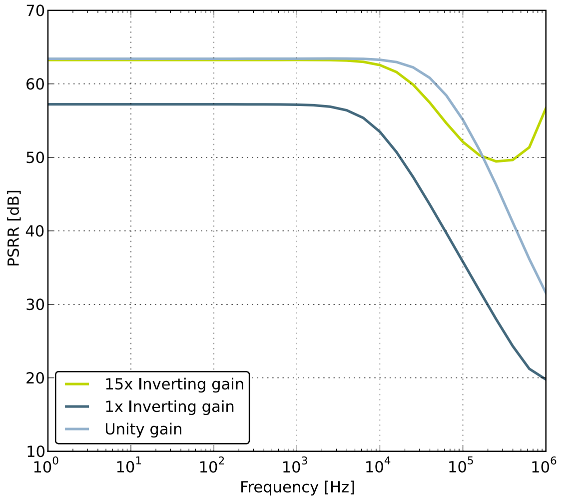


*Figure 3.35. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}$=1V*

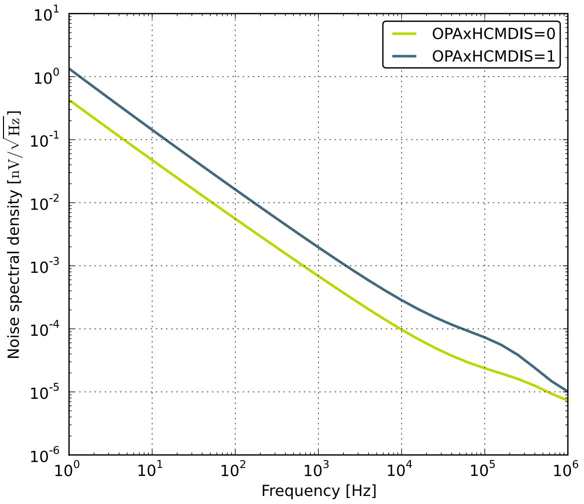
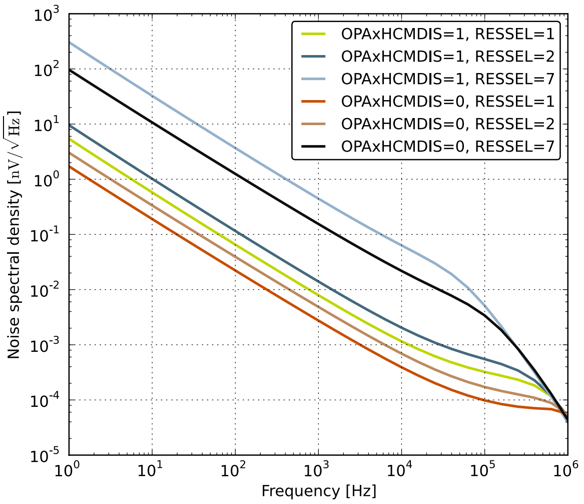


*Figure 3.36. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)*



| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| | | | | | | ETM_TD0 #3 |
| 4 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 10 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 11 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 12 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 15 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 16 | VSS | Ground | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 19 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 20 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 21 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 22 | PC4 | ACMP0_CH4<br>DAC0_P0 /<br>OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4<br>LETIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |
| 23 | PC5 | ACMP0_CH5<br>DAC0_N0 /<br>OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| 24 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 26 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| 27 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| 28 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| 29 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| 30 | PA11 | | EBI_HSNC #0/1/2 | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |
| 32 | VSS | Ground | | | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 95 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| 96 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| 97 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 98 | PE14 | | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 99 | PE15 | | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 100 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 61). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note**

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

*Table 4.2. Alternate functionality overview*

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX |
| BOOT_TX | PE10 | | | | | | | Bootloader TX |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0 / OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1 / OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| DAC0_P0 / OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1 / OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32WG380* is shown in Table 4.3 (p. 67). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

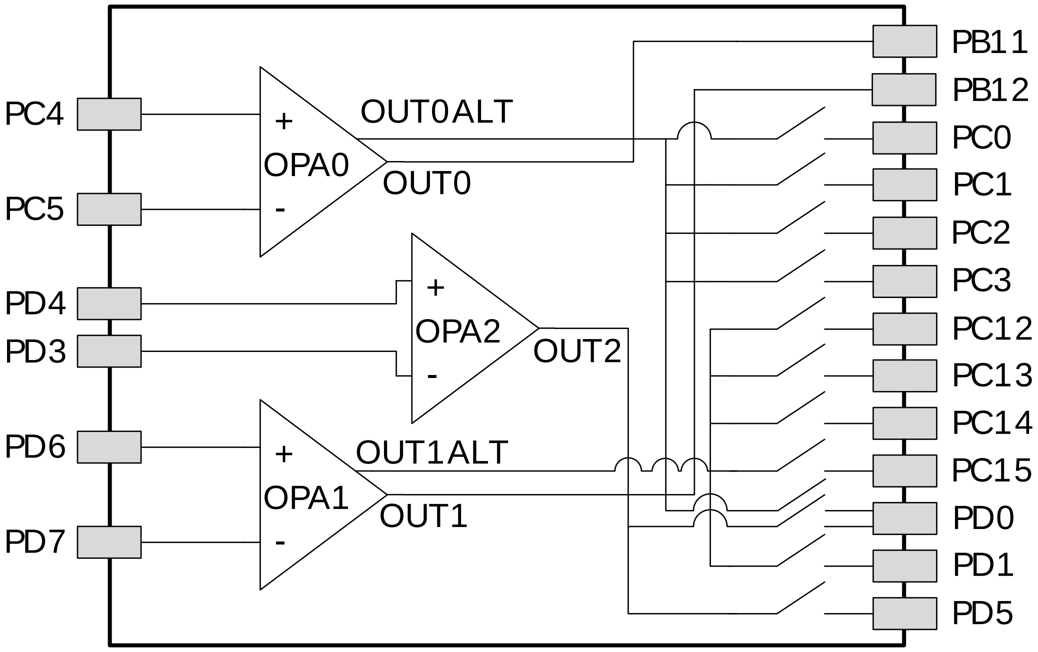
***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | - | - | - | - | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | - | - | - | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | - | - | PF2 | PF1 | PF0 |

## 4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32WG380* is shown in Figure 4.2 (p. 67) .

***Figure 4.2. Opamp Pinout***



# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

*Figure 5.1. LQFP100 PCB Land Pattern*

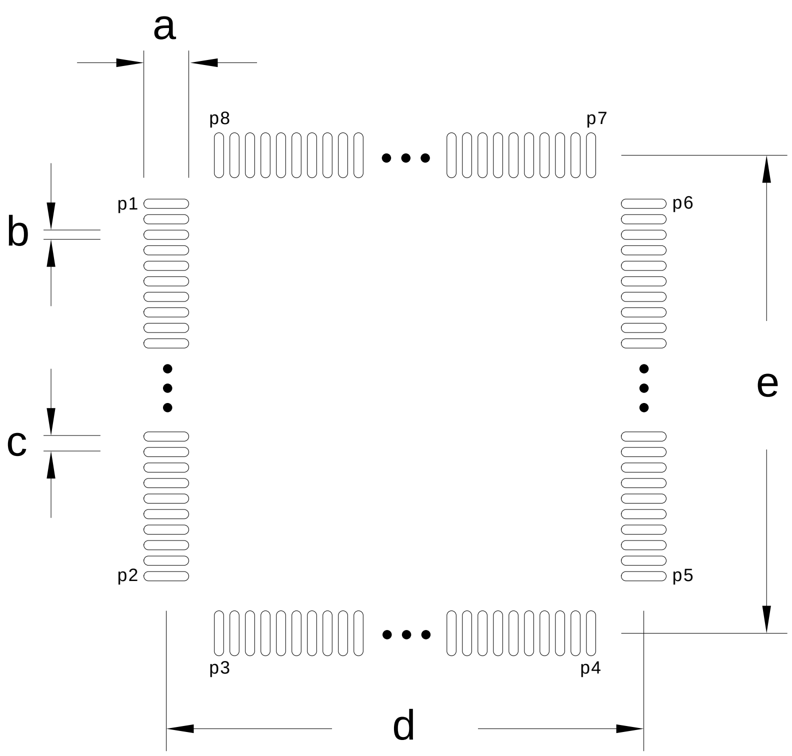


*Table 5.1. QFP100 PCB Land Pattern Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) | Symbol | Pin number | Symbol | Pin number |
|---|---|---|---|---|---|
| a | 1.45 | P1 | 1 | P6 | 75 |
| b | 0.30 | P2 | 25 | P7 | 76 |
| c | 0.50 | P3 | 26 | P8 | 100 |
| d | 15.40 | P4 | 50 | - | - |
| e | 15.40 | P5 | 51 | - | - |

*Figure 5.3. LQFP100 PCB Stencil Design*

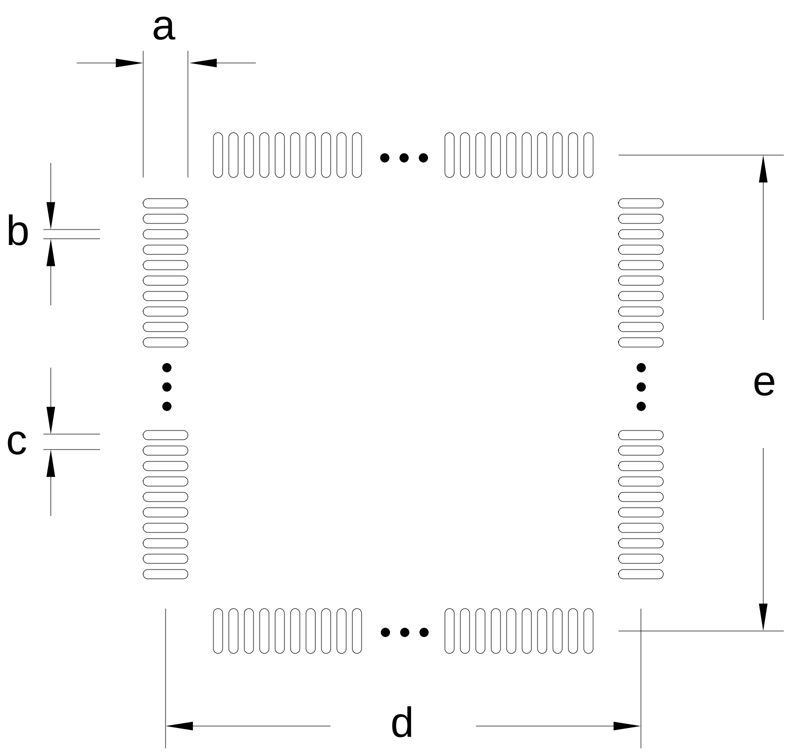


*Table 5.3. QFP100 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 1.35 |
| b | 0.20 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 68) .

## 5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

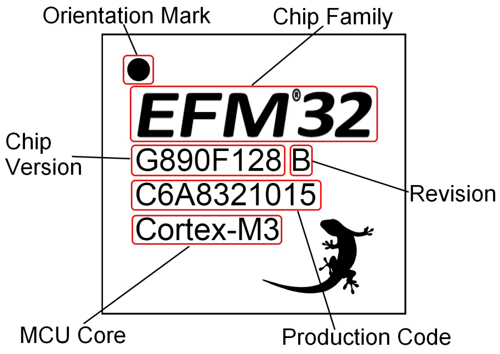
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

# 6 Chip Marking, Revision and Errata

## 6.1 Chip Marking

In the illustration below package fields and position are shown.

*Figure 6.1. Example Chip Marking (top view)*



## 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 73) .

## 6.3 Errata

Please see the errata document for EFM32WG380 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

# A Disclaimer and Trademarks

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