E·XFL

Zilog - ZGP323HAH2004C00TR Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	•
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hah2004c00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters 532 Race Street

San Jose, CA 95126-3432 Telephone: 408.558.8500 Fax: 408.558.8300 www.zilog.com

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

Document Disclaimer

©2005 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZILOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose. Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.



Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum		
Input capacitance	12pF		
Output capacitance	12pF		
I/O capacitance	12pF		
Note: $T_A = 25^{\circ}$ C, $V_{CC} = GND = 0$ V, f = 1.0 MHz, unmeasured pins returned to GND			

DC Characteristics

Table 9. GP323HS DC Characteristics

	T _≜ =0°C to +70°C								
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions N	lotes	
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5 5	5	
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator		
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator		
VIH	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V			
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V			
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	$I_{OH} = -0.5 \text{mA}$		
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA		
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$		
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA		
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV			
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{CC} 1.75	V			
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled		
R _{PU}	Pull-up Resistance	2.0V	225		675	KΩ	V _{IN} = 0V; Pullups selected by mask		
-		3.6V	75		275	KΩ	option		
		5.0V	40		160	KΩ			



Table 11. GP323HA DC Characteristics

	T _A = -40°C to +125°C								
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes	
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5	
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator		
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} –0.3		0.4	V	Driven by External Clock Generator		
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V			
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V			
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA		
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA		
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$		
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA		
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV			
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V			
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled		
R _{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V _{IN} = 0V; Pullups selected by mask		
		3.6V	50		300	KΩ	option		
		5.0V	25		175	KΩ	_		
I _{OL}	Output Leakage	2.0-5.5	-1		1	μΑ	$V_{IN} = 0V, V_{CC}$		
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2	
		3.6V		5	10	mA	at 8.0 MHz	1, 2	
		5.5V		10	15	mA	at 8.0 MHz	1, 2	
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6	
	(HALI Mode)	3.6V		0.8	2.0	mA	$V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6	
<u> </u>		5.5V		1.3	3.2	mA	$V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6	
I _{CC2}	Standby Current (Stop	2.0V		1.6	15	μA	$V_{IN} = 0$ V, V_{CC} WDT not Running	3	
	Mode)	3.6V		1.8	20	μA	$V_{IN} = 0$ V, V_{CC} WDT not Running	3	
		5.5V		1.9	25	μΑ	$v_{IN} = 0$ V, v_{CC} WDT not Running	3	
		2.00		с С	30	μΑ	$v_{IN} = 0$ V, v_{CC} WDT is Running	ა ი	
		3.0V 5.5V		0 15	40 60	μΑ	$v_{IN} = 0.0$, v_{CC} wDT is Running	ა ვ	
	Chan allow Course at	0.00		10	00	μΑ	$V_{\rm IN} = 0.0$, $V_{\rm CC}$ with the Ruthing	3	
	(Low Voltage)			1.2	0	μΑ		4	
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.		
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V			







Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



25

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP does not assert the $\overline{\text{RESET}}$ pin when under VBO.



Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®], functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.



Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field Bit Position			Description
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data







Figure 24. Demodulation Mode Flowchart



50

During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Interrupts

The ZGP323H features six different interrupts (Table 19). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 19) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 59.



FF	NOP	;	clear	the pipeline
6F	Stop	;	enter	Stop Mode
or				
FF	NOP	;	clear	the pipeline
7F	HALT	;	enter	HALT Mode

Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H



* Default setting after reset

Figure 32. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.







Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 22).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 21 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Reserved	7		0	Reserved (Must be 0)
Recovery Level	-6	W	0 [†]	Low
-			1	High
Reserved	5		0	Reserved (Must be 0)
Source	432	W	000†	A. POR Only
Source			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	10		00	Reserved (Must be 0)

Table 21. SMR2(F)0DH:Stop	Mode Recovery	Register	2*
---------------------------	---------------	----------	----

Notes:

* Port pins configured as outputs are ignored as a SMR recovery source. † Indicates the value upon Power-On Reset



69

CTR2(0D)02H



Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)



R247 P3M(F7H)



* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)



R249 IPR(F9H)



Figure 51. Interrupt Priority Register (F9H: Write Only)



R252 Flags(FCH)



Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)







MILLIMETER			INCH		
MIN	NOM	MAX	MIN	NOM	MAX
1.73	1.85	1.98	0.068	0.073	0.078
0.05	0.13	0.21	0.002	0.005	0.008
1.68	1.73	1.83	0.066	0.068	0.072
0.25	0.30	0.38	0.010	0.012	0.015
0.13	0.15	0.22	0.005	0.006	0.009
7.07	7.20	7.33	0.278	0.283	0.289
5.20	5.30	5.38	0.205	0.209	0.212
0.65 BSC		0.0256 BSC			
7.65	7.80	7.90	0.301	0.307	0.311
0.56	0.75	0.94	0.022	0.030	0.037
0.74	0.78	0.82	0.029	0.031	0.032
	MIN 1.73 0.05 1.68 0.25 0.13 7.07 5.20 7.65 0.56 0.74	MILLIMETER MIN NOM 1.73 1.85 0.05 0.13 1.68 1.73 0.25 0.30 0.13 0.15 7.07 7.20 5.20 5.30 0.65 BSC 7.65 7.80 0.56 0.75 0.74 0.78	MILLIMETER MIN NOM MAX 1.73 1.85 1.98 0.05 0.13 0.21 1.68 1.73 1.83 0.25 0.30 0.38 0.13 0.15 0.22 7.07 7.20 7.33 5.20 5.30 5.38 0.65 BSC 7.65 7.80 7.90 0.56 0.75 0.94 0.74 0.78 0.82	MILLIMETER MIN NOM MAX MIN 1.73 1.85 1.98 0.068 0.05 0.13 0.21 0.002 1.68 1.73 1.83 0.066 0.25 0.30 0.38 0.010 0.13 0.15 0.22 0.005 7.07 7.20 7.33 0.278 5.20 5.30 5.38 0.205 0.65 BSC - - 7.65 7.80 7.90 0.301 0.56 0.75 0.94 0.022 0.74 0.78 0.82 0.029	MILLIMETER INCH MIN NOM MAX MIN NOM 1.73 1.85 1.98 0.068 0.073 0.05 0.13 0.21 0.002 0.005 1.68 1.73 1.83 0.066 0.068 0.25 0.30 0.38 0.010 0.012 0.13 0.15 0.22 0.005 0.006 7.07 7.20 7.33 0.278 0.283 5.20 5.30 5.38 0.205 0.209 O.055 BSC 7.65 7.80 7.90 0.301 0.307 0.56 0.75 0.94 0.022 0.030 0.74 0.78 0.82 0.029 0.31



DETAIL A

Н

CONTROLLING DIMENSIONS : MM LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram







Figure 63. 28-Pin CDIP Package Diagram

SVMBOI	OL OPT#	MILLIMETER		INCH	
SIMDOL		MíN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
В		0.38	0.53	.015	.021
D1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
С		0.23	0.38	.009	.015
п	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
01	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
•	01	1.52	2.29	.060	.090
S	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

01

02

STANDARD

Figure 64. 28-Pin PDIP Package Diagram

A1	 ¥↓ ↓ δ
↓	A2 A

	MILLIMETER			INCH		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
А	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
В	0.25		0.38	0.010		0.015
С	0.09	-	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.402	0.407
E	5.20	5.30	5.38	0.205	0.209	0.212
е	0.65 TYP			0.0256 TYF)	
Н	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

CONTROLLING DIMENSIONS: MM LEADS ARE COPLANAR WITHIN .004 INCHES.

<u>DETAIL 'A'</u>

0-8

Figure 65. 28-Pin SSOP Package Diagram

SYMBOL	MILLIN	IETER	INCH		
SIMDOL	MIN	MAX	MIN	MAX	
A1	0.51	1.02	.020	.040	
A2	3.18	3.94	.125	.155	
В	0.38	0.53	.015	.021	
B1	1.02	1.52	.040	.060	
С	0.23	0.38	.009	.015	
D	52.07	52.58	2.050	2.070	
E	15.24	15.75	.600	.620	
E1	13.59	14.22	.535	.560	
e	2.54 TYP		.100 TYP		
eA	15.49	16.76	.610	.660	
L	3.05	3.81	.120	.150	
Q1	1.40	1.91	.055	.075	
2	1.52	2.20	060	000	

CONTROLLING DIMENSIONS : INCH

Figure 66. 40-Pin PDIP Package Diagram

16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C				
Part Number	Description	Part Number	Description	
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP	
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP	
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP	
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP	

16KB Automotive Temperature: -40° to +125°CPart NumberDescriptionPart NumberDescriptionZGP323HAH4816C48-pin SSOP 16K OTPZGP323HAS2816C28-pin SOIC 16K OTPZGP323HAP4016C40-pin PDIP 16K OTPZGP323HAH2016C20-pin SSOP 16K OTPZGP323HAH2816C28-pin SSOP 16K OTPZGP323HAP2016C20-pin PDIP 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPReplace C with G for Lead-Free Packaging

ZGP323H Z8[®] OTP Microcontroller with IR Timers

Numerics 16-bit counter/timer circuits 46 20-pin DIP package diagram 82 20-pin SSOP package diagram 84 28-pin DIP package diagram 86 28-pin SOICpackage diagram 85 28-pin SSOP package diagram 87 40-pin DIP package diagram 87 48-pin SSOP package diagram 89 8-bit counter/timer circuits 42 А absolute maximum ratings 10 AC characteristics 16 timing diagram 16 address spaces, basic 2 architecture 2 expanded register file 28 В basic address spaces 2 block diagram, ZLP32300 functional 3 С capacitance 11 characteristics AC 16 DC 11 clock 53 comparator inputs/outputs 25 configuration port 0 19 port 1 20 port 2 21 port 3 22 port 3 counter/timer 24 counter/timer 16-bit circuits 46 8-bit circuits 42 brown-out voltage/standby 64 clock 53 demodulation mode count capture flowchart 44

demodulation mode flowchart 45 EPROM selectable options 64 glitch filter circuitry 40 halt instruction 54 input circuit 40 interrupt block diagram 51 interrupt types, sources and vectors 52 oscillator configuration 53 output circuit 49 ping-pong mode 48 port configuration register 55 resets and WDT 63 SCLK circuit 58 stop instruction 54 stop mode recovery register 57 stop mode recovery register 2 61 stop mode recovery source 59 T16 demodulation mode 47 T16 transmit mode 46 T16 OUT in modulo-N mode 47 T16_OUT in single-pass mode 47 T8 demodulation mode 43 T8 transmit mode 40 T8 OUT in modulo-N mode 43 T8_OUT in single-pass mode 43 transmit mode flowchart 41 voltage detection and flags 65 watch-dog timer mode register 62 watch-dog timer time select 63 CTR(D)01h T8 and T16 Common Functions 35 D DC characteristics 11 demodulation mode count capture flowchart 44 flowchart 45 T1647 T8 43 description functional 25 general 2

ZGP323H Z8[®] OTP Microcontroller with IR Timers

28-pin DIP/SOIC/SSOP 6 40- and 48-pin 8 40-pin DIP 7 48-pin SSOP 8 pin functions port 0 (P07 - P00) 18 port 0 (P17 - P10) 19 port 0 configuration 19 port 1 configuration 20 port 2 (P27 - P20) 20 port 2 (P37 - P30) 21 port 2 configuration 21 port 3 configuration 22 port 3 counter/timer configuration 24 reset) 25 XTAL1 (time-based input 18 XTAL2 (time-based output) 18 ping-pong mode 48 port 0 configuration 19 port 0 pin function 18 port 1 configuration 20 port 1 pin function 19 port 2 configuration 21 port 2 pin function 20 port 3 configuration 22 port 3 pin function 21 port 3counter/timer configuration 24 port configuration register 55 power connections 3 power supply 5 program memory 25 map 26 R ratings, absolute maximum 10 register 61 CTR(D)01h 35 CTR0(D)00h 33 CTR2(D)02h 37 CTR3(D)03h 39 flag 80 HI16(D)09h 32

HI8(D)0Bh 32 interrupt priority 78 interrupt request 79 interruptmask 79 L016(D)08h 32 L08(D)0Ah 32 LVD(D)0Ch 65 pointer 80 port 0 and 1 77 port 2 configuration 75 port 3 mode 76 port configuration 55, 75 SMR2(F)0Dh 40 stack pointer high 81 stack pointer low 81 stop mode recovery 57 stop mode recovery 2 61 stop-mode recovery 73 stop-mode recovery 274 T16 control 69 T8 and T16 common control functions 67 T8/T16 control 70 TC16H(D)07h 32 TC16L(D)06h 33 TC8 control 66 TC8H(D)05h 33 TC8L(D)04h 33 voltage detection 71 watch-dog timer 75 register description Counter/Timer2 LS-Byte Hold 33 Counter/Timer2 MS-Byte Hold 32 Counter/Timer8 Control 33 Counter/Timer8 High Hold 33 Counter/Timer8 Low Hold 33 CTR2 Counter/Timer 16 Control 37 CTR3 T8/T16 Control 39 Stop Mode Recovery2 40 T16 Capture LO 32 T8 and T16 Common functions 35 T8_Capture_HI 32