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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hah2008g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

ZGP323H | Product Specification |



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Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.







Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—

ZGP323H Product Specification



Location of 3	2768	Not Accessible
first Byte of	-100	On-Chip
executed		KOM
after RESET	12	Reset Start Address
	11	IRQ5
Interrupt Vector (Lower Byte) Interrupt Vector (Upper Byte)	10	IRQ5
	9	IRQ4
	8	IRQ4
	7	IRQ3
	6	IRQ3
	5	IRQ2
	4	→ IRQ2
	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0



Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8[®] register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A OH in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.





Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 28)

R253 RP = 00h R0 = Port 0 R1 = Port 1 R2 = Port 2 R3 = Port 3

But if:

R253 RP = 0Dh R0 = CTR0 R1 = CTR1 R2 = CTR2R3 = Reserved







Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Mode	7	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/	-6	R/W		Transmit Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0*	P31
			1	P20
T8/T16_Logic/	54	R/W		Transmit Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

Table 16. CTR1(0D)01H T8 and T16 Common Functions



Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5– D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).



Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.







Figure 19. Transmit Mode Flowchart



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put



T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



Figure 25. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in "Interrupts" on page 50.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

)

Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.





Figure 30. Interrupt Block Diagram



Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:



Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.



SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

* * Default setting after Reset and Stop Mode Recovery

* * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



CTR2(0D)02H



Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)









Figure 58. 20-Pin CDIP Package





Figure 59. 20-Pin PDIP Package Diagram





CONTROLLING DIMENSIONS : INCH









MILLIMETER			INCH		
MIN	NOM	MAX	MIN	NOM	MAX
1.73	1.85	1.98	0.068	0.073	0.078
0.05	0.13	0.21	0.002	0.005	0.008
1.68	1.73	1.83	0.066	0.068	0.072
0.25	0.30	0.38	0.010	0.012	0.015
0.13	0.15	0.22	0.005	0.006	0.009
7.07	7.20	7.33	0.278	0.283	0.289
5.20	5.30	5.38	0.205 0.209		0.212
0.65 BSC				0.0256 BSC	;
7.65	7.80	7.90	0.301	0.307	0.311
0.56	0.75	0.94	0.022	0.030	0.037
0.74	0.78	0.82	0.029	0.031	0.032
	MIN 1.73 0.05 1.68 0.25 0.13 7.07 5.20 7.65 0.56 0.74	MILLIMETER MIN NOM 1.73 1.85 0.05 0.13 1.68 1.73 0.25 0.30 0.13 0.15 7.07 7.20 5.20 5.30 0.65 BSC 7.65 7.80 0.56 0.75 0.74 0.78	MILLIMETER MIN NOM MAX 1.73 1.85 1.98 0.05 0.13 0.21 1.68 1.73 1.83 0.25 0.30 0.38 0.13 0.15 0.22 7.07 7.20 7.33 5.20 5.30 5.38 0.65 BSC 7.65 7.80 7.90 0.56 0.75 0.94 0.74 0.78 0.82	MILLIMETER MIN NOM MAX MIN 1.73 1.85 1.98 0.068 0.05 0.13 0.21 0.002 1.68 1.73 1.83 0.066 0.25 0.30 0.38 0.010 0.13 0.15 0.22 0.005 7.07 7.20 7.33 0.278 5.20 5.30 5.38 0.205 0.65 BSC - - 7.65 7.80 7.90 0.301 0.56 0.75 0.94 0.022 0.74 0.78 0.82 0.029	MILLIMETER INCH MIN NOM MAX MIN NOM 1.73 1.85 1.98 0.068 0.073 0.05 0.13 0.21 0.002 0.005 1.68 1.73 1.83 0.066 0.068 0.25 0.30 0.38 0.010 0.012 0.13 0.15 0.22 0.005 0.006 7.07 7.20 7.33 0.278 0.283 5.20 5.30 5.38 0.205 0.209 O.055 BSC 7.65 7.80 7.90 0.301 0.307 0.56 0.75 0.94 0.022 0.030 0.74 0.78 0.82 0.029 0.31



DETAIL A

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CONTROLLING DIMENSIONS : MM LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram

ZGP323H Z8[®] OTP Microcontroller with IR Timers



pin 4 Ε **EPROM** selectable options 64 expanded register file 26 expanded register file architecture 28 expanded register file control registers 71 flag 80 interrupt mask register 79 interrupt priority register 78 interrupt request register 79 port 0 and 1 mode register 77 port 2 configuration register 75 port 3 mode register 76 port configuration register 75 register pointer 80 stack pointer high register 81 stack pointer low register 81 stop-mode recovery register 73 stop-mode recovery register 2 74 T16 control register 69 T8 and T16 common control functions register 67 T8/T16 control register 70 TC8 control register 66 watch-dog timer register 75 F features standby modes 1 functional description counter/timer functional blocks 40 CTR(D)01h register 35 CTR0(D)00h register 33 CTR2(D)02h register 37 CTR3(D)03h register 39 expanded register file 26 expanded register file architecture 28 HI16(D)09h register 32 HI8(D)0Bh register 32 L08(D)0Ah register 32 L0I6(D)08h register 32

program memory map 26 **RAM 25** register description 65 register file 30 register pointer 29 register pointer detail 31 SMR2(F)0D1h register 40 stack 31 TC16H(D)07h register 32 TC16L(D)06h register 33 TC8H(D)05h register 33 TC8L(D)04h register 33 G glitch filter circuitry 40 Η halt instruction, counter/timer 54 input circuit 40 interrupt block diagram, counter/timer 51 interrupt types, sources and vectors 52 L low-voltage detection register 65 Μ memory, program 25 modulo-N mode T16 OUT 47 T8 OUT 43 0 oscillator configuration 53 output circuit, counter/timer 49 Ρ package information 20-pin DIP package diagram 82 20-pin SSOP package diagram 84 28-pin DIP package diagram 86 28-pin SOIC package diagram 85 28-pin SSOP package diagram 87 40-pin DIP package diagram 87 48-pin SSOP package diagram 89 pin configuration 20-pin DIP/SOIC/SSOP 5