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#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hah2032g

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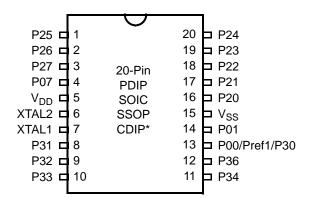
# ZGP323H Product Specification



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## Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 4.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20-P24	Port 2, Bits 0,1,2,3,4	Input/Output



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			T <sub>A</sub> =0°C t	o +70°C				
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
	(HALT Mode)	3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop	2.0V		1.6	8	μΑ	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
	Mode)	3.6V		1.8	10	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		5.5V		1.9	12	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		2.0V		5	20	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		3.6V		8	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		5.5V		15	45	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage			1.9	2.0	V	8MHz maximum	
	Protection						Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		
V <sub>HVD</sub>	Vcc High Voltage Detection			2.7		V		

## Table 9. GP323HS DC Characteristics (Continued)

#### Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when  $V_{CC}$  falls below  $V_{BO}$  limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

- 6. Comparator and Timers are on. Interrupt disabled.
- 7. Typical values shown are at 25 degrees C.

# Table 10. GP323HE DC Characteristics

T <sub>A</sub> = -40°C to +105°C								
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> –0.3		0.4	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	$I_{OH} = -0.5 \text{mA}$	



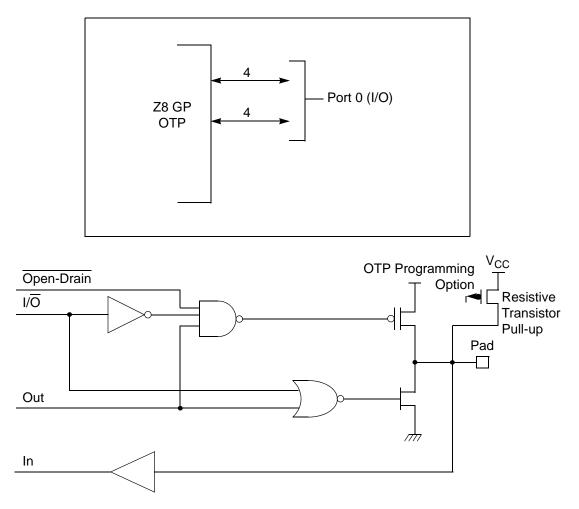


Figure 9. Port 0 Configuration

# Port 1 (P17–P10)

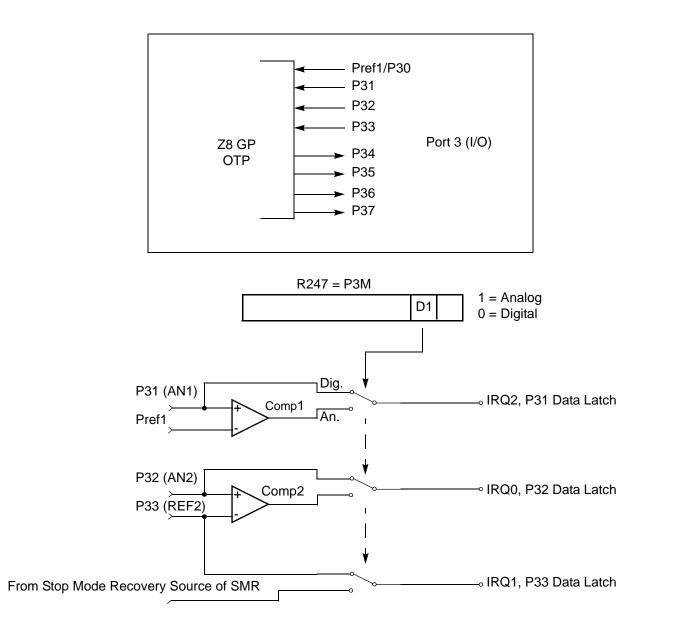
Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.



**Note:** The Port 1 direction is reset to its default state following an SMR.







## Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



CTR1(0D)01H" on page 35). Other edge detect and IRQ modes are described in Table 14.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

# Table 14. Port 3 Pin Function Summary

>

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.





Z8 <sup>®</sup> Standard (	Control Registers	Reset Condition
	Expanded Reg. Bank 0/Group 15	** D7 D6 D5 D4 D3 D2 D1 D0
	FF SPL	
	FE SPH	
Register Pointer	FD RP	0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	FC FLAGS	
	FB IMR	
Working Register Expanded Regist	er FA IRQ	0 0 0 0 0 0 0 0
Group Pointer Bank Pointer	F9 IPR	
	F8 P01M	1 1 0 0 1 1 1 1
	* F7 P3M	0 0 0 0 0 0 0 0
	* F6 P2M	
	F5 Reserved	
	F4 Reserved	
X	F3 Reserved F2 Reserved	
Register File (Bank 0)**		
FF F0		
	F0 Reserved	
	Expanded Reg. Bank F/Group 0**	×
	(F) OF WDTMR	
	(F) 0E Reserved	
	* (F) 0D_SMR2	0 0 0 0 0 0 0 0
	(F) 0C Reserved	
	(F) 0B_SMR	
7F	(F) 0A Reserved	
	(F) 09 Reserved	┫┣╌┽┽┽┽┽┽┽┥╴
	(F) 08 Reserved	┫┝┼┼┼┼┼┼┼┥
	(F) 07 Reserved	╢┝┼┼┼┼┼┼┼┤
	(F) 06 Reserved	┫┝┼┼┼┼┼┼┼┥
	(F) 05 Reserved	
₀₅┝─────₽₽∕	(F) 04 Reserved	
	(F) 03 Reserved	
	(F) 02 Reserved	
	(F) 01 Reserved	┨┠┼┼┼┼┼┼┼┥
Expanded Reg. Bank 0/Group (0)	(F) 00 PCON	
	Expanded Reg. Bank D/Group 0	, <u>, , , , , , , , , , , , , , , , , , </u>
(0) 03 P3 0 U	(D) OC LVD	
(0) 02 P2 U	* (D) 0B HI8	00000000
* (0) 01 P1 U	* (D) 0A LO8	00000000
	* (D) 09 HI16	000000000
(0) 00 P0 U	* (D) 08 LO16	000000000
U = Unknown	* (D) 07 TC16H	000000000
* Is not reset with a Stop-Mode Recovery	* (D) 06 TC16L	00000000
** All addresses are in hexadecimal	* (D) 05 TC8H	00000000
↑ Is not reset with a Stop-Mode Recovery, except Bit 0	* (D) 04 TC8L	0 0 0 0 0 0 0 0
↑↑ Bit 5 Is not reset with a Stop-Mode Recovery	1↑ (D) 03 CTR3	0 0 0 1 1 1 1 1
↑↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery	↑↑↓ (D) 02 CTR2	000000000
↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0 0 0 0 0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	000000000

# Figure 15. Expanded Register File Architecture



# Timers

# T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

# T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect

## T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

## T16\_Capture\_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

## Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data



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# Capture\_INT\_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

# Counter\_INT\_Mask

Set this bit to allow an interrupt when T8 has a timeout.

# P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

# T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Mode	7	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/	-6	R/W		Transmit Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0*	P31
			1	P20
T8/T16_Logic/	54	R/W		Transmit Mode
Edge _Detect			00**	AND
-			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

### Table 16. CTR1(0D)01H T8 and T16 Common Functions



Field	Bit Position		Value	Description
Transmit_Submode/	32	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

## Table 16.CTR1(0D)01H T8 and T16 Common Functions (Continued)

#### Note:

\*Default at Power-On Reset

\*Default at Power-On Reset. Not reset with Stop Mode recovery.

## Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

## P36\_Out/Demodulator\_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

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Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16\_OUT in Modulo-N Mode

# **T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

# If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

## ZGP323H Product Specification



#### Table 22. Stop Mode Recovery Source

SMR	IR:432 Operation		Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

**Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

## Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the  $T_{POR}$  delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

**Note:** This bit must be set to 1 if using a crystal or resonator clock source. The T<sub>POR</sub> delay allows the clock source to stabilize before executing instructions.

## Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

## Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).



# WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

# **EPROM Selectable Options**

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

## Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

# Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V<sub>DD</sub> is at the required level for correct operation of the device. Reset is globally driven when V<sub>DD</sub> falls below V<sub>BO</sub>. A small drop in V<sub>DD</sub> causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V<sub>DD</sub> is allowed to stay above V<sub>RAM</sub>, the RAM content is preserved. When the power level is returned to above V<sub>BO</sub>, the device performs a POR and functions normally.





# Low-Voltage Detection Register—LVD(D)0Ch

**Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	<b>Bit Position</b>			Description
LVD	76543			Reserved No Effect
	2	R	1 0*	HVD flag set HVD flag reset
	1-	R	1 0*	LVD flag set LVD flag reset
	0	R/W	1 0*	Enable VD Disable VD
*Default	after POR			

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

## **Voltage Detection and Flags**

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V<sub>CC</sub> voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V<sub>CC</sub> level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V<sub>CC</sub> is higher than V<sub>HVD</sub>. The LVD flag (bit 1 of the LVD register) is set only if V<sub>CC</sub> is lower than the V<sub>LVD</sub>. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

**Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.





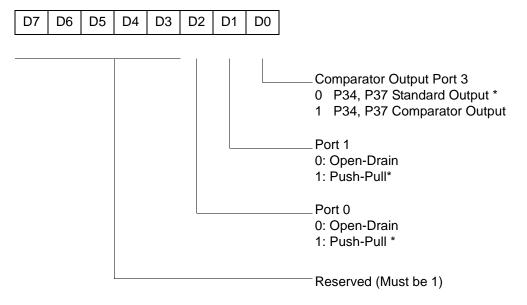


**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



# PCON(0F)00H

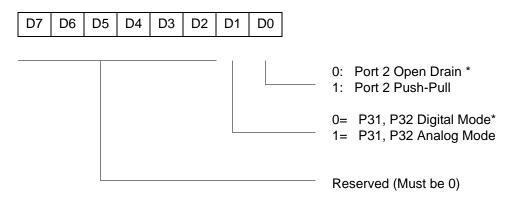


\* Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)



# R247 P3M(F7H)



\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)







Figure 68. 48-Pin SSOP Package Design

**Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.





# 8KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4808C	48-pin SSOP 8K OTP	ZGP323HSS2808C	28-pin SOIC 8K OTP
ZGP323HSP4008C	40-pin PDIP 8K OTP	ZGP323HSH2008C	20-pin SSOP 8K OTP
ZGP323HSH2808C	28-pin SSOP 8K OTP	ZGP323HSP2008C	20-pin PDIP 8K OTP
ZGP323HSP2808C	28-pin PDIP 8K OTP	ZGP323HSS2008C	20-pin SOIC 8K OTP

# 8KB Extended Temperature: -40° to +105°C

-			
Part Number	Description	Part Number	Description
ZGP323HEH4808C	48-pin SSOP 8K OTP	ZGP323HES2808C	28-pin SOIC 8K OTP
ZGP323HEP4008C	40-pin PDIP 8K OTP	ZGP323HEH2008C	20-pin SSOP 8K OTP
ZGP323HEH2808C	28-pin SSOP 8K OTP	ZGP323HEP2008C	20-pin PDIP 8K OTP
ZGP323HEP2808C	28-pin PDIP 8K OTP	ZGP323HES2008C	20-pin SOIC 8K OTP

## 8KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4808C	48-pin SSOP 8K OTP	ZGP323HAS2808C	28-pin SOIC 8K OTP
ZGP323HAP4008C	40-pin PDIP 8K OTP	ZGP323HAH2008C	20-pin SSOP 8K OTP
ZGP323HAH2808C	28-pin SSOP 8K OTP	ZGP323HAP2008C	20-pin PDIP 8K OTP
ZGP323HAP2808C	28-pin PDIP 8K OTP	ZGP323HAS2008C	20-pin SOIC 8K OTP
Replace C with G for	r Lead-Free Packaging		

## ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



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