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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 16 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323hah2032g |

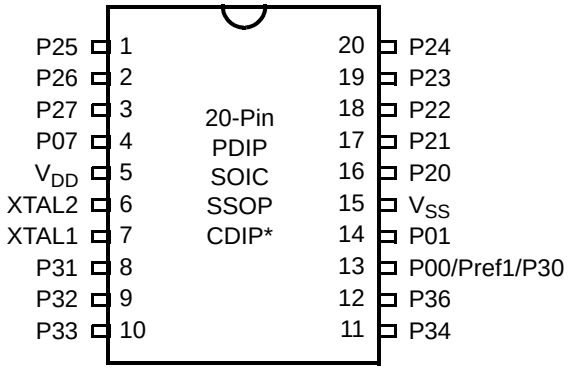



**Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration**

**Table 4. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification**

| Pin # | Symbol | Function | Direction |
|---|---|---|---|
| 1–3 | P25–P27 | Port 2, Bits 5,6,7 | Input/Output |
| 4 | P07 | Port 0, Bit 7 | Input/Output |
| 5 | $V_{DD}$ | Power Supply | |
| 6 | XTAL2 | Crystal Oscillator Clock | Output |
| 7 | XTAL1 | Crystal Oscillator Clock | Input |
| 8–10 | P31–P33 | Port 3, Bits 1,2,3 | Input |
| 11,12 | P34. P36 | Port 3, Bits 4,6 | Output |
| 13 | P00/Pref1/P30 | Port 0, Bit 0/Analog reference input<br>Port 3 Bit 0 | Input/Output for P00<br>Input for Pref1/P30 |
| 14 | P01 | Port 0, Bit 1 | Input/Output |
| 15 | $V_{SS}$ | Ground | |
| 16–20 | P20–P24 | Port 2, Bits 0,1,2,3,4 | Input/Output |

**Table 9. GP323HS DC Characteristics (Continued)**

| | | | $T_A$=0°C to +70°C | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Typ(7)** | **Max** | **Units** | **Conditions** | **Notes** |
| $I_{OL}$ | Output Leakage | 2.0-5.5 | –1 | | 1 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{CC}$ | Supply Current | 2.0V | | 1 | 3 | mA | at 8.0 MHz | 1, 2 |
| | | 3.6V | | 5 | 10 | mA | at 8.0 MHz | 1, 2 |
| | | 5.5V | | 10 | 15 | mA | at 8.0 MHz | 1, 2 |
| $I_{CC1}$ | Standby Current (HALT Mode) | 2.0V | | 0.5 | 1.6 | mA | $V_{IN}$ = 0V, Clock at 8.0MHz | 1, 2, 6 |
| | | 3.6V | | 0.8 | 2.0 | mA | $V_{IN}$ = 0V, Clock at 8.0MHz | 1, 2, 6 |
| | | 5.5V | | 1.3 | 3.2 | mA | $V_{IN}$ = 0V, Clock at 8.0MHz | 1, 2, 6 |
| $I_{CC2}$ | Standby Current (Stop Mode) | 2.0V | | 1.6 | 8 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT not Running | 3 |
| | | 3.6V | | 1.8 | 10 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT not Running | 3 |
| | | 5.5V | | 1.9 | 12 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT not Running | 3 |
| | | 2.0V | | 5 | 20 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT is Running | 3 |
| | | 3.6V | | 8 | 30 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT is Running | 3 |
| | | 5.5V | | 15 | 45 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT is Running | 3 |
| $I_{LV}$ | Standby Current (Low Voltage) | | | 1.2 | 6 | µA | Measured at 1.3V | 4 |
| $V_{BO}$ | $V_{CC}$ Low Voltage Protection | | | 1.9 | 2.0 | V | 8MHz maximum Ext. CLK Freq. | |
| $V_{LVD}$ | $V_{CC}$ Low Voltage Detection | | | 2.4 | | V | | |
| $V_{HVD}$ | Vcc High Voltage Detection | | | 2.7 | | V | | |

**Notes:**
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when $V_{CC}$ falls below $V_{BO}$ limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 µF), physically close to VCC and $V_{SS}$ pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

**Table 10. GP323HE DC Characteristics**

| | | | $T_A$= -40°C to +105°C | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Typ(7)** | **Max** | **Units** | **Conditions** | **Notes** |
| $V_{CC}$ | Supply Voltage | | 2.0 | | 5.5 | V | See Note 5 | 5 |
| $V_{CH}$ | Clock Input High Voltage | 2.0-5.5 | 0.8 $V_{CC}$ | | $V_{CC}$+0.3 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 2.0-5.5 | $V_{SS}$–0.3 | | 0.4 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 2.0-5.5 | 0.7 $V_{CC}$ | | $V_{CC}$+0.3 | V | | |
| $V_{IL}$ | Input Low Voltage | 2.0-5.5 | $V_{SS}$–0.3 | | 0.2 $V_{CC}$ | V | | |
| $V_{OH1}$ | Output High Voltage | 2.0-5.5 | $V_{CC}$–0.4 | | | V | $I_{OH}$ = –0.5mA | |

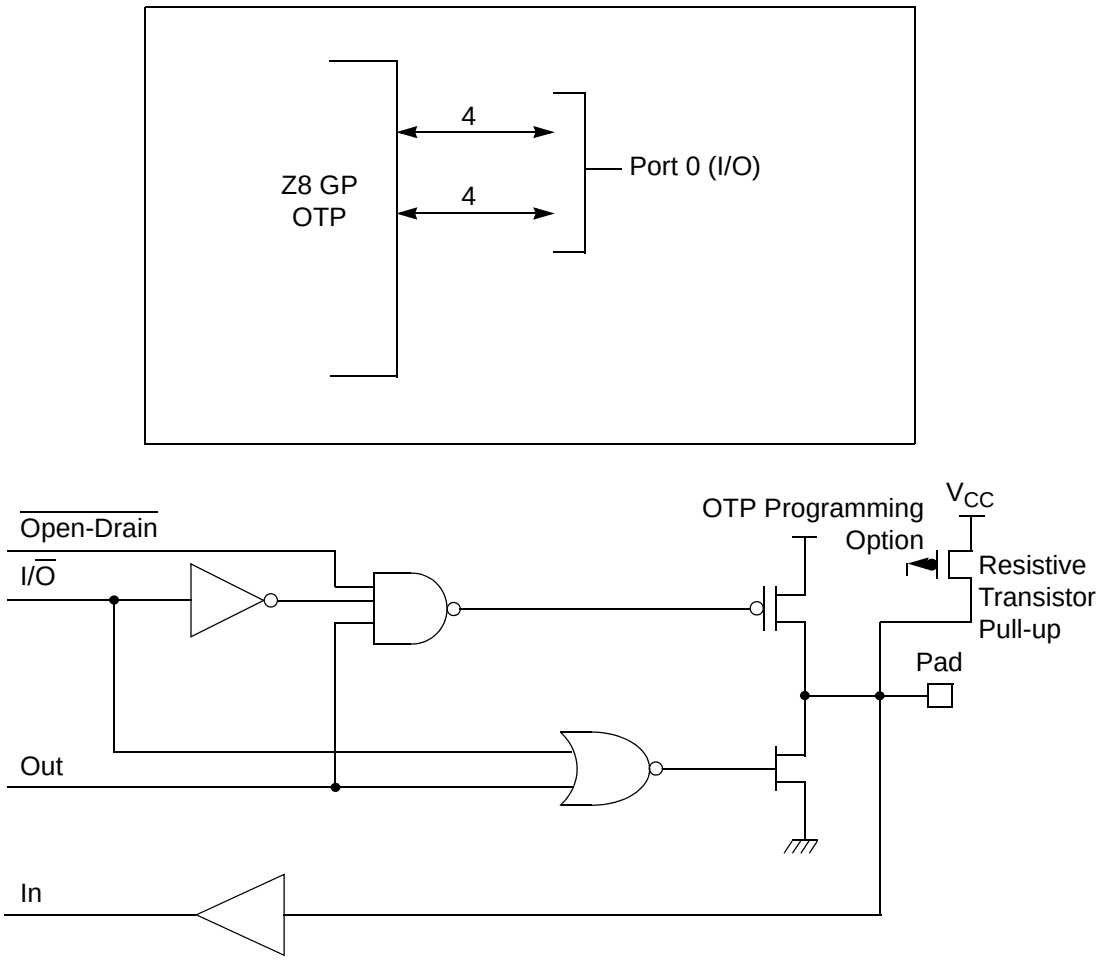



**Figure 9. Port 0 Configuration**

## Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

**Note:** The Port 1 direction is reset to its default state following an SMR.

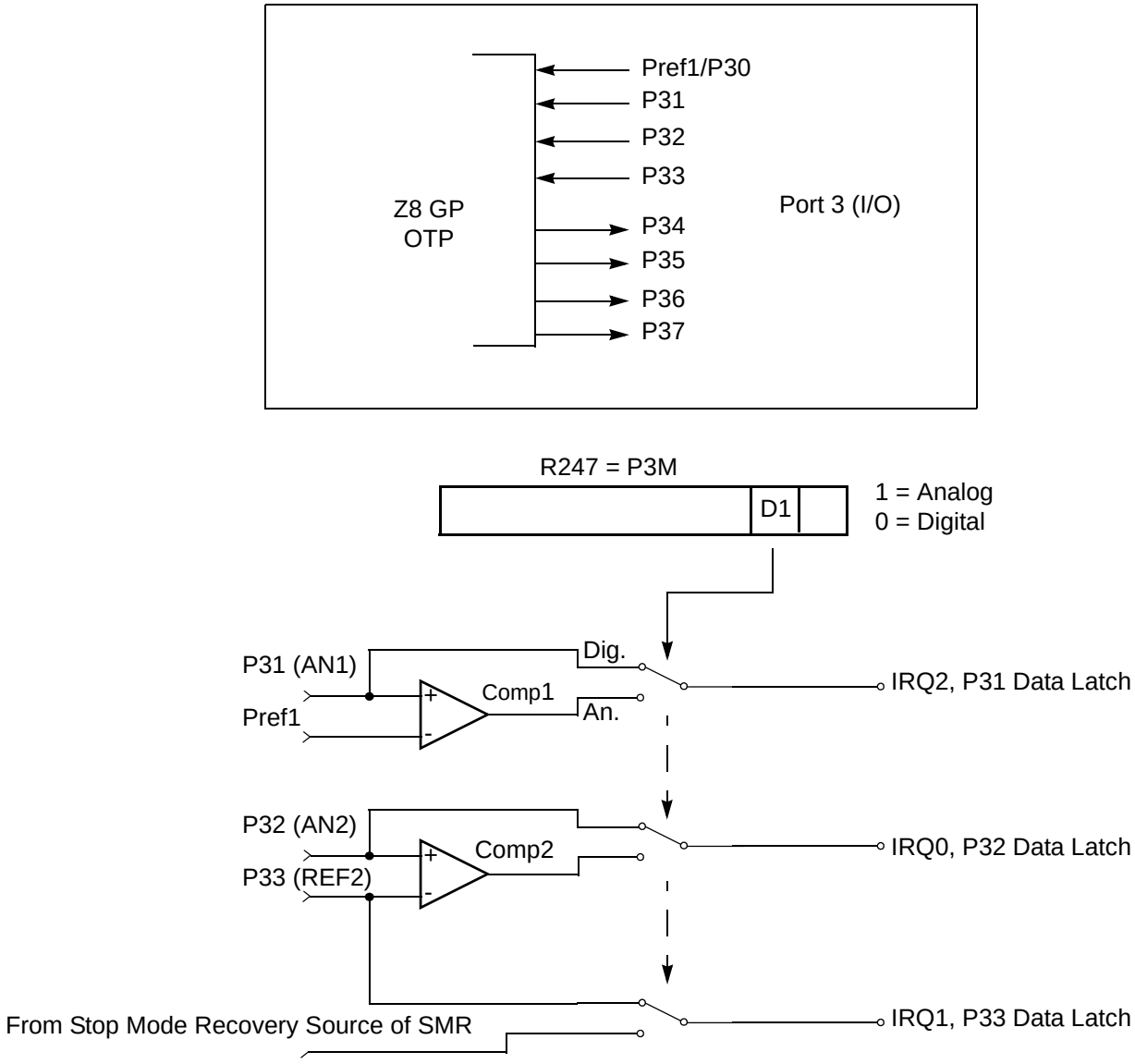



**Figure 12. Port 3 Configuration**

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—

CTR1(0D)01H" on page 35). Other edge detect and IRQ modes are described in Table 14.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

**Table 14. Port 3 Pin Function Summary**

| Pin | I/O | Counter/Timers | Comparator | Interrupt |
|---|---|---|---|---|
| Pref1/P30 | IN | | RF1 | |
| P31 | IN | IN | AN1 | IRQ2 |
| P32 | IN | | AN2 | IRQ0 |
| P33 | IN | | RF2 | IRQ1 |
| P34 | OUT | T8 | AO1 | |
| P35 | OUT | T16 | | |
| P36 | OUT | T8/16 | | |
| P37 | OUT | | AO2 | |
| P20 | I/O | IN | | |

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

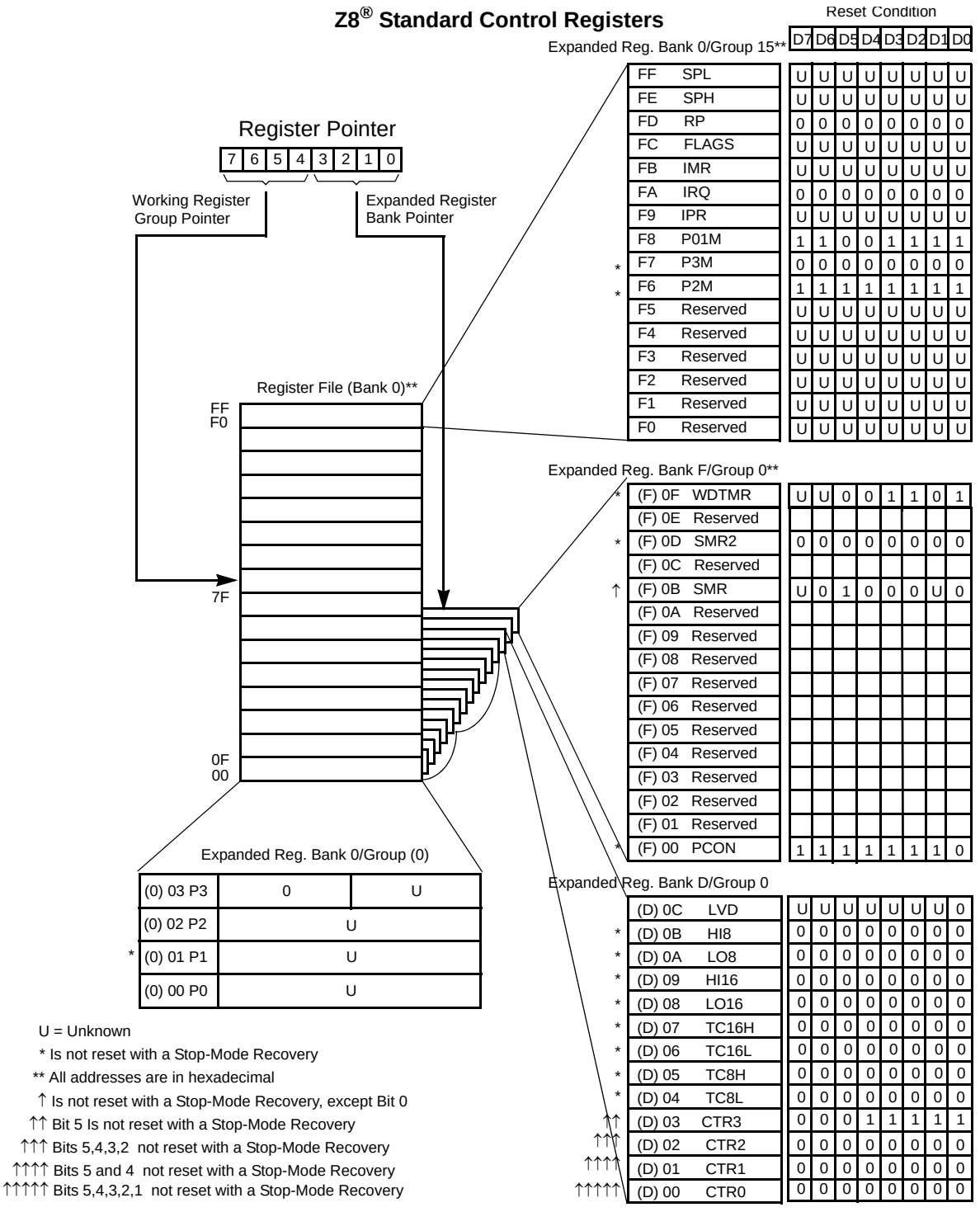



**Figure 15. Expanded Register File Architecture**

## Timers

### T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Capture_HI | [7:0] | R/W | Captured Data - No Effect |

### T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Capture_L0 | [7:0] | R/W | Captured Data - No Effect |

### T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Capture_HI | [7:0] | R/W | Captured Data - No Effect |

### T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Capture_LO | [7:0] | R/W | Captured Data - No Effect |

### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Data_HI | [7:0] | R/W | Data |

### Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

### T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

**Table 16. CTR1(0D)01H T8 and T16 Common Functions**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Mode | 7------- | R/W | 0* | Transmit Mode |
| | | | | Demodulation Mode |
| P36_Out/ | -6------ | R/W | | Transmit Mode |
| Demodulator_Input | | | 0* | Port Output |
| | | | 1 | T8/T16 Output |
| | | | | Demodulation Mode |
| | | | 0* | P31 |
| | | | 1 | P20 |
| T8/T16_Logic/ | --54---- | R/W | | Transmit Mode |
| Edge _Detect | | | 00** | AND |
| | | | 01 | OR |
| | | | 10 | NOR |
| | | | 11 | NAND |
| | | | | Demodulation Mode |
| | | | 00** | Falling Edge |
| | | | 01 | Rising Edge |
| | | | 10 | Both Edges |
| | | | 11 | Reserved |

**Table 16. CTR1(0D)01H T8 and T16 Common Functions (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Transmit_Submode/ Glitch_Filter | ----32-- | R/W | | Transmit Mode |
| | | | 00* | Normal Operation |
| | | | 01 | Ping-Pong Mode |
| | | | 10 | T16_Out = 0 |
| | | | 11 | T16_Out = 1 |
| | | | | Demodulation Mode |
| | | | 00* | No Filter |
| | | | 01 | 4 SCLK Cycle |
| | | | 10 | 8 SCLK Cycle |
| | | | 11 | Reserved |
| Initial_T8_Out/ Rising Edge | ------1- | | | Transmit Mode |
| | | R/W | 0* | T8_OUT is 0 Initially |
| | | | 1 | T8_OUT is 1 Initially |
| | | | | Demodulation Mode |
| | | R | 0* | No Rising Edge |
| | | | 1 | Rising Edge Detected |
| | | W | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |
| Initial_T16_Out/ Falling_Edge | -------0 | | | Transmit Mode |
| | | R/W | 0* | T16_OUT is 0 Initially |
| | | | 1 | T16_OUT is 1 Initially |
| | | | | Demodulation Mode |
| | | R | 0* | No Falling Edge |
| | | | 1 | Falling Edge Detected |
| | | W | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |

**Note:**
*Default at Power-On Reset
*Default at Power-On Reset. Not reset with Stop Mode recovery.

### Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

### P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

**Caution:** Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFEH. Transition from 0 to FFFFH is not a timeout condition.

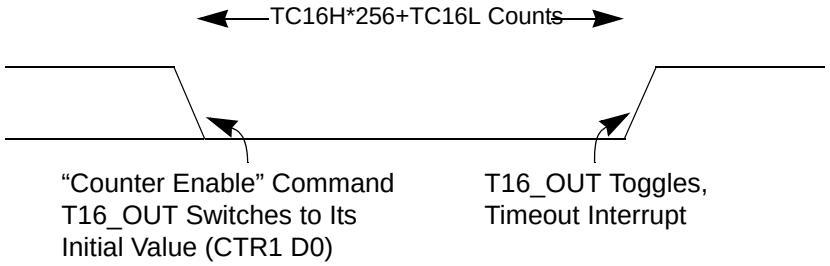



**Figure 26. T16_OUT in Single-Pass Mode**

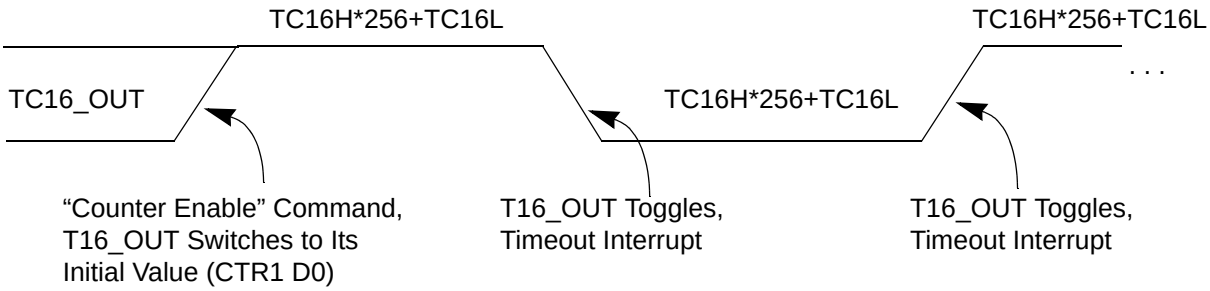



**Figure 27. T16_OUT in Modulo-N Mode**

### T16 DEMODULATION Mode

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

### If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

**Table 22. Stop Mode Recovery Source**

| SMR:432 | | | Operation |
|---|---|---|---|
| **D4** | **D3** | **D2** | **Description of Action** |
| 0 | 0 | 0 | POR and/or external reset recovery |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | P31 transition |
| 0 | 1 | 1 | P32 transition |
| 1 | 0 | 0 | P33 transition |
| 1 | 0 | 1 | P27 transition |
| 1 | 1 | 0 | Logical NOR of P20 through P23 |
| 1 | 1 | 1 | Logical NOR of P20 through P27 |

**Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

### Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the $T_{POR}$ delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

**Note:** This bit must be set to 1 if using a crystal or resonator clock source. The $T_{POR}$ delay allows the clock source to stabilize before executing instructions.

### Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

### Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

**Table 24. EPROM Selectable Options**

| | |
|---|---|
| Port 00–03 Pull-Ups | On/Off |
| Port 04–07 Pull-Ups | On/Off |
| Port 10–13 Pull-Ups | On/Off |
| Port 14–17 Pull-Ups | On/Off |
| Port 20–27 Pull-Ups | On/Off |
| EPROM Protection | On/Off |
| Watch-Dog Timer at Power-On Reset | On/Off |

### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the $V_{DD}$ is at the required level for correct operation of the device. Reset is globally driven when $V_{DD}$ falls below $V_{BO}$. A small drop in $V_{DD}$ causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the $V_{DD}$ is allowed to stay above $V_{RAM}$, the RAM content is preserved. When the power level is returned to above $V_{BO}$, the device performs a POR and functions normally.

### Low-Voltage Detection Register—LVD(D)0Ch

**Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

| Field | Bit Position | | | Description |
|---|---|---|---|---|
| LVD | 76543--- | | | Reserved<br>No Effect |
| | -----2-- | R | 1<br>0* | HVD flag set<br>HVD flag reset |
| | ------1- | R | 1<br>0* | LVD flag set<br>LVD flag reset |
| | -------0 | R/W | 1<br>0* | Enable VD<br>Disable VD |

***Default after POR

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

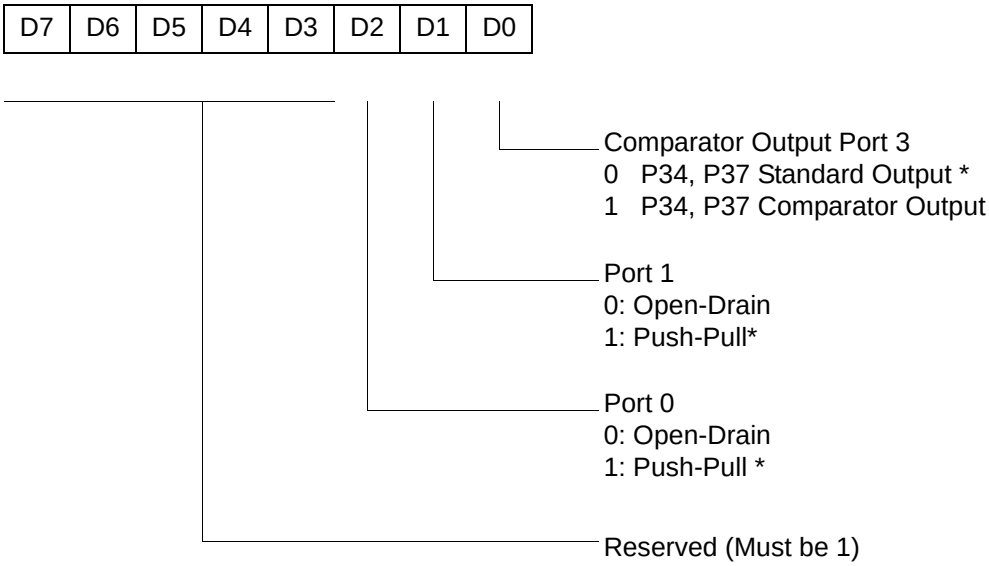
The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the $V_{CC}$ voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the $V_{CC}$ level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if $V_{CC}$ is higher than $V_{HVD.}$ The LVD flag (bit 1 of the LVD register) is set only if $V_{CC}$ is lower than the $V_{LVD}$. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

**Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

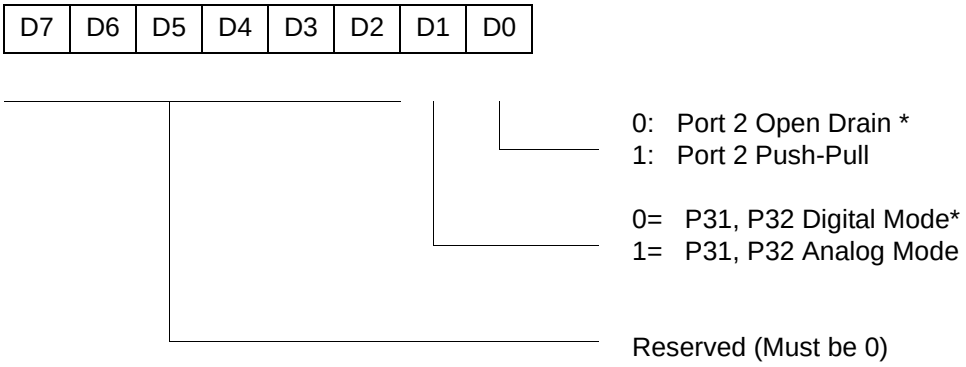
PCON(0F)00H




* Default setting after reset

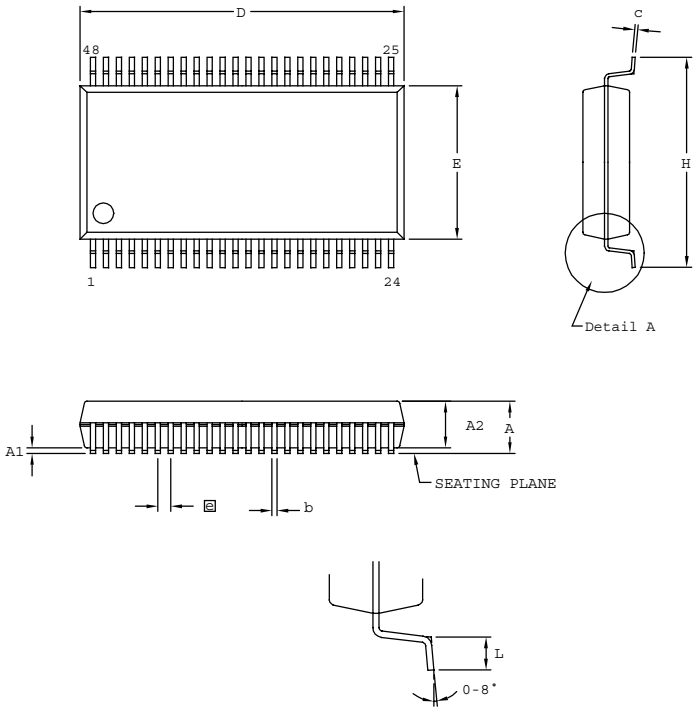
**Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)**

R247 P3M(F7H)




* Default setting after reset. Not reset with a Stop Mode recovery.

**Figure 49. Port 3 Mode Register (F7H: Write Only)**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.79 | 0.095 | 0.110 |
| A1 | 0.23 | 0.38 | 0.009 | 0.015 |
| A2 | 2.18 | 2.39 | 0.086 | 0.094 |
| b | 0.20 | 0.34 | 0.008 | 0.0135 |
| c | 0.13 | 0.25 | 0.005 | 0.010 |
| D | 15.75 | 16.00 | 0.620 | 0.630 |
| E | 7.39 | 7.59 | 0.291 | 0.299 |
| e | 0.635 BSC | | 0.025 BSC | |
| H | 10.16 | 10.41 | 0.400 | 0.410 |
| L | 0.51 | 1.016 | 0.020 | 0.040 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

**Figure 68. 48-Pin SSOP Package Design**

**Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

| 8KB Standard Temperature: 0° to +70°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HSH4808C | 48-pin SSOP 8K OTP | ZGP323HSS2808C | 28-pin SOIC 8K OTP |
| ZGP323HSP4008C | 40-pin PDIP 8K OTP | ZGP323HSH2008C | 20-pin SSOP 8K OTP |
| ZGP323HSH2808C | 28-pin SSOP 8K OTP | ZGP323HSP2008C | 20-pin PDIP 8K OTP |
| ZGP323HSP2808C | 28-pin PDIP 8K OTP | ZGP323HSS2008C | 20-pin SOIC 8K OTP |

| 8KB Extended Temperature: -40° to +105°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HEH4808C | 48-pin SSOP 8K OTP | ZGP323HES2808C | 28-pin SOIC 8K OTP |
| ZGP323HEP4008C | 40-pin PDIP 8K OTP | ZGP323HEH2008C | 20-pin SSOP 8K OTP |
| ZGP323HEH2808C | 28-pin SSOP 8K OTP | ZGP323HEP2008C | 20-pin PDIP 8K OTP |
| ZGP323HEP2808C | 28-pin PDIP 8K OTP | ZGP323HES2008C | 20-pin SOIC 8K OTP |

| 8KB Automotive Temperature: -40° to +125°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HAH4808C | 48-pin SSOP 8K OTP | ZGP323HAS2808C | 28-pin SOIC 8K OTP |
| ZGP323HAP4008C | 40-pin PDIP 8K OTP | ZGP323HAH2008C | 20-pin SSOP 8K OTP |
| ZGP323HAH2808C | 28-pin SSOP 8K OTP | ZGP323HAP2008C | 20-pin PDIP 8K OTP |
| ZGP323HAP2808C | 28-pin PDIP 8K OTP | ZGP323HAS2008C | 20-pin SOIC 8K OTP |
| Replace C with G for Lead-Free Packaging | | | |