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#### Zilog - ZGP323HAH2804C00TR Datasheet



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#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hah2804c00tr

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Figure 68.	48-Pin SSOP Package Design		J







#### Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 4.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output





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NC		1	-		40	þ	NC
P25		2			39	Þ	P24
P26		3			38		P23
P27		4			37	Þ	P22
P04		5			36	Þ	P21
P05	q	6			35		P20
P06	Ц	7			34	Þ	P03
P14	С	8	40-Pir	۱	33	Þ	P13
P15		9			32		P12
P07	Ц	10	CDIP		31	Þ	VSS
VDD		11			30		P02
P16		12			39		P11
P17	С	13			28		P10
XTAL2		14			27		P01
XTAL1	С	15			26		P00
P31		16			25		Pref1/P30
P32	С	17			24		P36
P33	q	18			23		P37
P34	С	19			22	þ	P35
NC	Ц	20			21	Þ	RESET
	_						

## Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration

**Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

## ZGP323H Product Specification



40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V <sub>DD</sub>
31	24, 37, 38	V <sub>SS</sub>
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC

## Table 6. 40- and 48-Pin Configuration (Continued)



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## **Comparator Inputs**

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

#### **Comparator Outputs**

These channels can be programmed to be output on P34 and P37 through the PCON register.

## **RESET (Input, Active Low)**

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the  $\overline{\text{RESET}}$  pin, the internal pull-up is disabled. The Z8 GP does not assert the  $\overline{\text{RESET}}$  pin when under VBO.



**Note:** The external Reset does not initiate an exit from STOP mode.

# **Functional Description**

This device incorporates special functions to enhance the Z8<sup>®</sup>, functionality in consumer and battery-operated applications.

## **Program Memory**

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

#### RAM

This device features 256B of RAM. See Figure 14.

## ZGP323H Product Specification



Location of 3	2768	Not Accessible
first Byte of	-100	On-Chip
executed		KOM
after RESET	12	Reset Start Address
	11	IRQ5
	10	IRQ5
	9	IRQ4
	8	IRQ4
Interrupt Vector	7	IRQ3
(Lower Byte)	6	IRQ3
	5	IRQ2
Interrupt Vector	4	→ IRQ2
(Upper Byte)	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0



## **Expanded Register File**

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8<sup>®</sup> register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

**Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).







Figure 17. Register Pointer—Detail

## Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



Field	Bit Position		Value	Description
Transmit_Submode/	32	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

#### Table 16.CTR1(0D)01H T8 and T16 Common Functions (Continued)

#### Note:

\*Default at Power-On Reset

\*Default at Power-On Reset. Not reset with Stop Mode recovery.

#### Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

#### P36\_Out/Demodulator\_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.



#### T8/T16\_Logic/Edge \_Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

#### Transmit\_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to "NORMAL OPERATION Mode" terminates the "PING-PONG Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

#### Initial\_T8\_Out/Rising\_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

#### Initial\_T16 Out/Falling \_Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

**Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16\_OUT.

#### CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8\_OUT in Modulo-N Mode

## **T8 Demodulation Mode**

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put



## Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

#### Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.







Figure 35. Stop Mode Recovery Source



## Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved (Must be 0) Reserved (Must be 0) Stop-Mode Recovery Source 2 000 POR Only * 001 NAND P20, P21, P22, P23 010 NAND P20, P21, P22, P23, P24, P25, P26, P27 011 NOR P31, P32, P33 100 NAND P31, P32, P33 101 NOR P31, P32, P33, P00, P07 110 NAND P31, P32, P33, P00, P07
								111 NAND P31, P32, P33, P20, P21, P22
								Reserved (Must be 0)
								Recovery Level * * 0 Low * 1 High
								Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset

\* \* At the XOR gate input

#### Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.



**Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.





CI	R1(0L	)01H							
D7	D6	D5	D4	D3	D2	D1	D0		
									Transmit Mode* R/W 0 T16_OUT is 0 initially 1 T16_OUT is 1 initially Demodulation Mode R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially Demodulation Mode R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 Demodulation Mode 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 1 Reserved Transmit Mode/T8/T16 Logic 0 0 AND** 0 1 0R 1 0 NOR 1 1 NAND Demodulation Mode 0 0 Falling Edge Detection 0 1 Rising Edge Detection
									1 0 Both Edge Detection 1 0 Both Edge Detection 1 1 Reserved Transmit Mode* 0 P36 as Port Output *
									1 P36 as T8/T16_OUT Demodulation Mode 0 P31 as Demodulator Input 1 P20 as Demodulator Input
* De **De reco	efault se efault se overy.	etting aft etting aft	er Res er Res	et et Not	reset	with a S	Stop-N	lode	Transmit/Demodulation Mode 0 Transmit Mode * 1 Demodulation Mode

Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)







**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



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#### CTR2(0D)02H



Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)



## LVD(0D)0CH



\* Default setting after reset.

#### Figure 43. Voltage Detection Register

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

# **Expanded Register File Control Registers (0F)**

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.





Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset. Not reset with a Stop Mode recovery.

\* \* At the XOR gate input

#### Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)



#### WDTMR(0F)0FH



\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

# **Standard Control Registers**

#### R246 P2M(F6H)



\* Default setting after reset. Not reset with a Stop Mode recovery.

#### Figure 48. Port 2 Mode Register (F6H: Write Only)