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Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323hah2804g |



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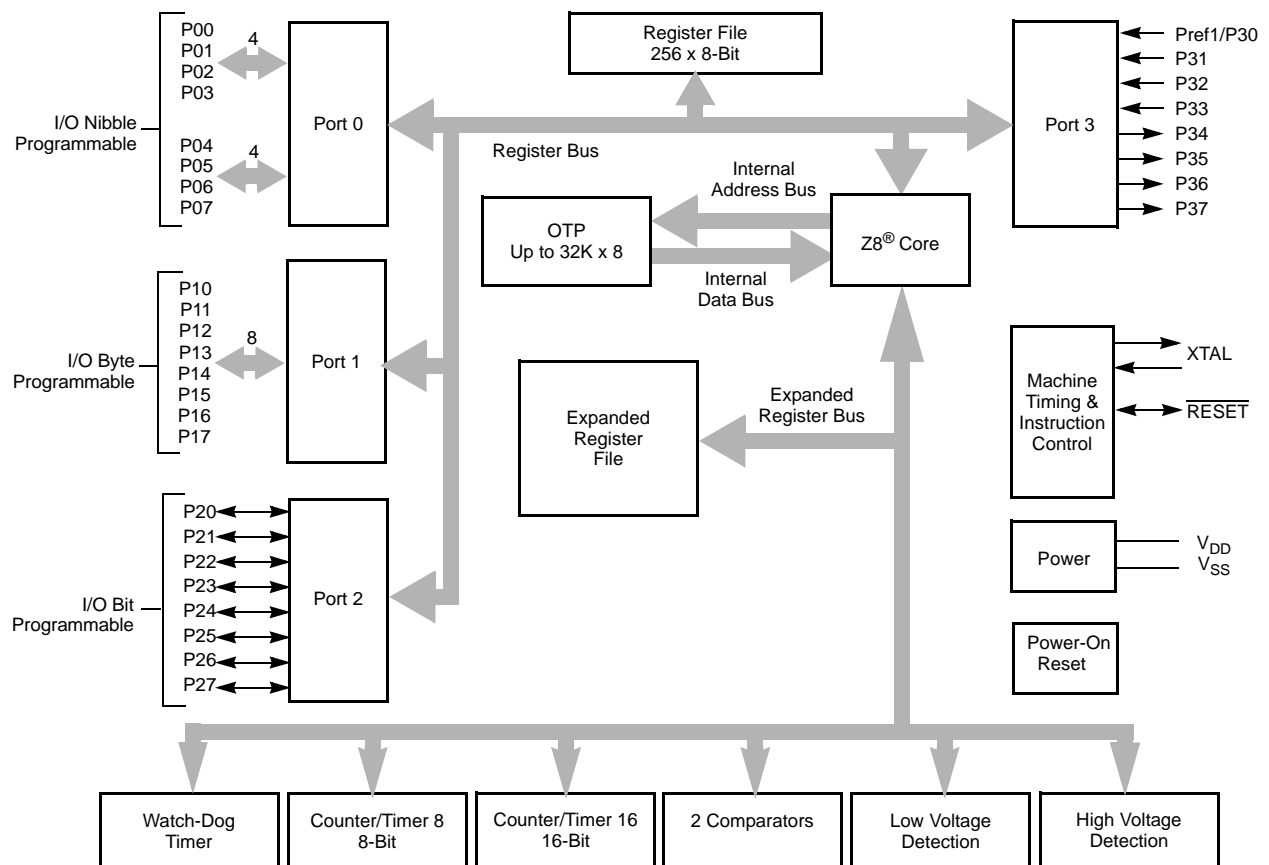


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Table 3. Power Connections

| Connection | Circuit | Device |
|------------|-----------------|-----------------|
| Power | V _{CC} | V _{DD} |
| Ground | GND | V _{SS} |



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

Absolute Maximum Ratings

Stresses greater than those listed in Table 8 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 7. Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Units | Notes |
|---|---------|---------|---------|-------|
| Ambient temperature under bias | -40 | 125 | ° C | 1 |
| Storage temperature | -65 | +150 | ° C | |
| Voltage on any pin with respect to V_{SS} | -0.3 | 7.0 | V | 2 |
| Voltage on V_{DD} pin with respect to V_{SS} | -0.3 | 7.0 | V | |
| Maximum current on input and/or inactive output pin | -5 | +5 | μ A | |
| Maximum output current from active output pin | -25 | +25 | mA | |
| Maximum current into V_{DD} or out of V_{SS} | | 75 | mA | |

Notes:

1. See Ordering Information.
2. This voltage applies to all pins except the following: V_{DD} , P32, P33 and RESET.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

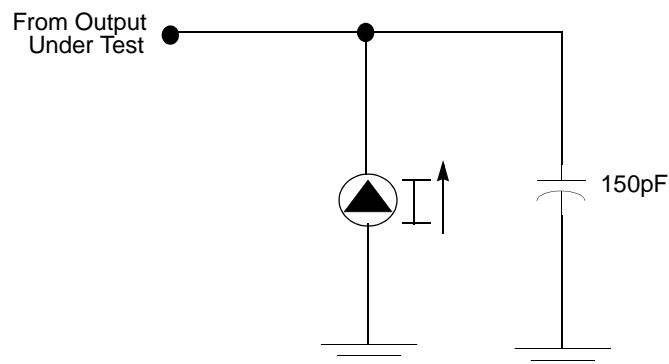


Figure 7. Test Load Diagram

Table 11. GP323HA DC Characteristics

| T_A = -40°C to +125°C | | | | | | | | |
|--|--|-----------------------|----------------------|---------------|-----------------------|--------------|---|--------------|
| Symbol | Parameter | V_{CC} | Min | Typ(7) | Max | Units | Conditions | Notes |
| V _{CC} | Supply Voltage | | 2.0 | | 5.5 | V | See Note 5 | 5 |
| V _{CH} | Clock Input High Voltage | 2.0-5.5 | 0.8 V _{CC} | | V _{CC} +0.3 | V | Driven by External Clock Generator | |
| V _{CL} | Clock Input Low Voltage | 2.0-5.5 | V _{SS} -0.3 | | 0.4 | V | Driven by External Clock Generator | |
| V _{IH} | Input High Voltage | 2.0-5.5 | 0.7 V _{CC} | | V _{CC} +0.3 | V | | |
| V _{IL} | Input Low Voltage | 2.0-5.5 | V _{SS} -0.3 | | 0.2 V _{CC} | V | | |
| V _{OH1} | Output High Voltage | 2.0-5.5 | V _{CC} -0.4 | | | V | I _{OH} = -0.5mA | |
| V _{OH2} | Output High Voltage (P36, P37, P00, P01) | 2.0-5.5 | V _{CC} -0.8 | | | V | I _{OH} = -7mA | |
| V _{OL1} | Output Low Voltage | 2.0-5.5 | | | 0.4 | V | I _{OL} = 4.0mA | |
| V _{OL2} | Output Low Voltage (P00, P01, P36, P37) | 2.0-5.5 | | | 0.8 | V | I _{OL} = 10mA | |
| V _{OFFSET} | Comparator Input Offset Voltage | 2.0-5.5 | | | 25 | mV | | |
| V _{REF} | Comparator Reference Voltage | 2.0-5.5 | 0 | | V _{DD} -1.75 | V | | |
| I _{IL} | Input Leakage | 2.0-5.5 | -1 | | 1 | μA | V _{IN} = 0V, V _{CC} Pull-ups disabled | |
| R _{PU} | Pull-up Resistance | 2.0V | 200 | | 700 | KΩ | V _{IN} = 0V; Pullups selected by mask option | |
| | | 3.6V | 50 | | 300 | KΩ | | |
| | | 5.0V | 25 | | 175 | KΩ | | |
| I _{OL} | Output Leakage | 2.0-5.5 | -1 | | 1 | μA | V _{IN} = 0V, V _{CC} | |
| I _{CC} | Supply Current | 2.0V | | 1 | 3 | mA | at 8.0 MHz | 1, 2 |
| | | 3.6V | | 5 | 10 | mA | at 8.0 MHz | 1, 2 |
| | | 5.5V | | 10 | 15 | mA | at 8.0 MHz | 1, 2 |
| I _{CC1} | Standby Current (HALT Mode) | 2.0V | | 0.5 | 1.6 | mA | V _{IN} = 0V, Clock at 8.0MHz | 1, 2, 6 |
| | | 3.6V | | 0.8 | 2.0 | mA | V _{IN} = 0V, Clock at 8.0MHz | 1, 2, 6 |
| | | 5.5V | | 1.3 | 3.2 | mA | V _{IN} = 0V, Clock at 8.0MHz | 1, 2, 6 |
| I _{CC2} | Standby Current (Stop Mode) | 2.0V | | 1.6 | 15 | μA | V _{IN} = 0 V, V _{CC} WDT not Running | 3 |
| | | 3.6V | | 1.8 | 20 | μA | V _{IN} = 0 V, V _{CC} WDT not Running | 3 |
| | | 5.5V | | 1.9 | 25 | μA | V _{IN} = 0 V, V _{CC} WDT not Running | 3 |
| | | 2.0V | | 5 | 30 | μA | V _{IN} = 0 V, V _{CC} WDT is Running | 3 |
| | | 3.6V | | 8 | 40 | μA | V _{IN} = 0 V, V _{CC} WDT is Running | 3 |
| | | 5.5V | | 15 | 60 | μA | V _{IN} = 0 V, V _{CC} WDT is Running | 3 |
| | | | | | | | | |
| I _{LV} | Standby Current (Low Voltage) | | | 1.2 | 6 | μA | Measured at 1.3V | 4 |
| V _{BO} | V _{CC} Low Voltage Protection | | | 1.9 | 2.15 | V | 8MHz maximum Ext. CLK Freq. | |
| V _{LVD} | V _{CC} Low Voltage Detection | | | 2.4 | | V | | |

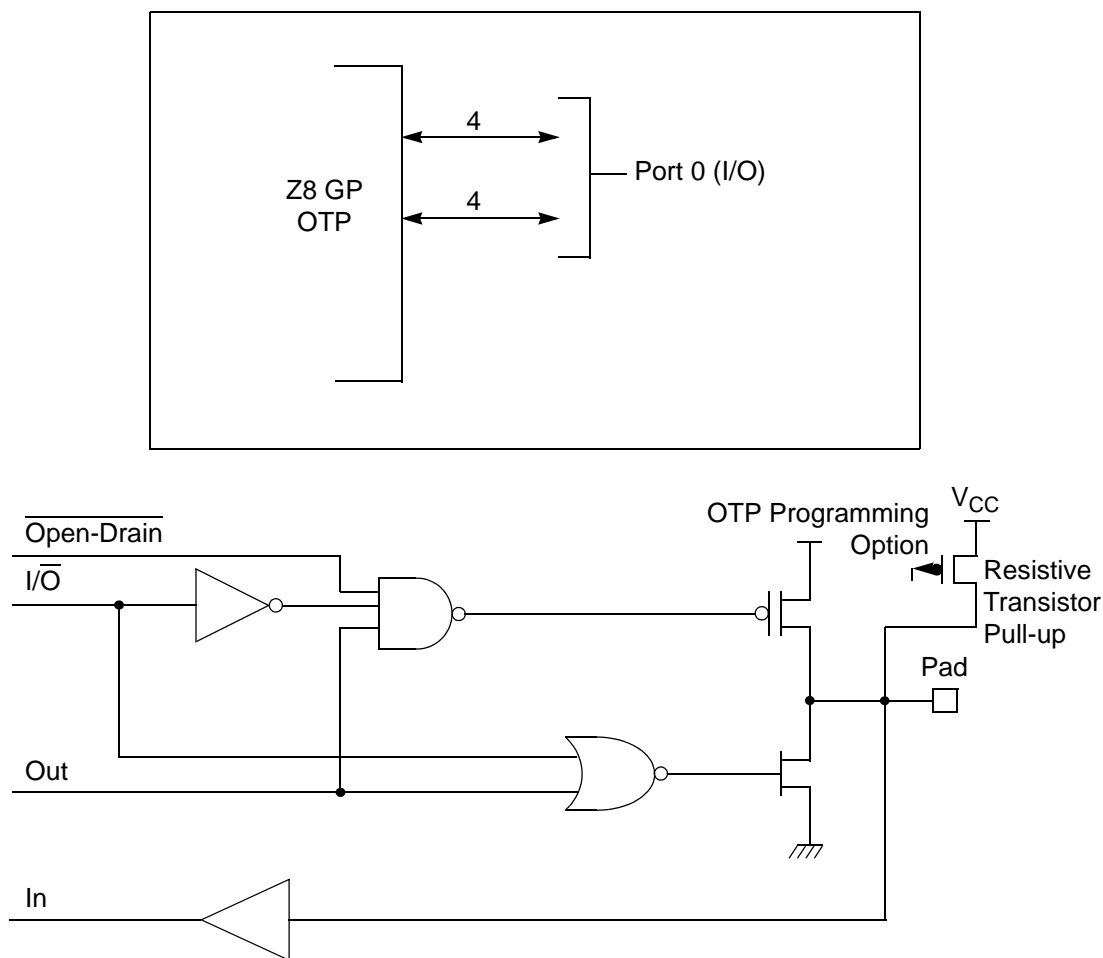


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to its default state following an SMR.

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

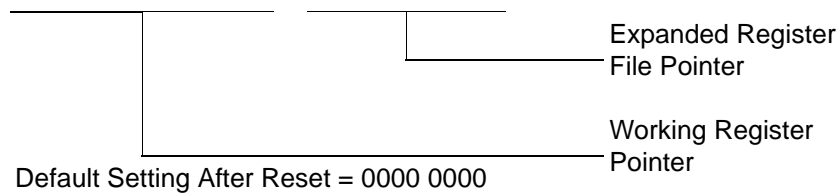


Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 28)

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = Reserved



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          R0, #xx          ; load CTR0
LD          1, #xx          ; load CTR1
LD          R1, 2            ; CTR2→CTR1

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          RP, #7Dh          ; Select
expanded register bank D and working ; register
group 7 of bank 0 for access.
LD          71h, 2
; CTRL2→register 71h
LD          R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 15) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.



Table 16. CTR1(0D)01H T8 and T16 Common Functions (Continued)

| Field | Bit Position | | Value | Description |
|------------------------------------|--------------|-----|-------|------------------------|
| Transmit_Submode/ Glitch_Filter | ----32-- | R/W | | Transmit Mode |
| | | | 00* | Normal Operation |
| | | | 01 | Ping-Pong Mode |
| | | | 10 | T16_Out = 0 |
| | | | 11 | T16_Out = 1 |
| | | | | Demodulation Mode |
| | | | 00* | No Filter |
| | | | 01 | 4 SCLK Cycle |
| | | | 10 | 8 SCLK Cycle |
| | | | 11 | Reserved |
| Initial_T8_Out/ Rising Edge | -----1- | R/W | 0* | Transmit Mode |
| | | | 1 | T8_OUT is 0 Initially |
| | | R | 0* | T8_OUT is 1 Initially |
| | | | 1 | Demodulation Mode |
| | | W | 0 | No Rising Edge |
| | | | 1 | Rising Edge Detected |
| | | | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |
| Initial_T16_Out/ Falling_Edge | -----0 | R/W | 0* | Transmit Mode |
| | | | 1 | T16_OUT is 0 Initially |
| | | R | 0* | T16_OUT is 1 Initially |
| | | | 1 | Demodulation Mode |
| | | W | 0 | No Falling Edge |
| | | | 1 | Falling Edge Detected |
| | | | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |

Note:

*Default at Power-On Reset

*Default at Power-On Reset. Not reset with Stop Mode recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

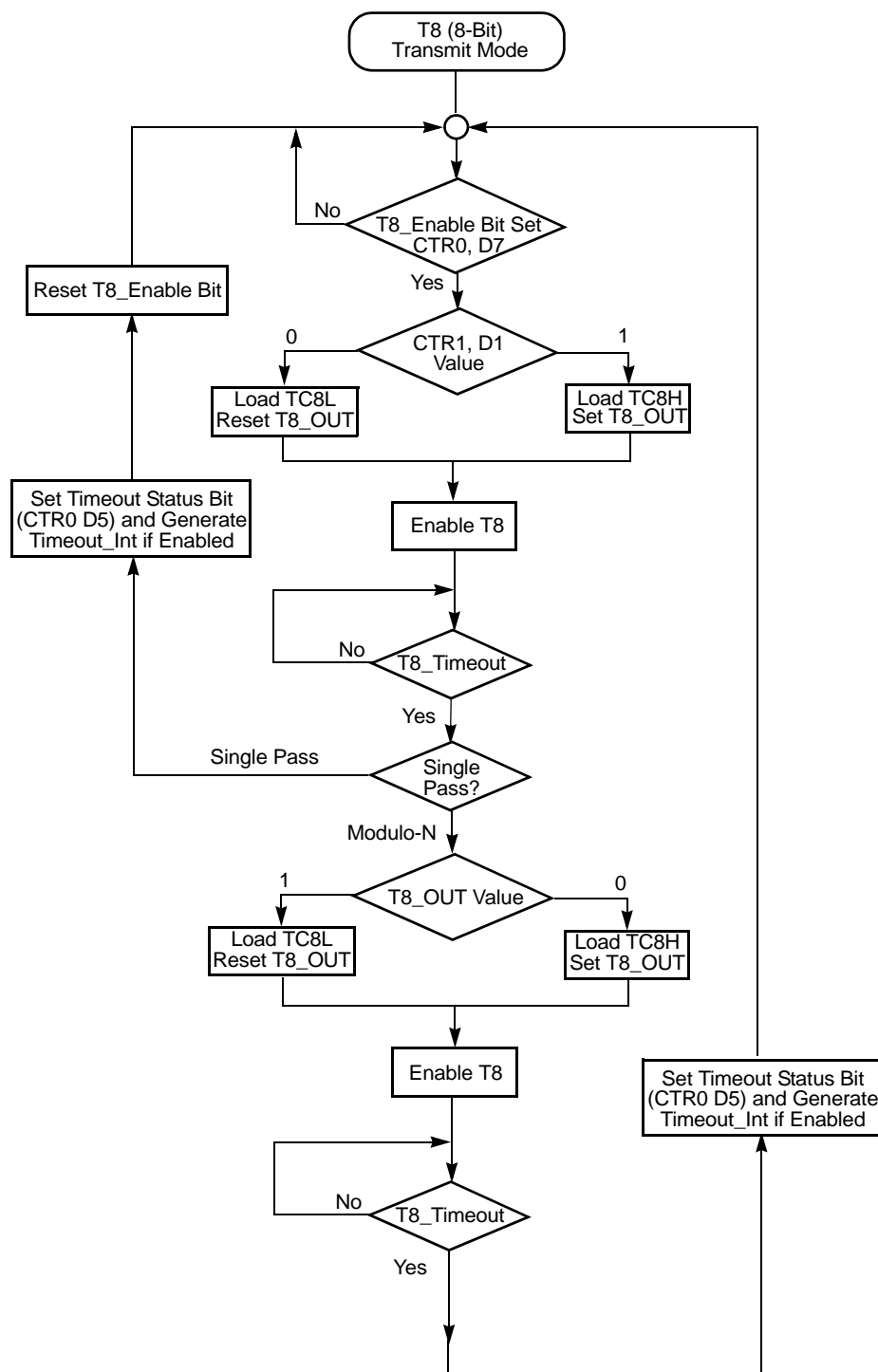


Figure 19. Transmit Mode Flowchart

► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF_h is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.

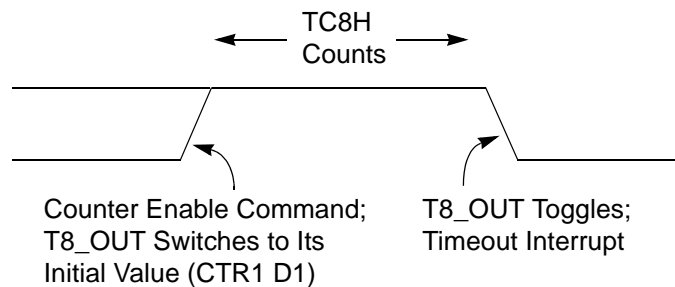


Figure 21. T8_OUT in Single-Pass Mode

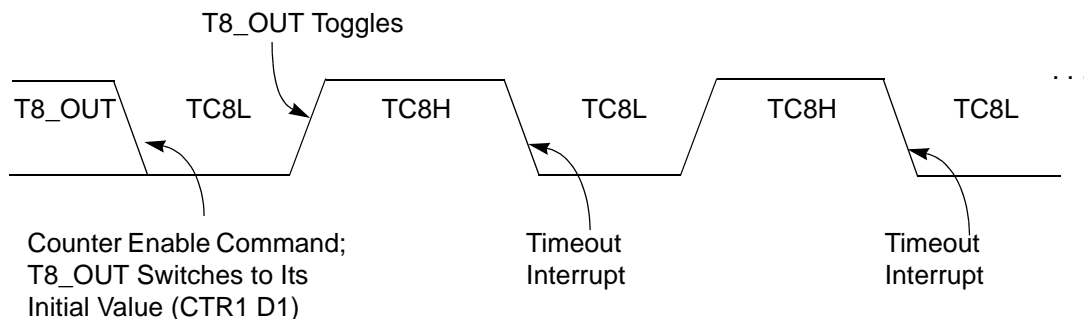


Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FF_h. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

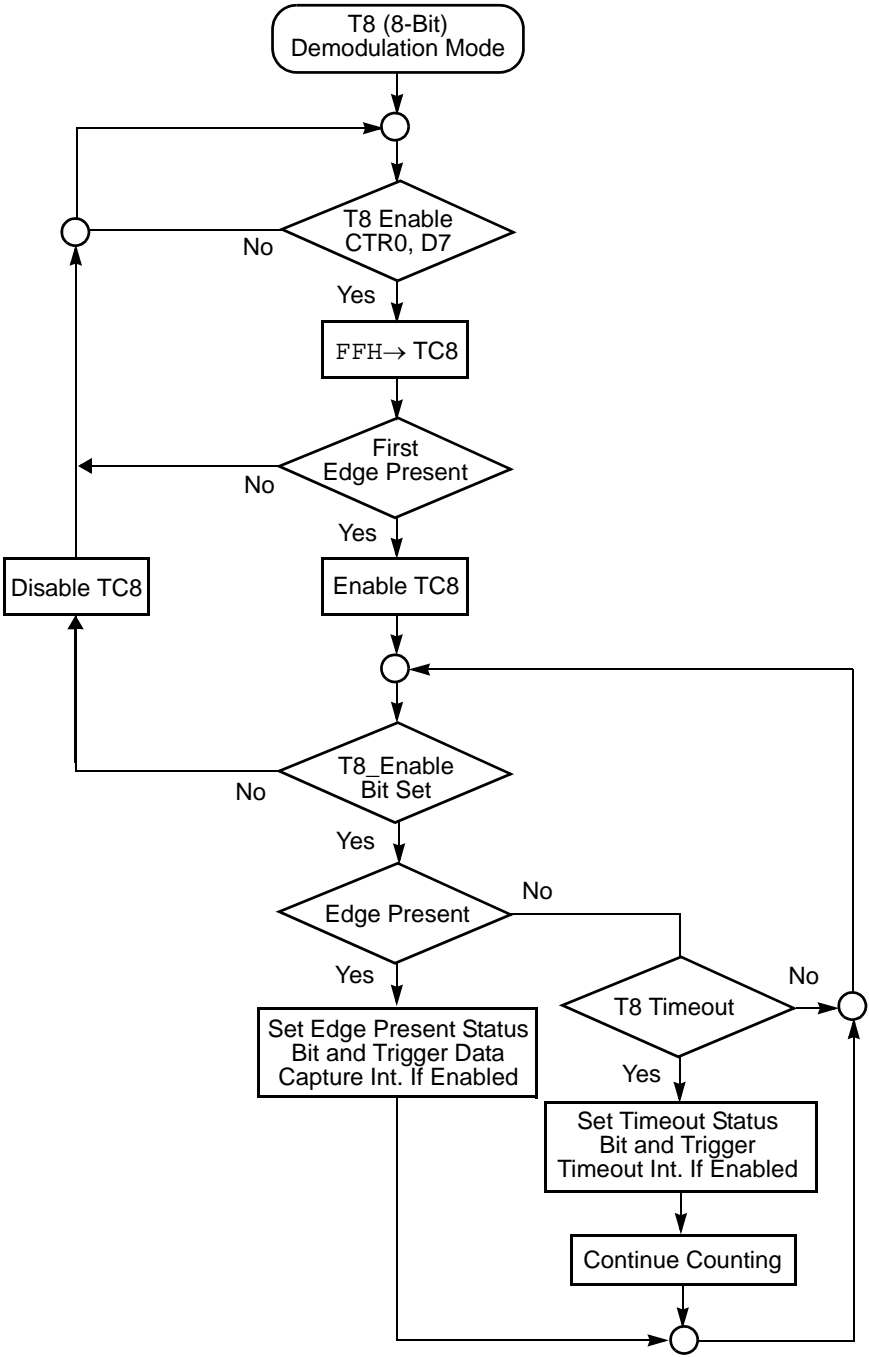


Figure 24. Demodulation Mode Flowchart



During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Interrupts

The ZGP323H features six different interrupts (Table 19). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 19) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 59.



Port 0 Output Mode (D2)

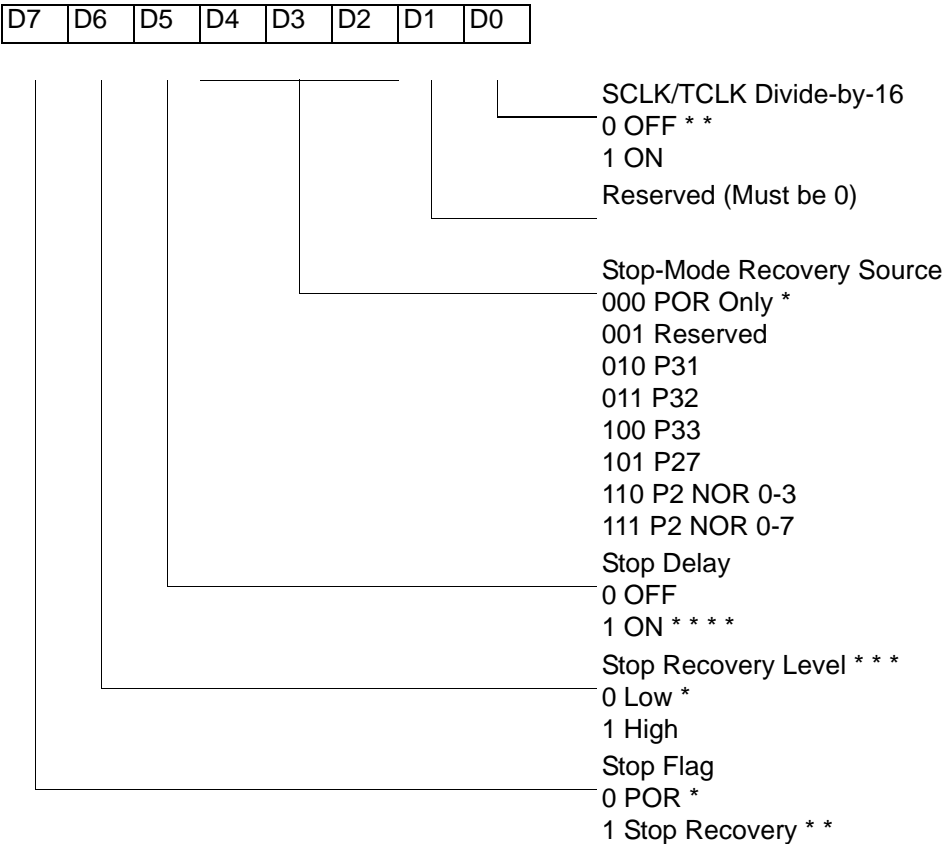
Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.



SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset
* * Default setting after Reset and Stop Mode Recovery
* * * At the XOR gate input
* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

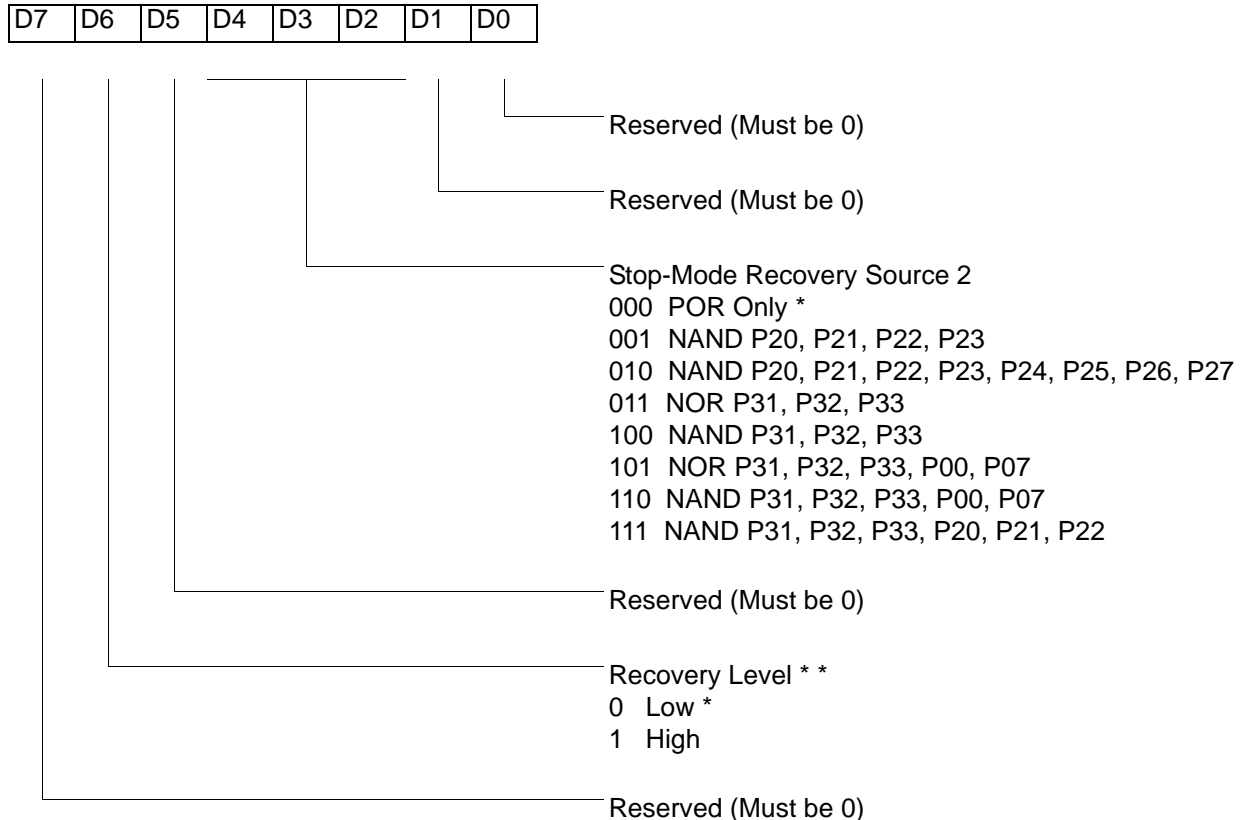
SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

** At the XOR gate input

Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

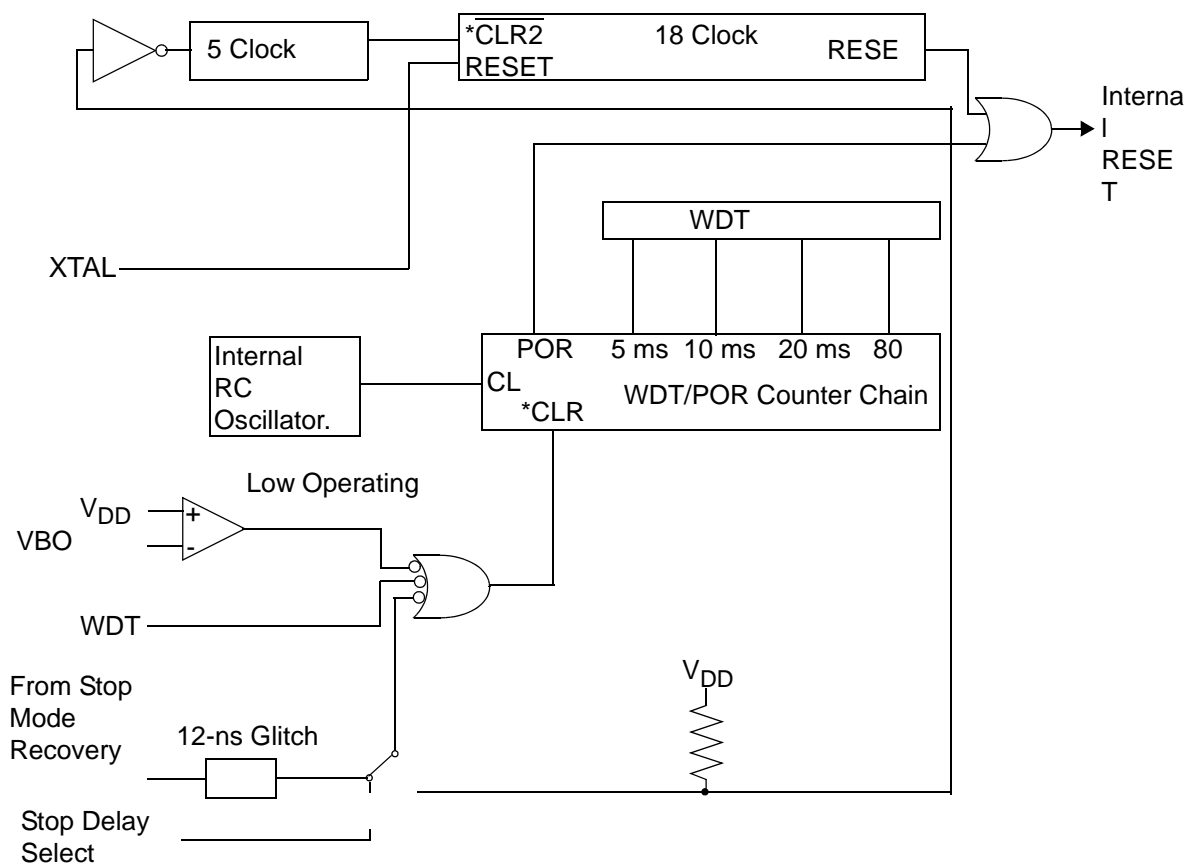
► **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

Table 23. Watch-Dog Timer Time Select

| D1 | D0 | Timeout of Internal RC-Oscillator |
|----|----|-----------------------------------|
| 0 | 0 | 5ms min. |
| 0 | 1 | 10ms min. |
| 1 | 0 | 20ms min. |
| 1 | 1 | 80ms min. |

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



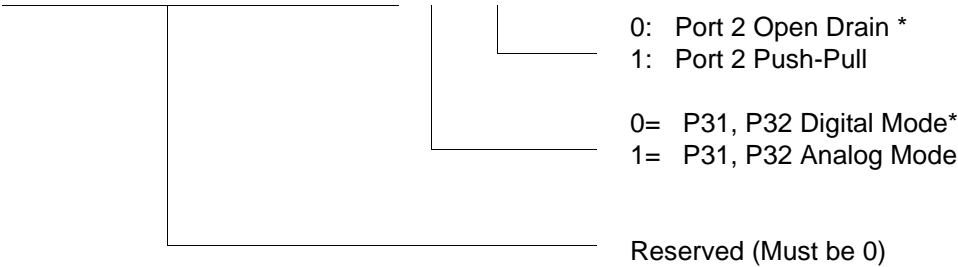
* CLR1 and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-

Figure 38. Resets and WDT



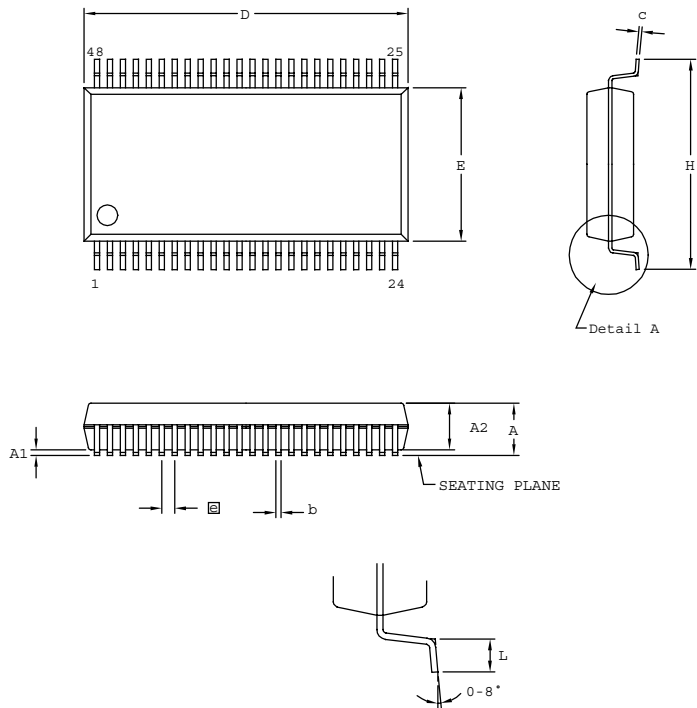
R247 P3M(F7H)

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|



* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)



| SYMBOL | MILLIMETER | | INCH | |
|--------|------------|-------|-----------|--------|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.79 | 0.095 | 0.110 |
| A1 | 0.23 | 0.38 | 0.009 | 0.015 |
| A2 | 2.18 | 2.39 | 0.086 | 0.094 |
| b | 0.20 | 0.34 | 0.008 | 0.0135 |
| c | 0.13 | 0.25 | 0.005 | 0.010 |
| D | 15.75 | 16.00 | 0.620 | 0.630 |
| E | 7.39 | 7.59 | 0.291 | 0.299 |
| ⓐ | 0.635 BSC | | 0.025 BSC | |
| H | 10.16 | 10.41 | 0.400 | 0.410 |
| L | 0.51 | 1.016 | 0.020 | 0.040 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 68. 48-Pin SSOP Package Design

► **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

- 28-pin DIP/SOIC/SSOP 6
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- 40-pin DIP 7
- 48-pin SSOP 8
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