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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323hah4808c00tr">https://www.e-xfl.com/product-detail/zilog/zgp323hah4808c00tr</a>



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## Development Features

Table 2 lists the features of ZiLOG®'s ZGP323H members.

**Table 2. Features**

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption—18mW (typical)
- T = Temperature  
S = Standard 0° to +70°C  
E = Extended -40° to +105°C  
A = Automotive -40° to +125°C
- Three standby modes:
  - STOP— (typical 1.8µA)
  - HALT— (typical 0.8mA)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors

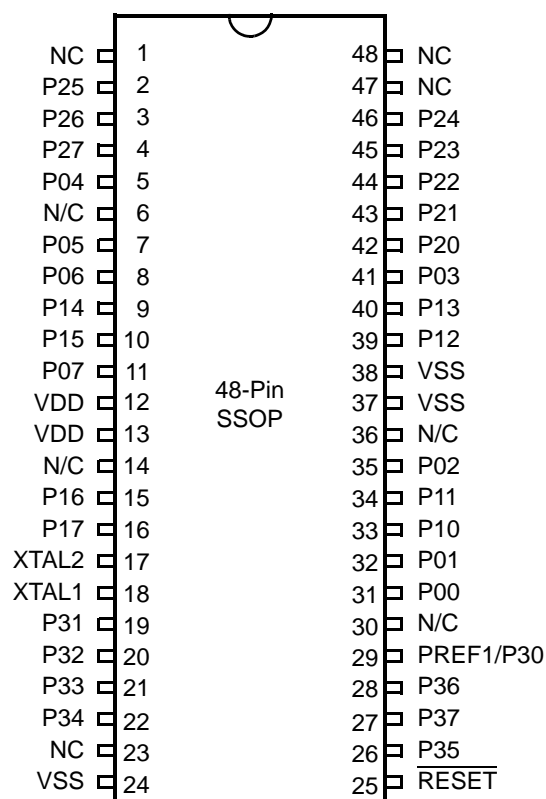


Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



**Table 11. GP323HA DC Characteristics (Continued)**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +125°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V <sub>HVD</sub>	V <sub>CC</sub> High Voltage Detection			2.7		V		

**Notes:**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V<sub>CC</sub> and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

**Table 12. EPROM/OTP Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	100			Cycles	1

**Notes:**

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(E_a/k) * (1/T_{use} - 1/T_{stress})]$$

Where:

E<sub>a</sub> is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10<sup>-5</sup> eV/°K)

°K = -273.16°C

T<sub>use</sub> = Use Temperature in °K

T<sub>stress</sub> = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>

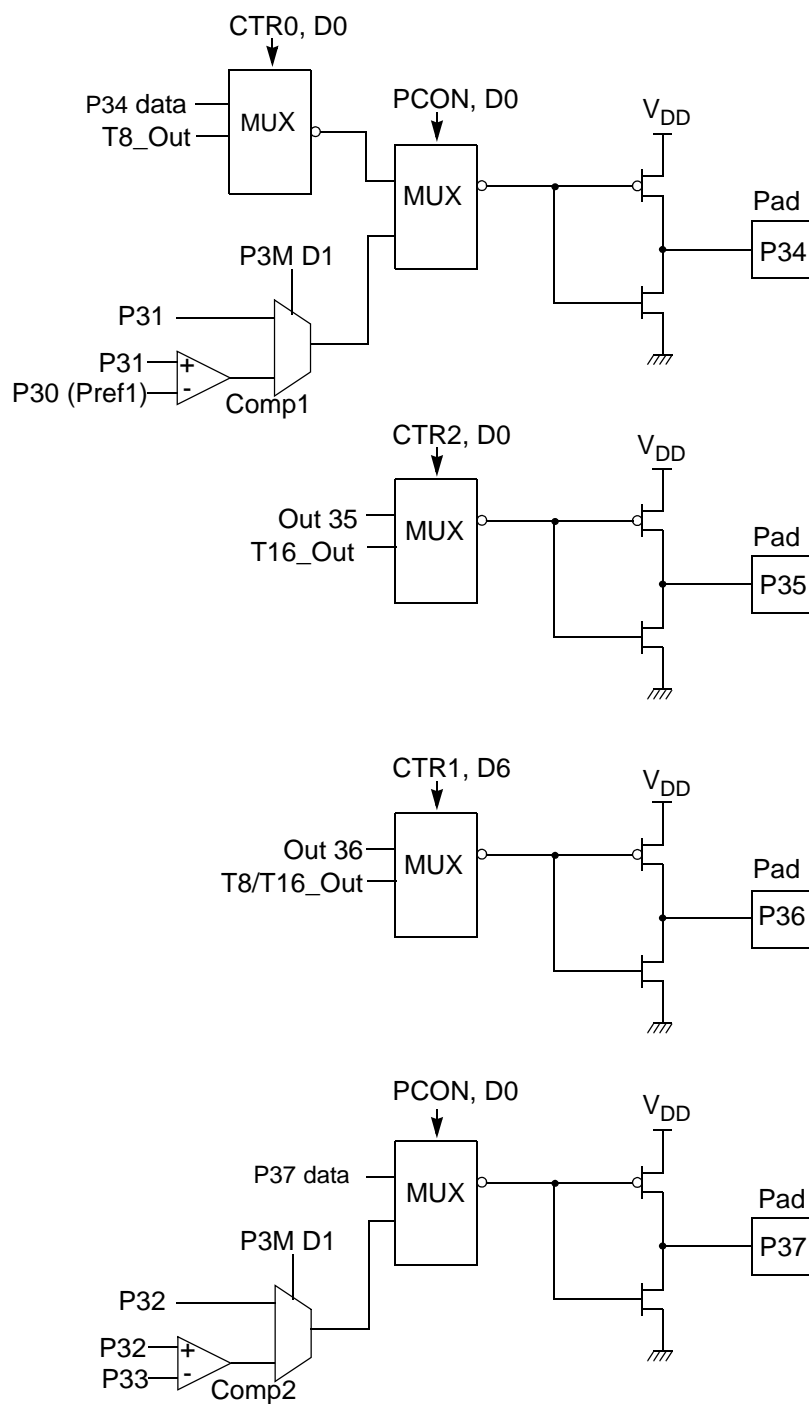


Figure 13. Port 3 Counter/Timer Output Configuration

### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

- **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP does not assert the RESET pin when under VBO.

- **Note:** The external Reset does not initiate an exit from STOP mode.

## Functional Description

This device incorporates special functions to enhance the Z8<sup>®</sup> functionality in consumer and battery-operated applications.

### Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

### RAM

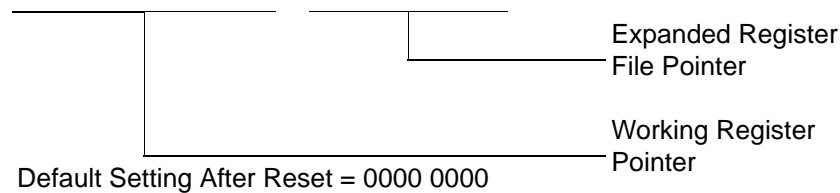
This device features 256B of RAM. See Figure 14.



The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



**Figure 16. Register Pointer**

**Example: Z8 GP: (See Figure 15 on page 28)**

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = Reserved



### Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

### Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description
T8_Level_HI	[7:0]	R/W Data

### Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position	Description
T8_Level_LO	[7:0]	R/W Data

### CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

**Table 15. CTR0(D)00H Counter/Timer8 Control Register**

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

Table 15. CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	-----1-	R/W	0**	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-----0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

**Note:**

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

**T8 Enable**

This field enables T8 when set (written) to 1.

**Single/Modulo-N**

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

**Timeout**

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

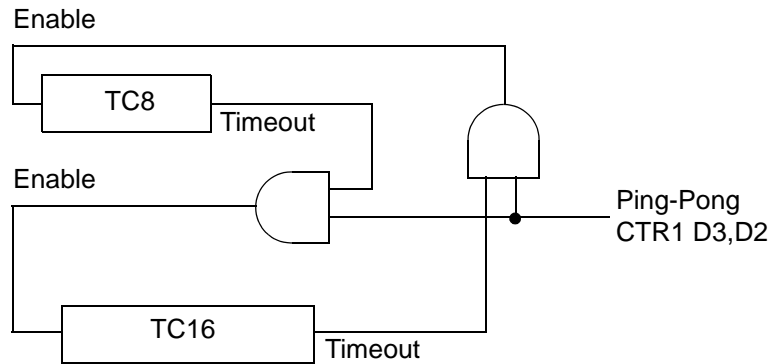


**Note:** Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

**T8 Clock**

This bit defines the frequency of the input signal to T8.

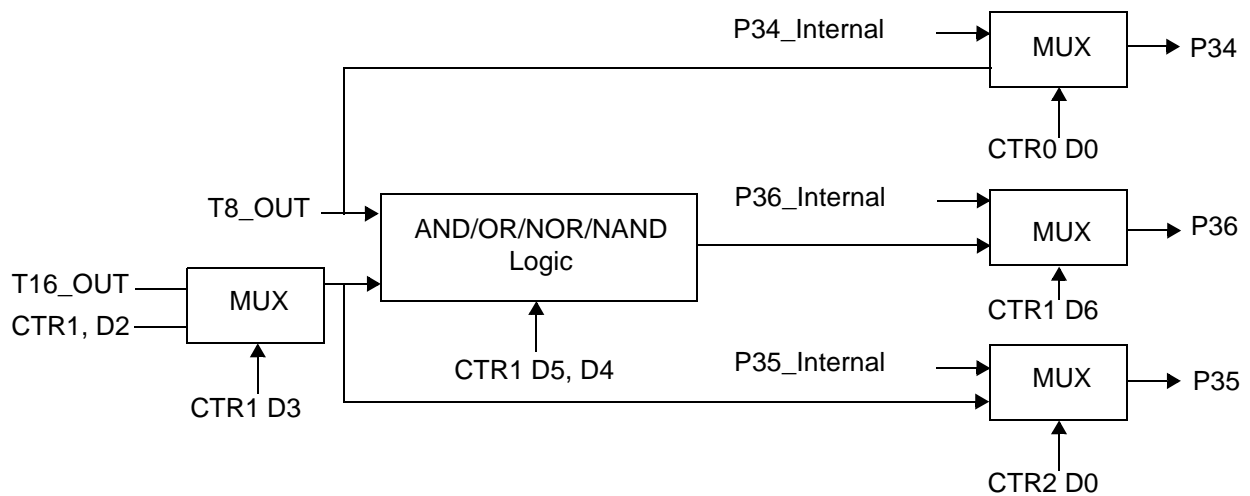




**Figure 28. Ping-Pong Mode Diagram**

### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

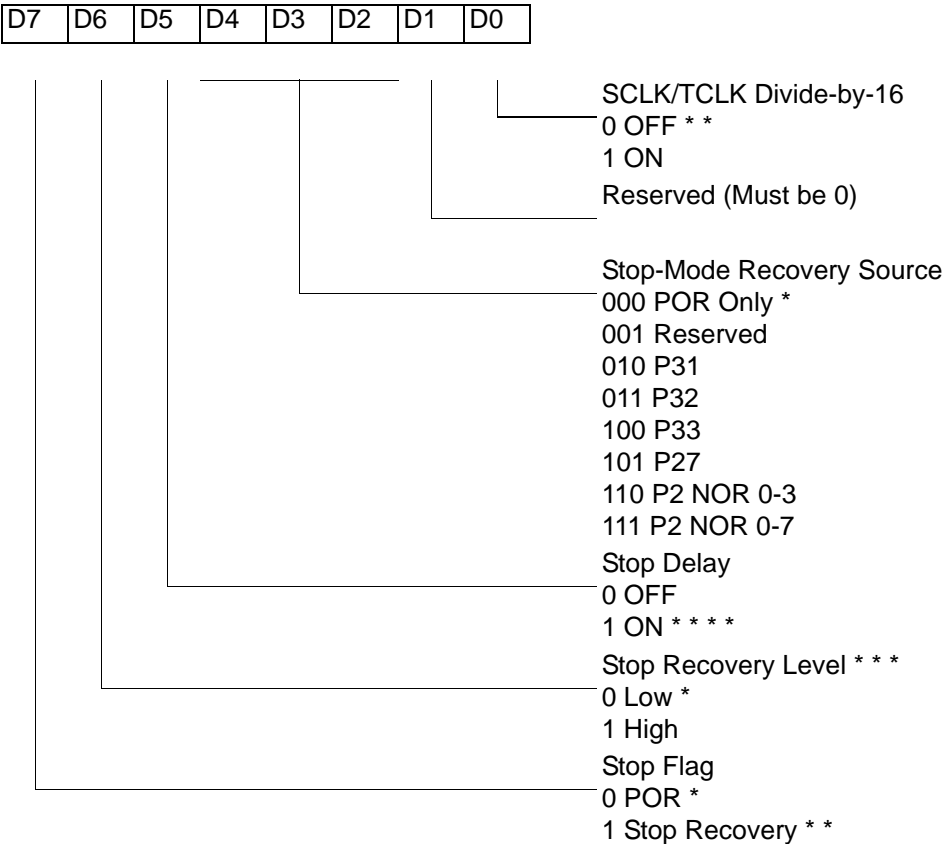


**Figure 29. Output Circuit**

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.



SMR(0F)0BH



\* Default after Power On Reset or Watch-Dog Reset  
\* \* Default setting after Reset and Stop Mode Recovery  
\* \* \* At the XOR gate input  
\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

### Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position	Description		
LVD	76543---	Reserved No Effect		
	----2--	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

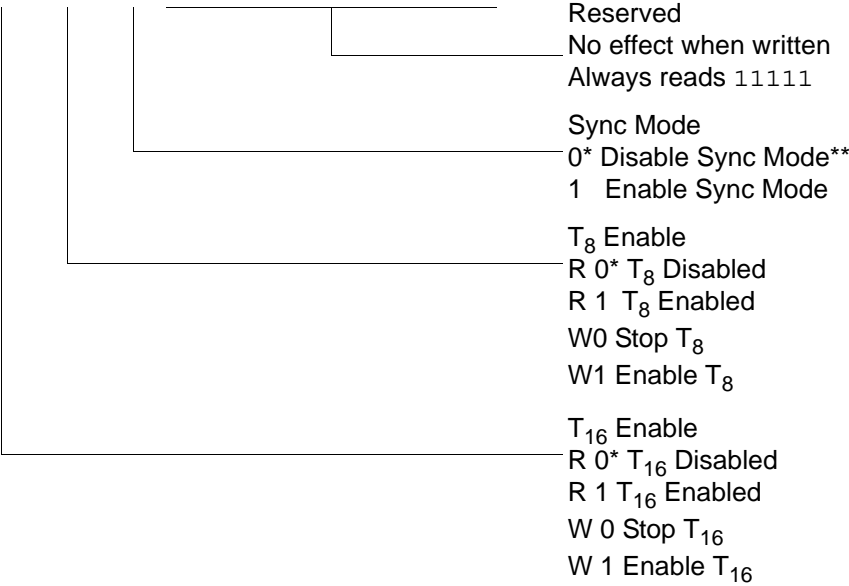
The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.



CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



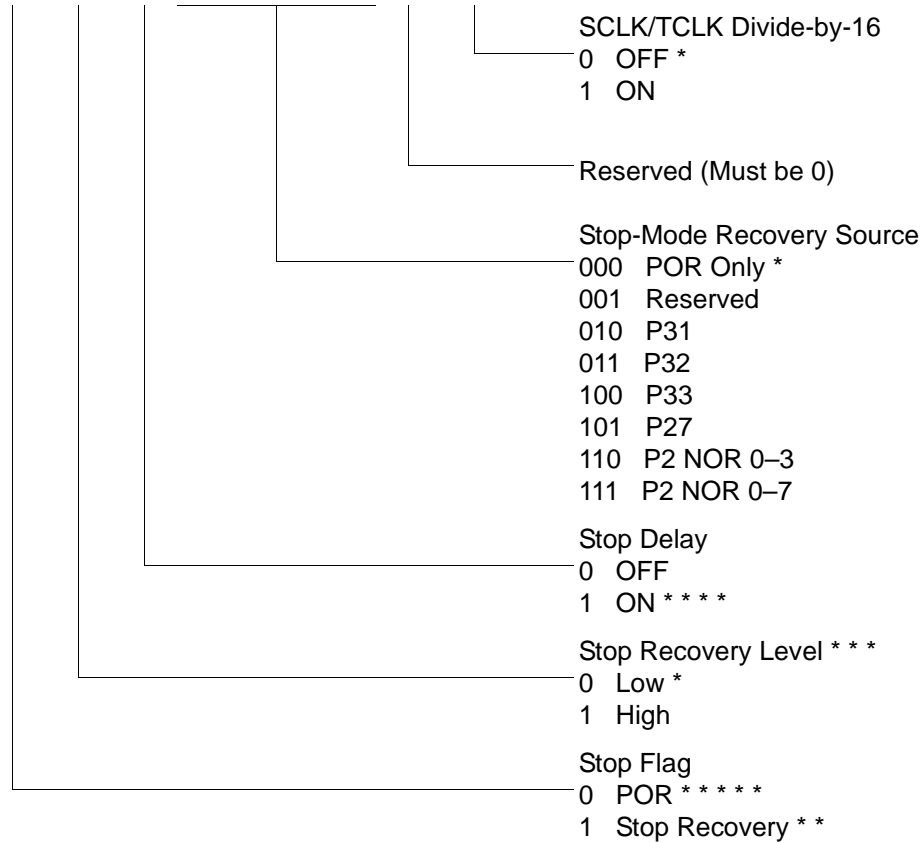
\* Default setting after reset.  
\*\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)



SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset

\* \* Set after Stop Mode Recovery

\* \* \* At the XOR gate input

\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

\* \* \* \* \* Default setting after Power On Reset. Not reset with a Stop Mode recovery.

**Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)**



R250 IRQ(FAH)

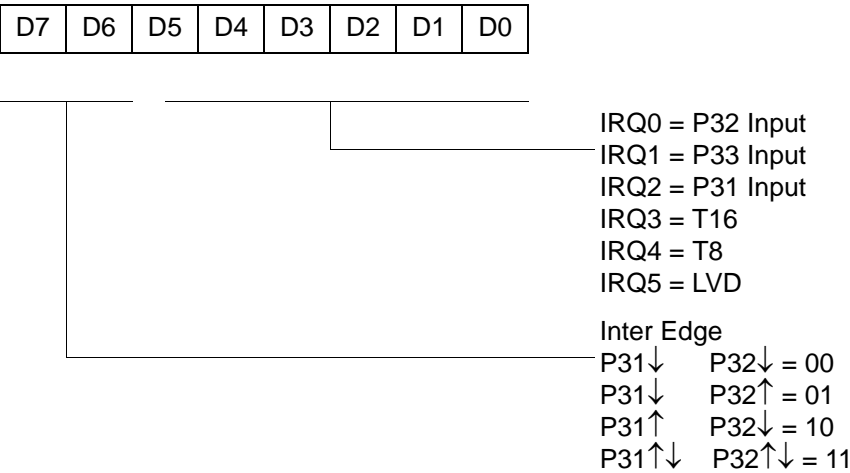


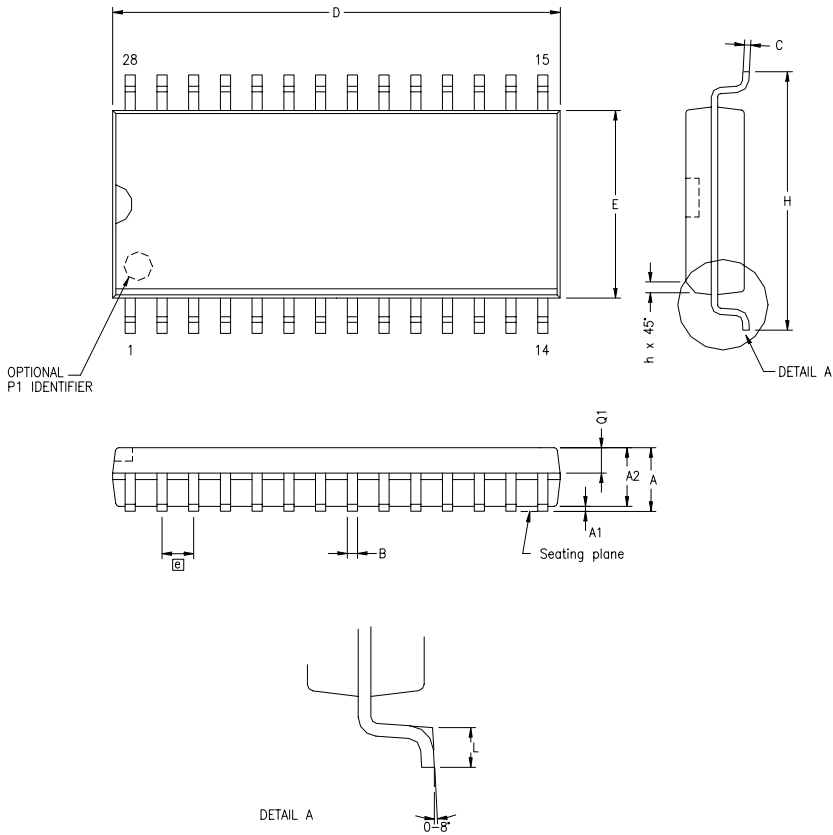
Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



\* Default setting after reset  
\*\* Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
@	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM  
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 62. 28-Pin SOIC Package Diagram



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

**Codes**

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

H = High Voltage

T = Temperature

S = Standard 0° to +70°C

E = Extended -40° to +105°C

A = Automotive -40° to +125°C

P = Package Type:

K = CDIP

P = PDIP

H = SSOP

S = SOIC

## = Number of Pins

CC = Memory Size

M = Molding Compound

C = Standard Plastic Packaging Molding Compound

G = Green Plastic Molding Compound

E = Standard Cer Dip flow

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