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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hap2008g

Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Section	Description	Page #
December 2004	02		Changed low power consumption, STOP and HALT mode current values, deleted mask option note, clarified temperature ranges in Tables 6 and 8 and 10. Added new Tables 9 and 10. Also added Characterization data to Table 11 and changed Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
			Removed Preliminary designation	All
March 2005	03		Minor change to Table 9 Electrical Characteristics. Added 20, 28 and 40-pin CDIP parts in the Ordering Section.	11,90

Table of Contents

    – Port 1: 0–3 pull-up transistors

    – Port 1: 4–7 pull-up transistors

    – Port 2: 0–7 pull-up transistors

    – EPROM Protection

    – WDT enabled at POR

General Description

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

▶ **Note:** All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

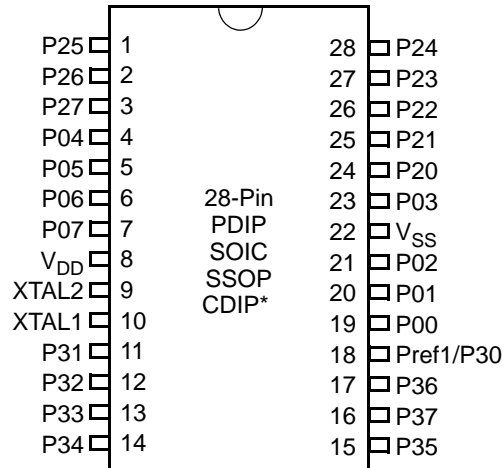Power connections use the conventional descriptions listed in Table 3.

Figure 4.   28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 5.   28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V_{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V_{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V_{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

Table 10. GP323HE DC Characteristics (Continued)

Symbol	Parameter	V_{CC}	T_A= -40°C to +105°C Min	Typ(7)	Max	Units	Conditions	Notes
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V_{CC}–0.8			V	I_{OH} = −7mA	
V_{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-5.5	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-5.5	−1		1	μA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V_{IN} = 0V; Pullups selected by mask option	
		3.6V	50.0		300.0	KΩ		
		5.0V	25.0		175.0	KΩ		
I_{OL}	Output Leakage	2.0-5.5	−1		1	μA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I_{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I_{CC2}	Standby Current (Stop Mode)	2.0V		1.6	12	μA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		3.6V		1.8	15	μA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		5.5V		1.9	18	μA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		2.0V		5	30	μA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6V		8	40	μA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		5.5V		15	60	μA	V_{IN} = 0 V, V_{CC} WDT is Running	3
I_{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	V_{CC} Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.
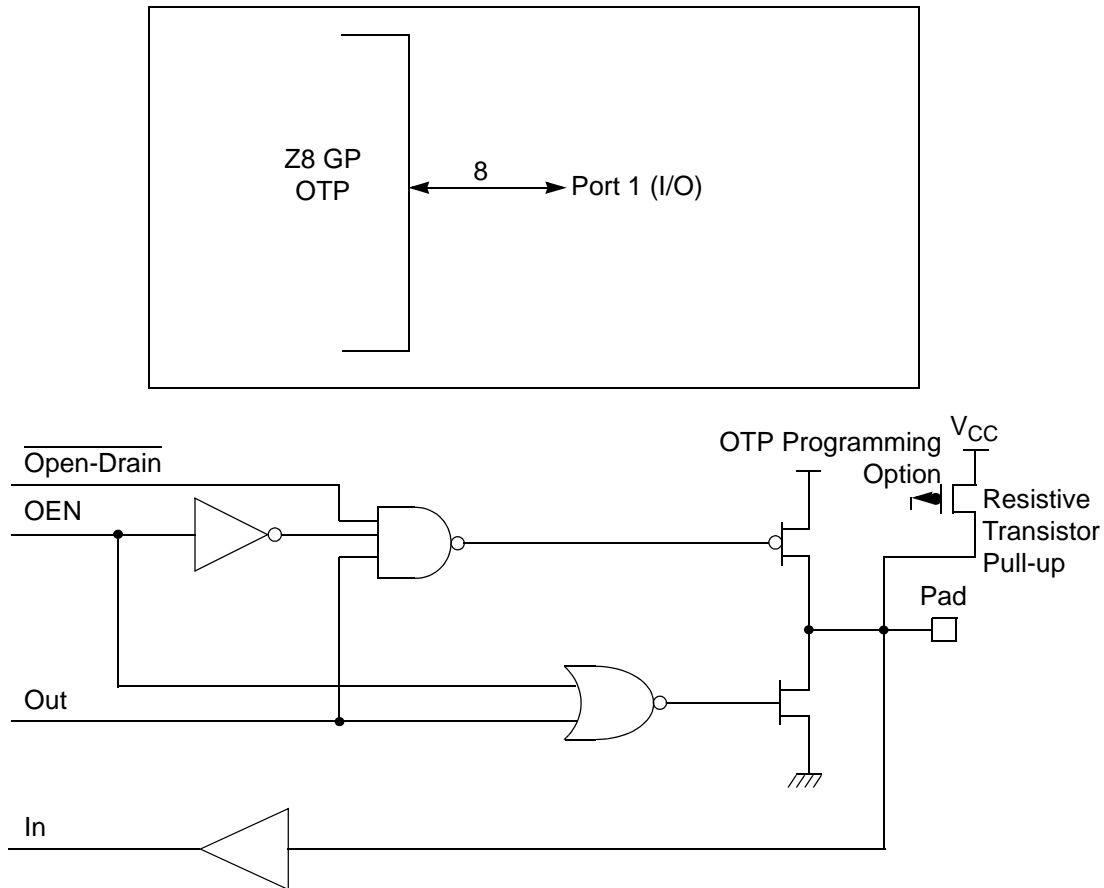
Figure 10. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      R0,#xx                  ; load CTR0
LD                      1, #xx                  ; load CTR1
LD                      R1, 2                   ; CTR2→CTR1

LD                      RP, #0Dh                ; Select ERF D
for access to bank D
                                                ; (working
register group 0)
LD                      RP, #7Dh                ; Select
expanded register bank D and working            ; register
group 7 of bank 0 for access.
LD                      71h, 2
; CTRL2→register 71h
LD                      R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 15) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

> **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.
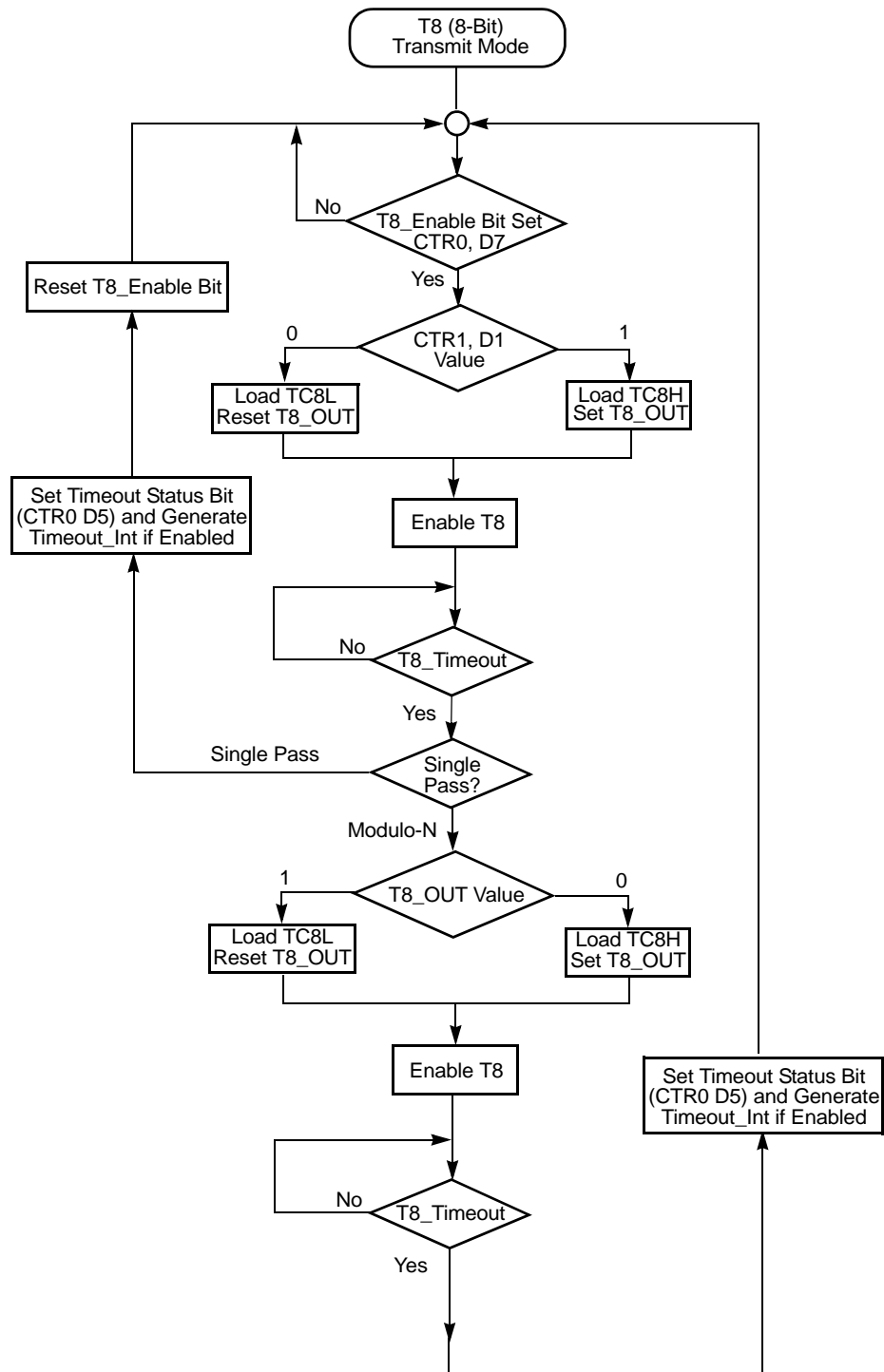
Figure 19. Transmit Mode Flowchart

T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.
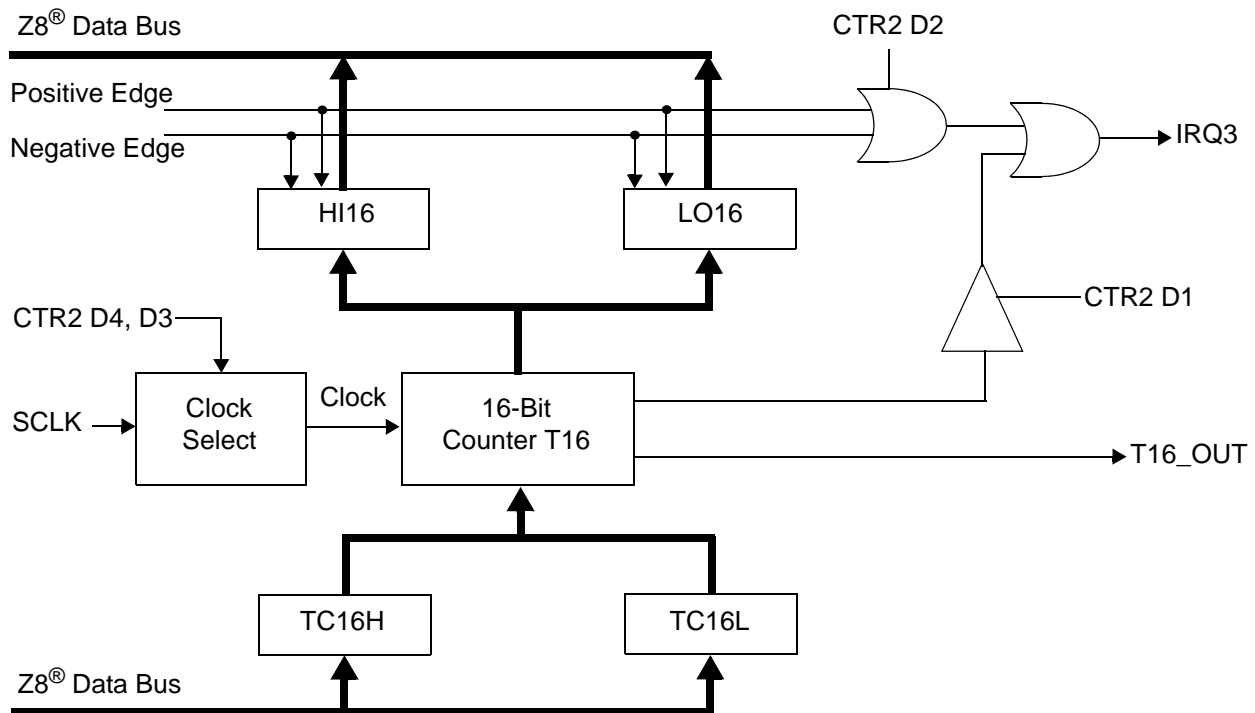

Figure 25. 16-Bit Counter/Timer Circuits

> **Note:** Global interrupts override this function as described in "Interrupts" on page 50.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.
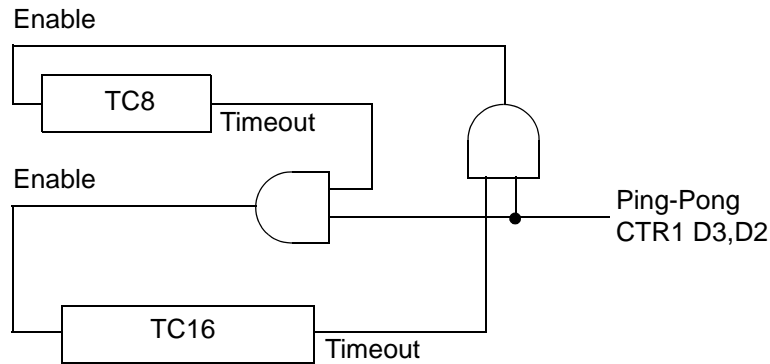
Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.
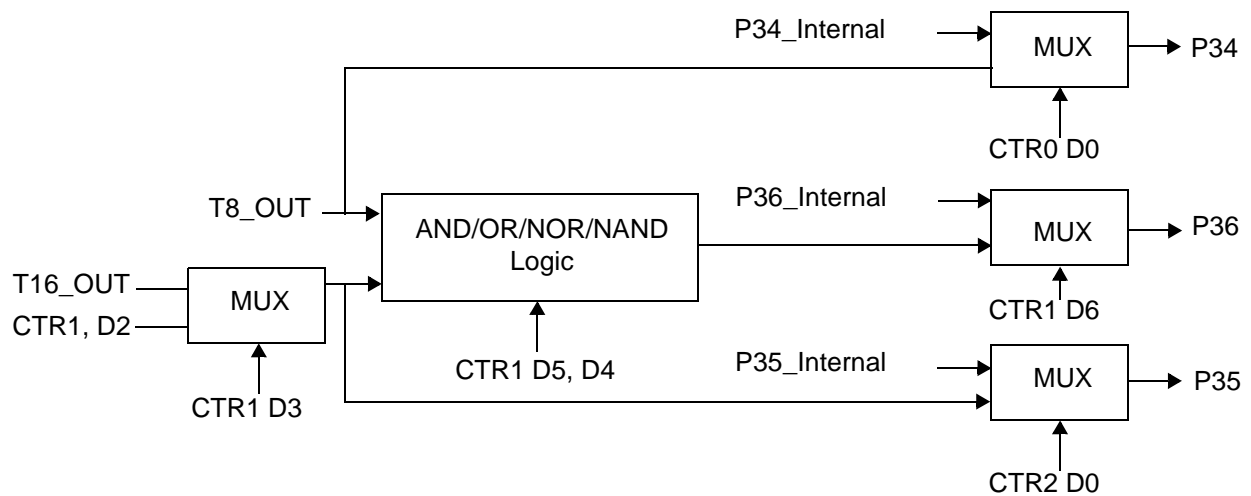
Figure 29. Output Circuit

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

Figure 30. Interrupt Block Diagram

Table 19. Interrupt Types, Sources, and Vectors

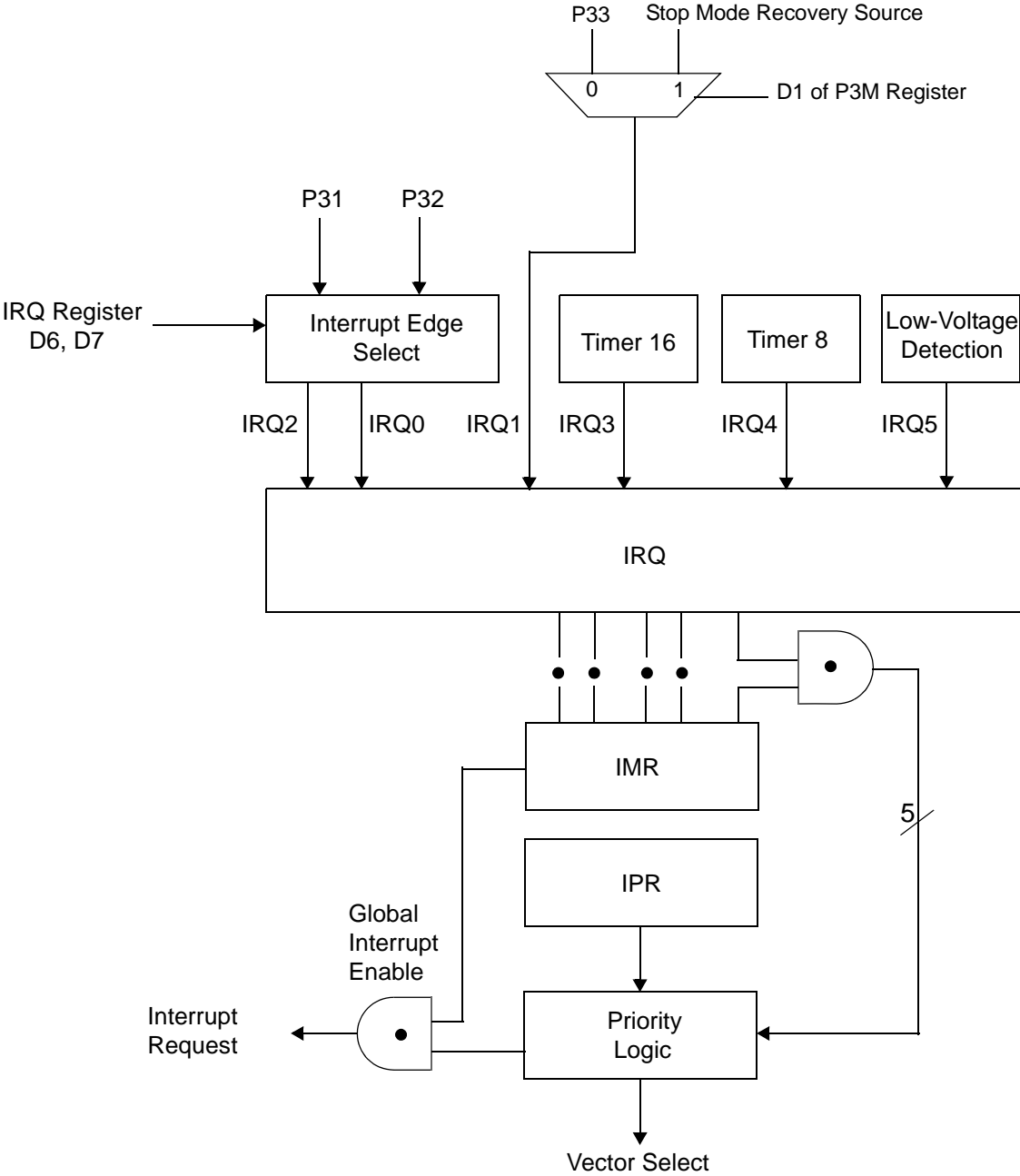| Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

Table 20. IRQ Register

IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Note: F = Falling Edge; R = Rising Edge

Table 22. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

> **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

> **Note:** This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).
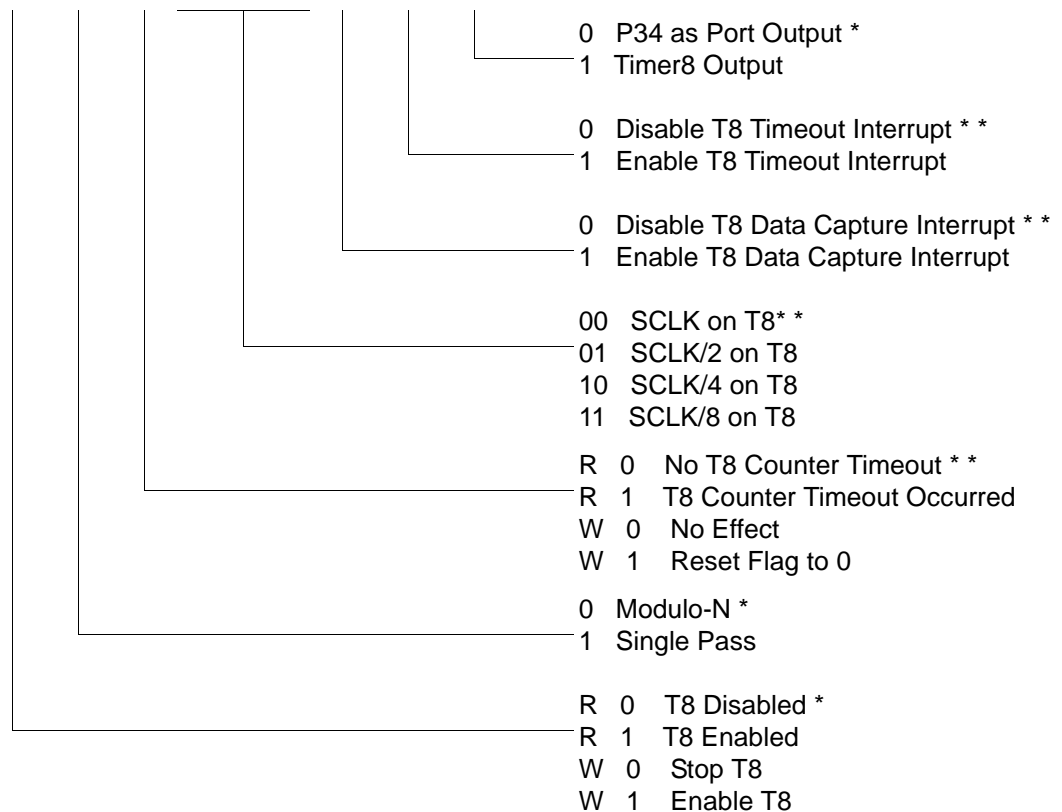
Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0

0 P34 as Port Output *
1 Timer8 Output

0 Disable T8 Timeout Interrupt * *
1 Enable T8 Timeout Interrupt

0 Disable T8 Data Capture Interrupt * *
1 Enable T8 Data Capture Interrupt

00 SCLK on T8* *
01 SCLK/2 on T8
10 SCLK/4 on T8
11 SCLK/8 on T8

R 0 No T8 Counter Timeout * *
R 1 T8 Counter Timeout Occurred
W 0 No Effect
W 1 Reset Flag to 0

0 Modulo-N *
1 Single Pass

R 0 T8 Disabled *
R 1 T8 Enabled
W 0 Stop T8
W 1 Enable T8

* Default setting after reset.
* * Default setting after Reset.. Not reset with a Stop-Mode recovery.

Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)

CTR1(0D)01H

D7	D6	D5	D4	D3	D2	D1	D0

Transmit Mode*
R/W   0   T16_OUT is 0 initially
          1   T16_OUT is 1 initially

Demodulation Mode
R   0   No Falling Edge Detection
R   1   Falling Edge Detection
W   0   No Effect
W   1   Reset Flag to 0

Transmit Mode*
R/W   0   T8_OUT is 0 initially*
          1   T8_OUT is 1 initially

Demodulation Mode
R   0   No Rising Edge Detection
R   1   Rising Edge Detection
W   0   No Effect
W   1   Reset Flag to 0

Transmit Mode*
0   0   Normal Operation*
0   1   Ping-Pong Mode
1   0   T16_OUT = 0
1   1   T16_OUT = 1

Demodulation Mode
0   0   No Filter
0   1   4 SCLK Cycle Filter
1   0   8 SCLK Cycle Filter
1   1   Reserved

Transmit Mode/T8/T16 Logic
0   0   AND**
0   1   OR
1   0   NOR
1   1   NAND

Demodulation Mode
0   0   Falling Edge Detection
0   1   Rising Edge Detection
1   0   Both Edge Detection
1   1   Reserved

Transmit Mode*
0   P36 as Port Output *
1   P36 as T8/T16_OUT

Demodulation Mode
0   P31 as Demodulator Input
1   P20 as Demodulator Input

Transmit/Demodulation Mode
0   Transmit Mode *
1   Demodulation Mode

* Default setting after Reset
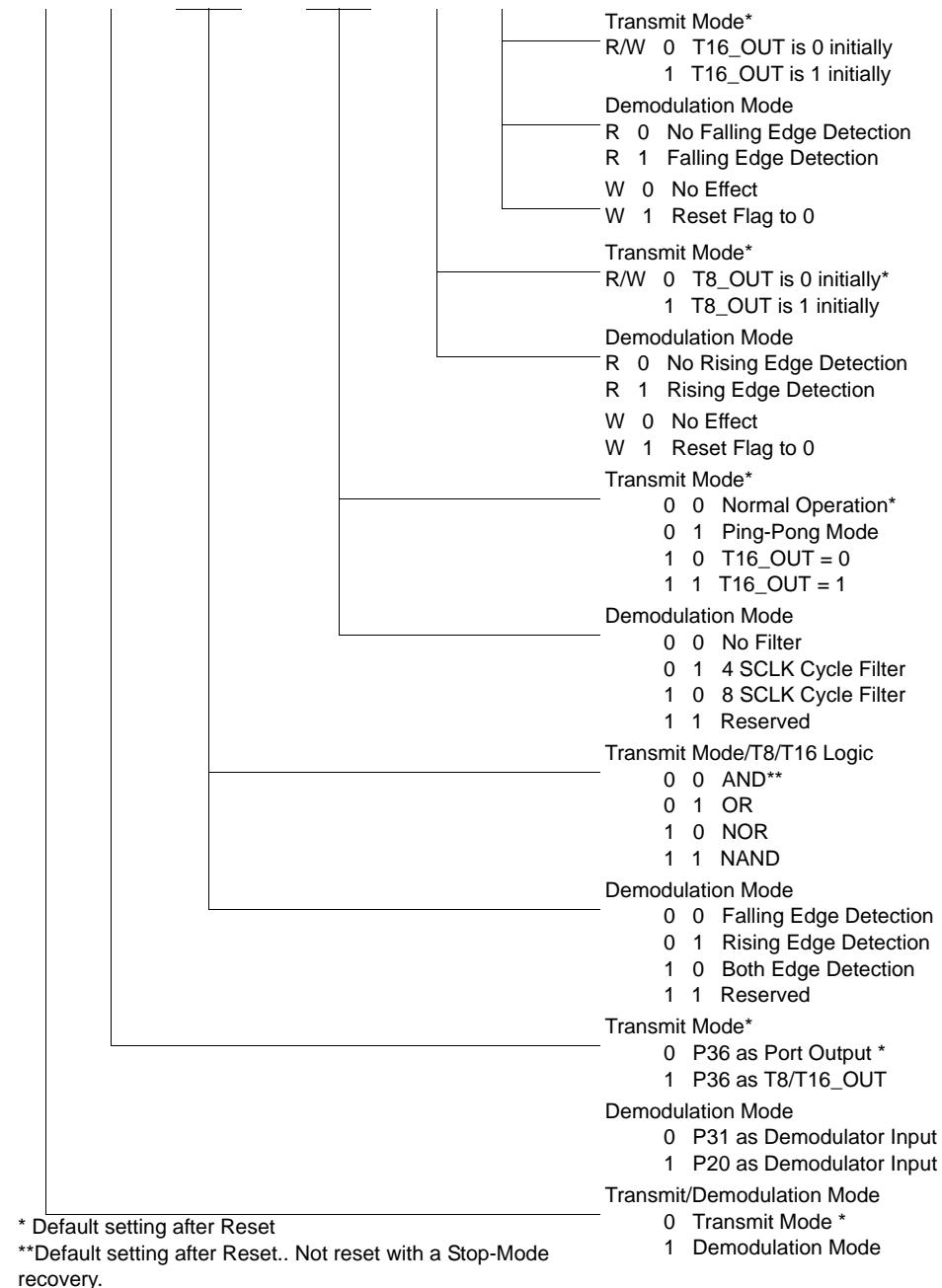**Default setting after Reset.. Not reset with a Stop-Mode recovery.

Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)
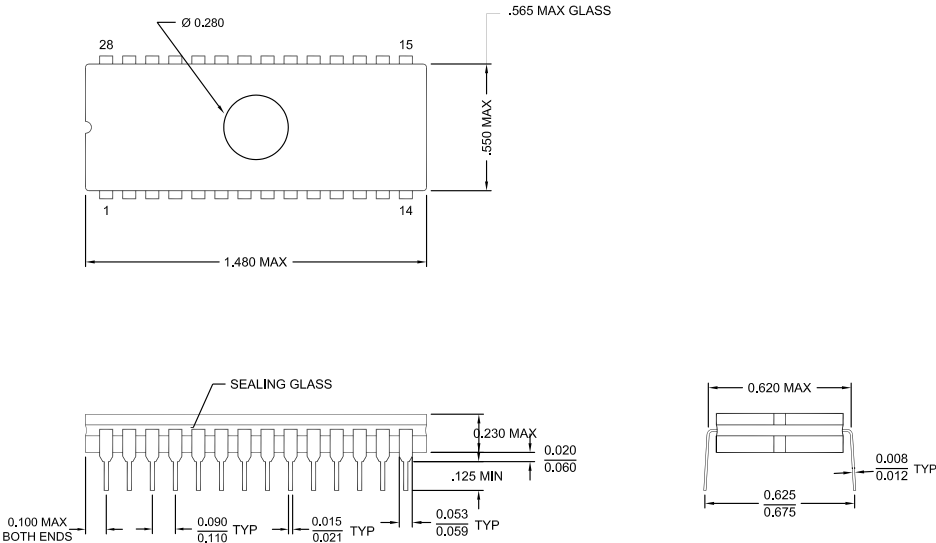
Figure 63. 28-Pin CDIP Package Diagram

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
⒠		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060
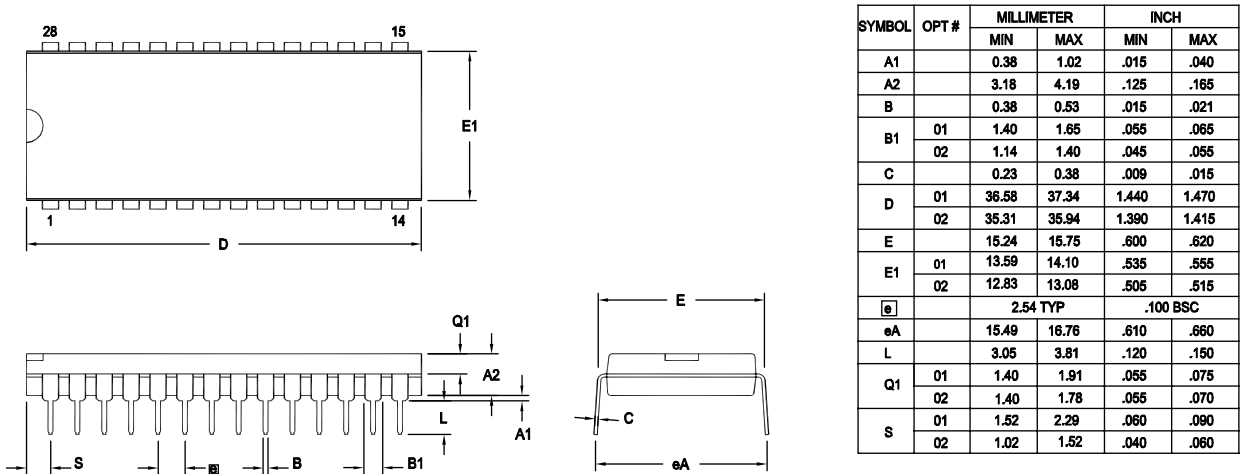
CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZiLOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 64. 28-Pin PDIP Package Diagram

Figure 67. 40-Pin CDIP Package Diagram

Figure 68. 48-Pin SSOP Package Design
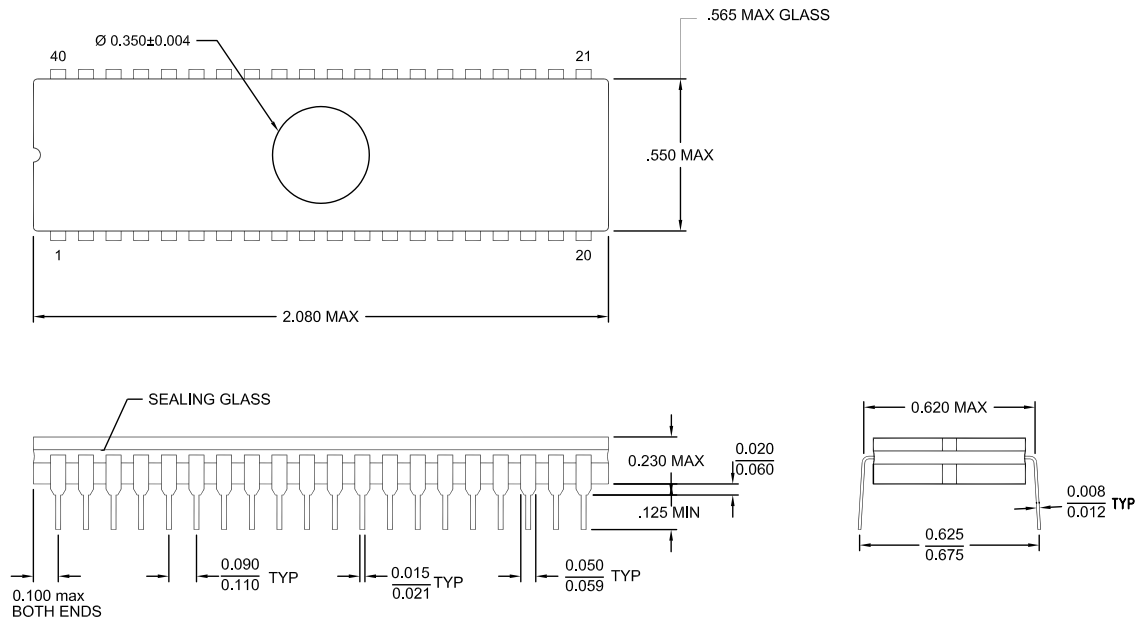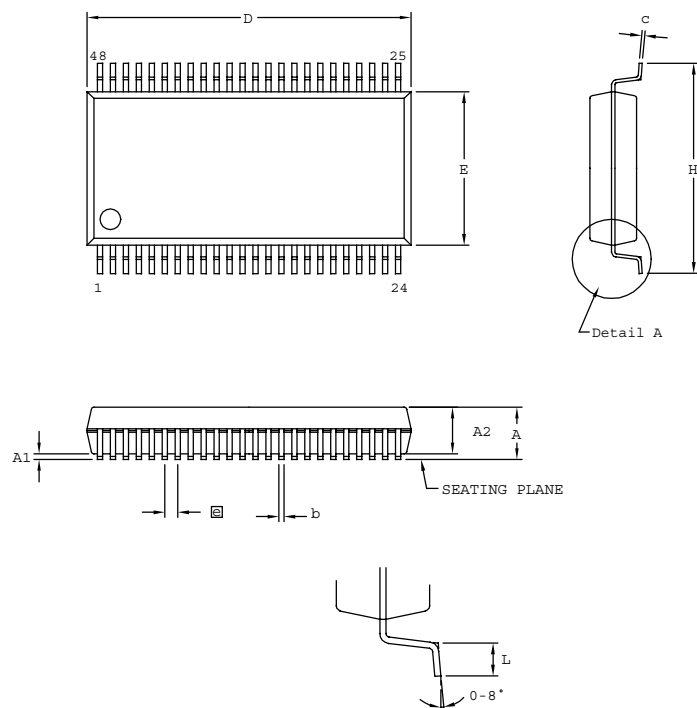
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
⊖	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

▶ **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP

16KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4816C	48-pin SSOP 16K OTP	ZGP323HAS2816C	28-pin SOIC 16K OTP
ZGP323HAP4016C	40-pin PDIP 16K OTP	ZGP323HAH2016C	20-pin SSOP 16K OTP
ZGP323HAH2816C	28-pin SSOP 16K OTP	ZGP323HAP2016C	20-pin PDIP 16K OTP
ZGP323HAP2816C	28-pin PDIP 16K OTP	ZGP323HAS2016C	20-pin SOIC 16K OTP
Replace C with G for Lead-Free Packaging			