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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	· .
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hap2016c

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# **Revision History**

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Docume	ent
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Date	Revision Level	Section	Description	Page #
December 2004	02	Changed low power of deleted mask option and 10. Added new T Table 11 and change	consumption, STOP and HALT mode current values, note, clarified temperature ranges in Tables 6 and 8 ables 9 and 10. Also added Characterization data to d Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
		Removed Preliminar	/ designation	All
March 2005	03	Minor change to Tabl pin CDIP parts in the	e 9 Electrical Characteristics. Added 20, 28 and 40- Ordering Section.	11,90

# ZGP323H Product Specification



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- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0-7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

# **General Description**

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG<sup>®</sup>'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8<sup>®</sup> offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

**Note:** All signals with an overline, "", are active Low. For example, B/W, in which WORD is active Low, and B/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.

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	1	-	<del>\</del>			
NC		1	$\bigcirc$	48	_	NC
DOF		2		17	_	NC
F 20		2		47		NC DO4
P20		3		40		P24
P2/		4		45		P23
P04		5		44		P22
N/C		6		43		P21
P05	q	7		42		P20
P06		8		41		P03
P14		9		40		P13
P15		10		39		P12
P07		11	40 Dia	38		VSS
VDD		12	48-PIN	37		VSS
VDD		13	330P	36		N/C
N/C		14		35		P02
P16	Е	15		34		P11
P17		16		33		P10
XTAL2		17		32		P01
XTAL1		18		31		P00
P31		19		30		N/C
P32		20		29		PREF1/P30
P33		21		28		P36
P34		22		27		P37
NC		22		26		P35
VSS	Д	20		20	_	RESET
100	-	24		ZD		NEOL I

Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



	T <sub>∆</sub> =0°C to +70°C									
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Мах	Units	Conditions	Notes		
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$			
Icc	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2		
00		3.6V		5	10	mA	at 8.0 MHz	1, 2		
		5.5V		10	15	mA	at 8.0 MHz	1, 2		
I <sub>CC1</sub>	Standby Current	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6		
	(HALT Mode)	3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6		
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6		
I <sub>CC2</sub>	Standby Current (Stop	2.0V		1.6	8	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3		
	Mode)	3.6V		1.8	10	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3		
		5.5V		1.9	12	μΑ	$V_{IN} = 0 V, V_{CC} WDT not Running$	3		
		2.0V		5	20	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3		
		3.6V		8	30	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3		
		5.5V		15	45	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3		
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4		
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage			1.9	2.0	V	8MHz maximum			
20	Protection						Ext. CLK Freq.			
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage			2.4		V				
	Detection									
V <sub>HVD</sub>	Vcc High Voltage			2.7		V				
	Detection									

#### Table 9. GP323HS DC Characteristics (Continued)

#### Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when  $V_{CC}$  falls below  $V_{BO}$  limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

- 6. Comparator and Timers are on. Interrupt disabled.
- 7. Typical values shown are at 25 degrees C.

## Table 10. GP323HE DC Characteristics

	T <sub>A</sub> = -40°C to +105°C									
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes		
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5		
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator			
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.4	V	Driven by External Clock Generator			
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V				
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> 0.3		0.2 V <sub>CC</sub>	V				
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	I <sub>OH</sub> = -0.5mA			



# **AC Characteristics**





Figure 8. AC Timing Diagram



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			T <sub>A</sub> =0°C to +70°C (S) −40°C to +105°C (E) −40°C to +125°C (A) 8.0MHz					Watch-Dog Timer Mode Register
No	Symbol	Parameter	V <sub>CC</sub>	Minimum	Maximum	Units	Notes	(D1, D0)
1	ТрС	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	TwC	Input Clock Width	2.0–5.5	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–5.5	3ТрС			1	
6	TpTin	Timer Input Period	2.0–5.5	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–5.5	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width	2.0–5.5	12		ns	3	
		Spec		5TpC			4	
11	Tost	Oscillator Start-Up Time	2.0–5.5		5TpC		4	
12	Twdt	Watch-Dog Timer	2.0–5.5	5		ms		0, 0
		Delay Time	2.0–5.5	10		ms		0, 1
			2.0-5.5	20		ms		1,0
			2.0-0.0	ðU		ms		1, 1
13	T <sub>POR</sub>	Power-On Reset	2.0–5.5	2.5	10	ms		

#### **Table 13. AC Characteristics**

Notes:

1. Timing Reference uses 0.9  $V_{CC}$  for a logic 1 and 0.1  $V_{CC}$  for a logic 0. 2. Interrupt request through Port 3 (P33–P31).

3. SMR – D5 = 1.

4. SMR - D5 = 0.



# **Pin Functions**

# XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

# XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

# Port 0 (P07-P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

**Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to its default state following an SMR.





Figure 13. Port 3 Counter/Timer Output Configuration





Expanded Reg. Bank 0/Group 15"         Register Pointer         [7] [5] [4] [3] [2] [10]         Working Register         Group Pointer         Bank Pointer         FF         FP         Bank Pointer         FF         FP         Bank Pointer         FF         FF         FF         FF         Bank Pointer         FF          FF		Res	et C	Cond	itior	۱		
Register Pointer       FF       SPL FE       U <thu< th=""> <thu< th="">       U       U</thu<></thu<>			Expanded Reg. Bank 0/Group 15	** D7 D6 D	5 D4	D3	D2[	D1 D0
Register Pointer       Image: Construction of the second of					1	ii		
Register Pointer       T       D								
Register Pointer         U       <			FD RP		0	0	0	
7       6       5       4       3       2       1       0		Register Pointer	FC FLAGS					
Working Register Group Pointer       Expanded Register Bank Pointer       FA       IRQ       0 <td< td=""><td>7</td><td>7 6 5 4 3 2 1 0</td><td>FB IMB</td><td></td><td></td><td></td><td></td><td></td></td<>	7	7 6 5 4 3 2 1 0	FB IMB					
Working Register       Expanded Register       F3       F3 <td></td> <td></td> <td>FA IBO</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td>			FA IBO		0	0	0	
Ordop Pollies       Dirth Antes         PB       PD1M       1       0 <t< td=""><td>Working Regist</td><td>ter Expanded Regist</td><td>er F9 IPR</td><td></td><td></td><td></td><td></td><td></td></t<>	Working Regist	ter Expanded Regist	er F9 IPR					
F7       P3M       0	Group Pointer	Dank i ontei	F8 P01M	1 1 0	0	1	1	1 1
F6       P2M       1			F7 P3M		0	0	0	0 0
F5       Reserved       I			F6 P2M	1 1 1	1	1	1	1 1
F4       Reserved         F3       Reserved         F3       Reserved         F4       Reserved         F5       Reserved         F6       F6         F6       F7         F7       F8         F8       F8         F7       F8         F8       F8         F9       F8 <td></td> <td></td> <td>F5 Reserved</td> <td></td> <td></td> <td><math>\frac{1}{1}</math></td> <td>ii l</td> <td></td>			F5 Reserved			$\frac{1}{1}$	ii l	
Fig       Reserved       U			F4 Reserved			11	<del>U</del>	
File       (Bank 0)**       File       (Bank 0)**       File       (Bank 0)**         File       Reserved       U			F3 Reserved		U U	U	U	
Findersterning (bank 0)**       Findersterning (bank 0)**			F2 Reserved		U U	U	Ŭ	
F0       Reserved       U	FF	Register File (Bank 0)	F1 Reserved		U U	Ŭ	U	υυ
Image: Second State Sta	Fo		F0 Reserved		U U	Ŭ	U	
Figure 1       Expanded Reg. Bank F/Group 0**         (F) 0F       WD 1MR         (F) 0F       WD 1MR         (F) 0F       Reserved         (F) 0F       Reserved         (F) 0R       Reserved						1-1	~	
Image: constraint of the second state stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the			Expanded Reg. Bank F/Group 0*	*				
(F) 0E Reserved       0			(F) 0F WDTMR	U U O	0	1	1	0 1
F) OD SMR2       0			(F) 0E Reserved			Π		
7F       F			* (F) 0D SMR2	0 0 0	0	0	0	0 0
7F       (F) 0B SMR       U 0 1 0 0 0 U 0         (F) 0B Reserved       (F) 0B Reserved       (F) 0B Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved </td <td>_</td> <td></td> <td>(F) 0C Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_		(F) 0C Reserved					
(F) 0A Reserved       (F) 09 Reserved         (F) 06 Reserved       (F) 06 Reserved         (F) 07 Reserved       (F) 06 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 09 Reserved       (F) 07 Reserved         (F) 00 Reserved       (F) 00 Reserved         (D) 00 C LVD       (D) 0 0 0 0 0 0 0 0	7F	· ↓	↑ (F) 0B SMR	U 0 1	0	0	0	U 0
(F) 09       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 07       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 01       Reserved         (F) 02       Reserved         (F) 01       Reserved         (F) 02       Reserved         (F) 01       Reserved         (F) 01       Reserved         (F) 01       Reserved         (F) 01       Reserved         (F) 02       Reserved         (F) 03       Reserved         (F) 04       Reserved         (F) 01       Reserved		<b>_</b>	(F) 0A Reserved			Π		
(F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 00 PCON       (F) 01 Reserved         (O) 01 P1       U         (O) 00 P0       U         U = Unknown       (D) 00 C T16L         * 18 not reset with a Stop-Mode Recovery         * 111 Bits 5,4,3,2 not reset with a Stop-Mode Recovery         * 111 Bits 5,4,3,2,2 not reset with a			(F) 09 Reserved					
0F       (F) 07 Reserved       (F) 06 Reserved         (F) 06 Reserved       (F) 05 Reserved         (F) 07 Reserved       (F) 04 Reserved         (F) 07 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 04 Reserved       (F) 04 Reserved			(F) 08 Reserved					
0F       (F) 06 Reserved       (F) 05 Reserved         (F) 04 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 01 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 03 P3 0       (F) 01 Reserved         (F) 00 PCON       (F) 01 Reserved         (F) 01 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 00 PCON       (F) 01 Reserved         (F) 01 P1       (F) 01 Reserved         (D) 02 P2       (F) 00 PCON         (F) 03 B Hil8       (F) 00 0 0 0 0 0 0 0         (D) 04 LO8       (F) 00 0 0 0 0 0         (F) 03 B LO16       (F) 00 0 0 0 0 0         (F) 04 C LD8       (F) 00 0 0 0 0 0         (D) 05 TC8H       (F) 00 0 0 0 0 0         (F) 03 C TR3       (F) 0 0 0 0 0 0         (F) 04 TC8L       (F) 0 0 0 0 0 0         (F) 04 C C R2<			(F) 07 Reserved					
0F       0F <td< td=""><td></td><td></td><td>(F) 06 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 06 Reserved					
0F       00 <td< td=""><td></td><td></td><td>(F) 05 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 05 Reserved					
00       Image: constraint of the set with a Stop-Mode Recovery         1 <td>0F</td> <td><u> </u>₩/</td> <td>(F) 04 Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	0F	<u> </u> ₩/	(F) 04 Reserved					
Expanded Reg. Bank 0/Group (0)       (F) 02 Reserved       1	00		(F) 03 Reserved					
Expanded Reg. Bank 0/Group (0)         (0) 03 P3       0         (0) 02 P2       U         (0) 01 P1       U         (0) 01 P1       U         (0) 00 P0       U         U = Unknown         * Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ↑ Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ↑ Is not reset with a Stop-Mode Recovery         ** Di 03 CTR3       0         ** (D) 04 TC8L       0         0       0         ** (D) 03 CTR3       0         ** (D) 04 TC8L       0         0       0         ** (D) 02 CTR2       0         ** (D) 04 TC8L       0         0       0         ** (D) 02 CTR2       0         ** (D) 04 TC8L       0         0       0         ** (D) 02 CTR2       0         ** (D) 01 CTR1       0         ** (D) 00 CTR0       0		$\backslash$	(F) 02 Reserved					
Expanded Reg. Bank 0/Group (0)         (0) 03 P3       0       U         (0) 02 P2       U         *       (0) 01 P1       U         (0) 00 P0       U         (0) 00 P0       U         U = Unknown         * Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ↑ Is not reset with a Stop-Mode Recovery         ** His 5 Is not reset with a Stop-Mode Recovery         ** (D) 04 TC8L       0       <			(F) 01 Reserved					
(0) 03 P3       0       U         (0) 02 P2       U         * (0) 01 P1       U         (0) 00 P0       U         * (0) 00 P0       U         U = Unknown         * Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ^* (D) 05 TC8H       0	Expa	anded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1	1	1	1	1 0
(0) 03 P3       0			Expanded Reg. Bank D/Group 0					
(b) 02 P2       U         *       (0) 01 P1       U         (0) 00 P0       U         U = Unknown       *         * All addresses are in hexadecimal       *         ↑ Bit 5 Is not reset with a Stop-Mode Recovery         **       (D) 04         **       (D) 05         **       (D) 06         **       (D) 07         **       (D) 08         **       (D) 08         **       (D) 07         **       (D) 08         **       (D) 07         **       (D) 06         **       (D) 06         **       (D) 07         **       (D) 06         **       (D) 07         **       (D) 08         **       (D) 08         **       (D) 04         **       (D) 05         **       (D) 04         **       (D) 03         **       (D) 02         **       (D) 01         **       (D) 01         **       (D) 01         **       (D) 01         **       (D) 02         **       (D) 01       (D) 0	(0) 03 P3	U U		UUI	υ	U	U	υn
*       (0) 01 P1       U         (0) 01 P1       U         (0) 00 P0       U         *       (D) 00 A LO8       0<	(0) 02 P2	U	* (D) 0B HI8	0 0 0	0	0	0	0 0
(b) 01 1 1       0	* (0) 01 P1	U	* (D) 0A   08	0 0 0	0	0	0	0 0
(0) 00 P0       U         U = Unknown       (D) 08 LO16       0	(0) 011 1	<u> </u>	* (D) 09 HI16	0 0 0	0	0	0	0 0
U = Unknown       *       (D) 07 TC16H       0 <td>(0) 00 P0</td> <td>U</td> <td>* (D) 08 LO16</td> <td>0 0 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td>	(0) 00 P0	U	* (D) 08 LO16	0 0 0	0	0	0	0 0
* Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ^* All addresses are in hexadecimal         ^* Is not reset with a Stop-Mode Recovery, except Bit 0         ^* Bit 5 Is not reset with a Stop-Mode Recovery         ^* Bit 5 Is not reset with a Stop-Mode Recovery         ^* Bit 5 Js not reset with a Stop-Mode Recovery         ^* Bit 5 Js not reset with a Stop-Mode Recovery         ^* Bit 5 Js not reset with a Stop-Mode Recovery         ^* Diss 5,4,3,2 not reset with a Stop-Mode Recovery         ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery         ^* CD 00 CTR1         0       0         ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery         ^* CD 00 CTR0         ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery			* (D) 07 TC16H	0 0 0	0	0	0	0 0
*** All addresses are in hexadecimal       *       (D) 05 TC8H       0 <t< td=""><td>* Is not reset with a Ston-Mor</td><td>de Recoverv</td><td>* (D) 06 TC16L</td><td>0 0 0</td><td>0</td><td>0</td><td>0</td><td>0 0</td></t<>	* Is not reset with a Ston-Mor	de Recoverv	* (D) 06 TC16L	0 0 0	0	0	0	0 0
<sup>+</sup> Is not reset with a Stop-Mode Recovery, except Bit 0 <sup>+</sup> 1bit 5 Is not reset with a Stop-Mode Recovery <sup>+</sup> (D) 04 TC8L <sup>-</sup> 0 0 0 0 0 0 0 0 0 0 0 <sup>+</sup> (D) 03 CTR3 <sup>-</sup> 0 0 0 0 1 1 1 1 1 <sup>+</sup> 1 <sup>+</sup> (D) 02 CTR2 <sup>-</sup> 0 0 0 0 0 0 0 0 0 <sup>-</sup> 1 1 1 1 <sup>+</sup>	** All addresses are in beyade	ecimal	* (D) 05 TC8H	0 0 0	0	0	0	0 0
	↑ Is not reset with a Stop-Mo	de Recovery, except Bit 0	* (D) 04 TC8L	0 0 0	0	0	0	0 0
<sup>↑</sup> ↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑↑↑ <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑ <sup>↑</sup> ↑ <sup>↑</sup>	↑↑ Bit 5 Is not reset with a Sto	p-Mode Recovery	1↑ (D) 03 CTR3	0 0 0	1	1	1	1 1
<sup>↑↑↑↑</sup> Bits 5 and 4 not reset with a Stop-Mode Recovery <sup>↑↑↑↑↑</sup> (D) 01 CTR1         (D) 01 CTR1         (D) 0 0 0 0 0 0 0 0         (D) 01 CTR1         (D) 00 CTR0         (D)	↑↑↑ Bits 5,4,3.2 not reset with	a Stop-Mode Recoverv	↑↑↑ (D) 02 CTR2	0 0 0	0	0	0	0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery ↑↑↑↑↑↓ (D) 00 CTR0 0 0 0 0 0 0 0 0 0 0	↑↑↑↑ Bits 5 and 4 not reset with	a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0	0	0	0	0 0
	↑↑↑↑↑ Bits 5,4,3,2,1 not reset wit	th a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	0 0 0	0	0	0	0 0

# Figure 15. Expanded Register File Architecture



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#### Table 15.CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	0	R/W	0* 1	P34 as Port Output T8 Output on P34

#### Note:

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

## **T8 Enable**

This field enables T8 when set (written) to 1.

## Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

#### Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

#### **T8 Clock**

This bit defines the frequency of the input signal to T8.



Field	Bit Position		Value	Description
Transmit_Submode/	32	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

#### Table 16.CTR1(0D)01H T8 and T16 Common Functions (Continued)

#### Note:

\*Default at Power-On Reset

\*Default at Power-On Reset. Not reset with Stop Mode recovery.

#### Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

#### P36\_Out/Demodulator\_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.







Figure 19. Transmit Mode Flowchart



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When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8\_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8\_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



**Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



## Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved (Must be 0) Reserved (Must be 0) Stop-Mode Recovery Source 2 000 POR Only * 001 NAND P20, P21, P22, P23 010 NAND P20, P21, P22, P23, P24, P25, P26, P27 011 NOR P31, P32, P33 100 NAND P31, P32, P33 101 NOR P31, P32, P33, P00, P07 110 NAND P31, P32, P33, P00, P07
								111 NAND P31, P32, P33, P20, P21, P22
								Reserved (Must be 0)
								Recovery Level * * 0 Low * 1 High
								Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset

\* \* At the XOR gate input

## Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.



**Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.



#### Table 23. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

## WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



\* CLR1 and CLR2 enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-

#### Figure 38. Resets and WDT



## PCON(0F)00H



\* Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)



## R250 IRQ(FAH)





#### Figure 52. Interrupt Request Register (FAH: Read/Write)

#### R251 IMR(FBH)



\* Default setting after reset

\* \* Only by using EI, DI instruction; DI is required before changing the IMR register

#### Figure 53. Interrupt Mask Register (FBH: Read/Write)



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## Codes

ZG = ZiLOG General Purpose Family

P = OTP

- 323 = Family Designation
- H = High Voltage
- T = Temparature
  - S = Standard 0° to +70°C
  - $E = Extended 40^{\circ} to + 105^{\circ}C$
  - A = Automotive  $-40^{\circ}$  to  $+125^{\circ}C$
- P = Package Type:
  - K = CDIP
  - P = PDIP
  - H = SSOP
  - S = SOIC

## = Number of Pins

- CC = Memory Size
- M = Molding Compound
- C = Standard Plastic Packaging Molding Compound
- G = Green Plastic Molding Compound
- E = Standard Cer Dip flow

# ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



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X XTAL1 5 XTAL1 pin function 18 XTAL2 5 XTAL2 pin function 18