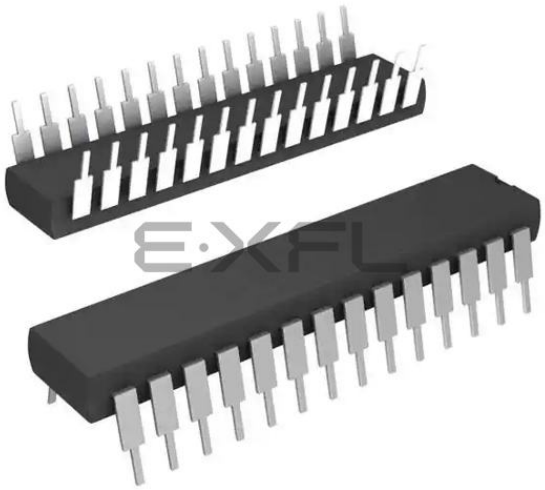

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hap2816g

List of Figures

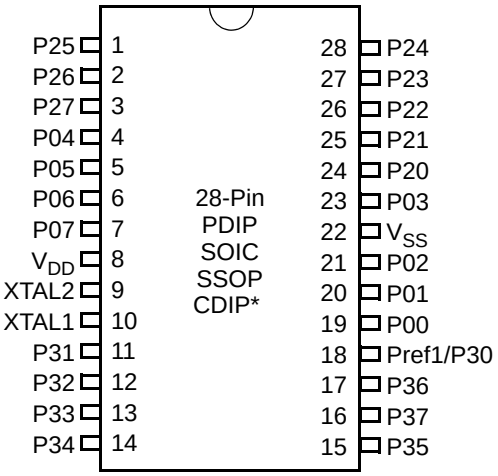


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V_{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V_{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V_{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

Table 6. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	$\overline{\text{RESET}}$
15	18	XTAL1
14	17	XTAL2
11	12, 13	V_{DD}
31	24, 37, 38	V_{SS}
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC

Table 11. GP323HA DC Characteristics

			T_A= -40°C to +125°C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ(7)**	**Max**	**Units**	**Conditions**	**Notes**
V_{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-5.5	0.8 V_{CC}		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-5.5	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-5.5	V_{CC}–0.4			V	I_{OH} = –0.5mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V_{CC}–0.8			V	I_{OH} = –7mA	
V_{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-5.5	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V_{IN} = 0V; Pullups selected by mask option	
		3.6V	50		300	KΩ		
		5.0V	25		175	KΩ		
I_{OL}	Output Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I_{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I_{CC2}	Standby Current (Stop Mode)	2.0V		1.6	15	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		3.6V		1.8	20	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		5.5V		1.9	25	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		2.0V		5	30	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6V		8	40	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		5.5V		15	60	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
I_{LV}	Standby Current (Low Voltage)			1.2	6	µA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	V_{CC} Low Voltage Detection			2.4		V		

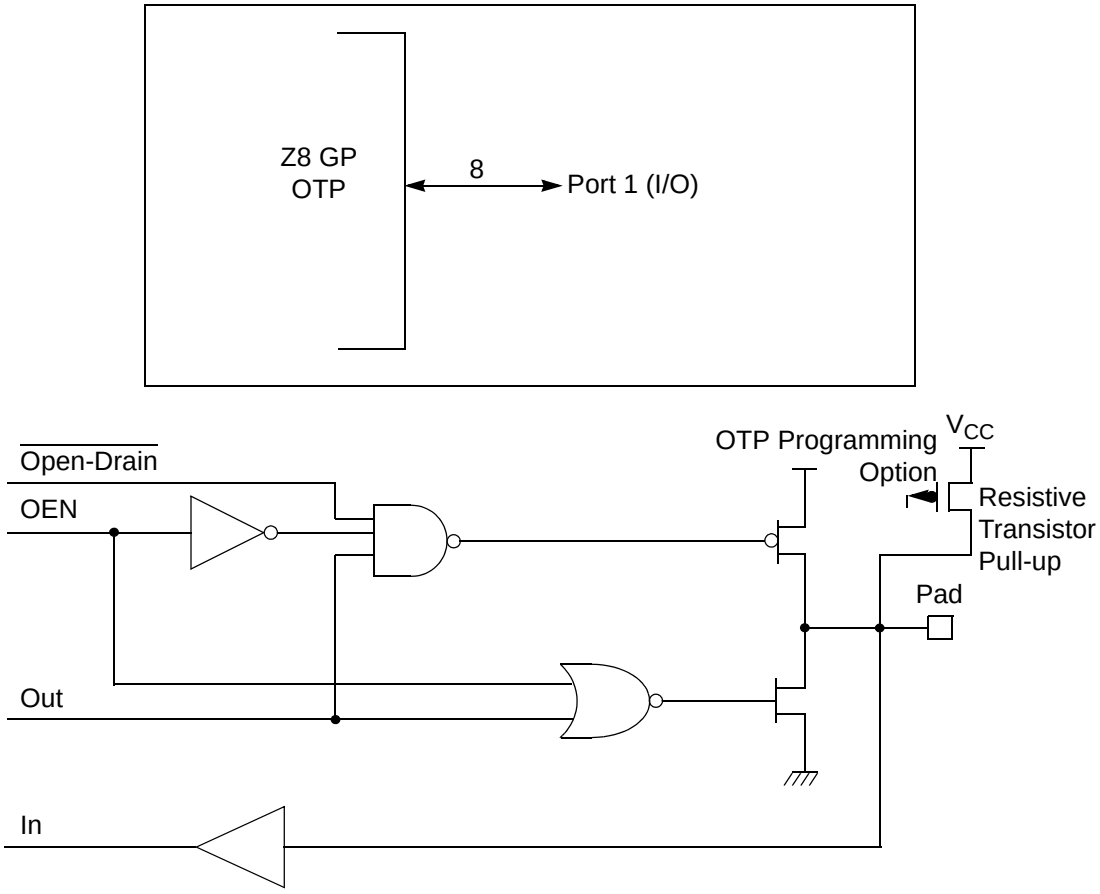


Figure 10. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.

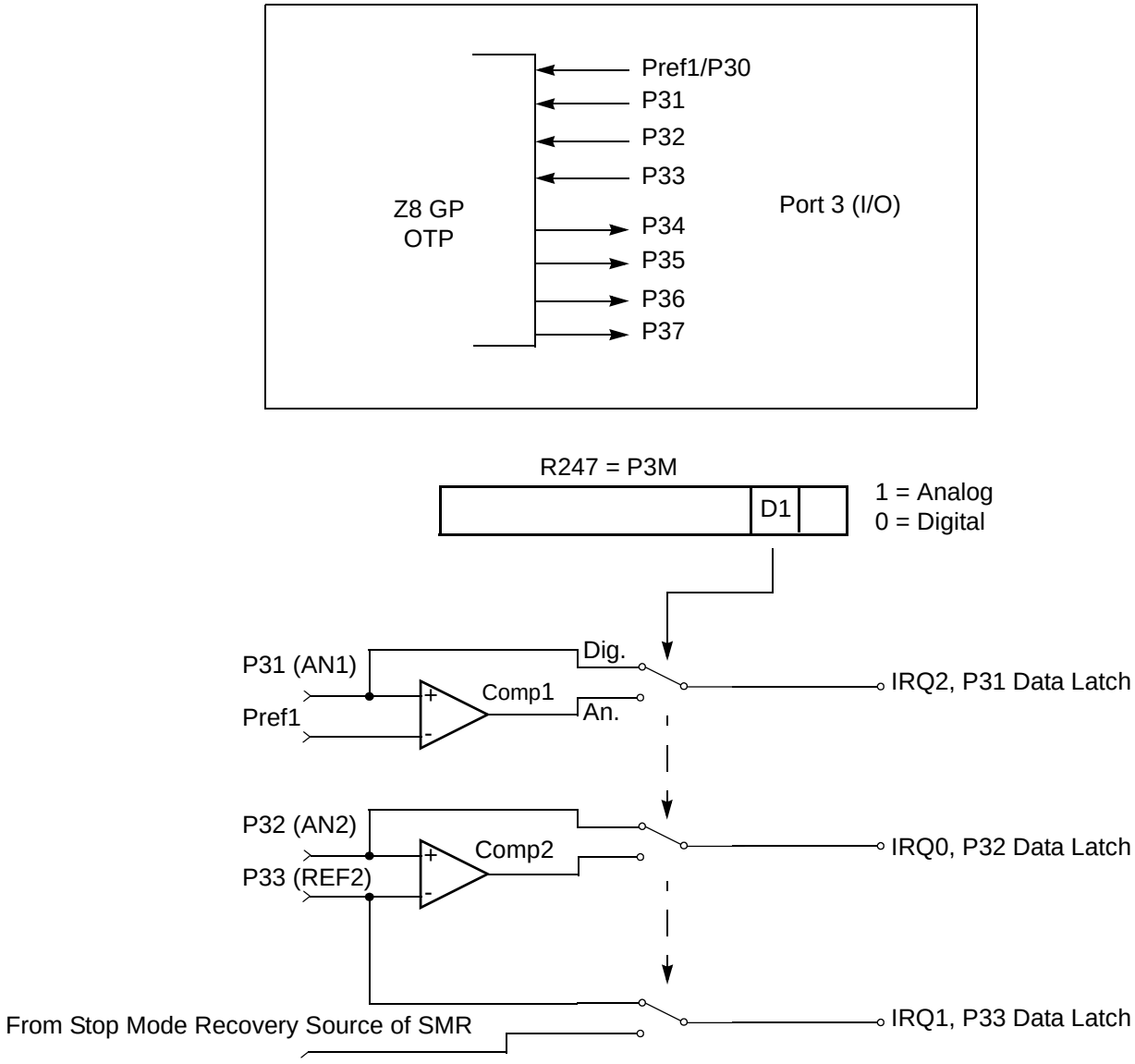


Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—

CTR1(0D)01H" on page 35). Other edge detect and IRQ modes are described in Table 14.

Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Table 14. Port 3 Pin Function Summary

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

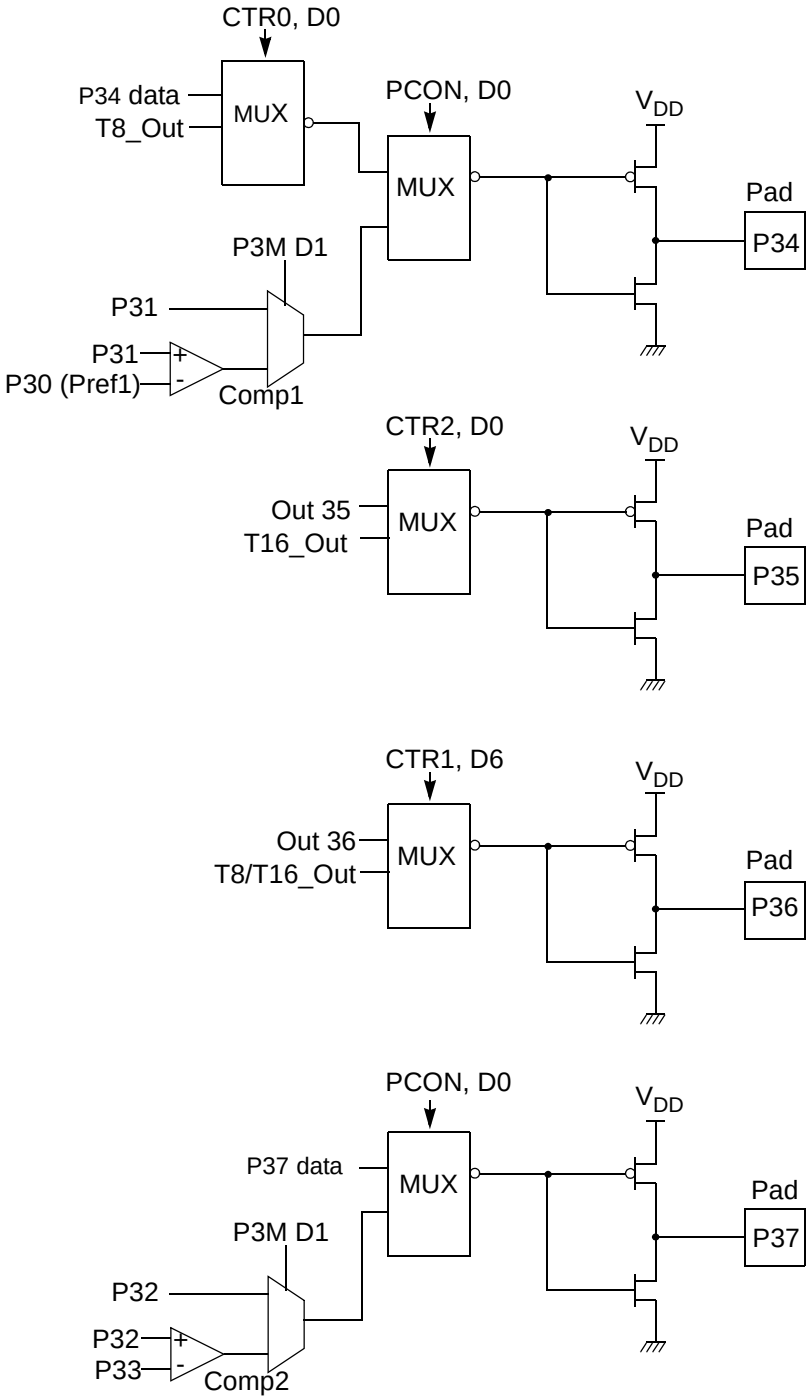


Figure 13. Port 3 Counter/Timer Output Configuration

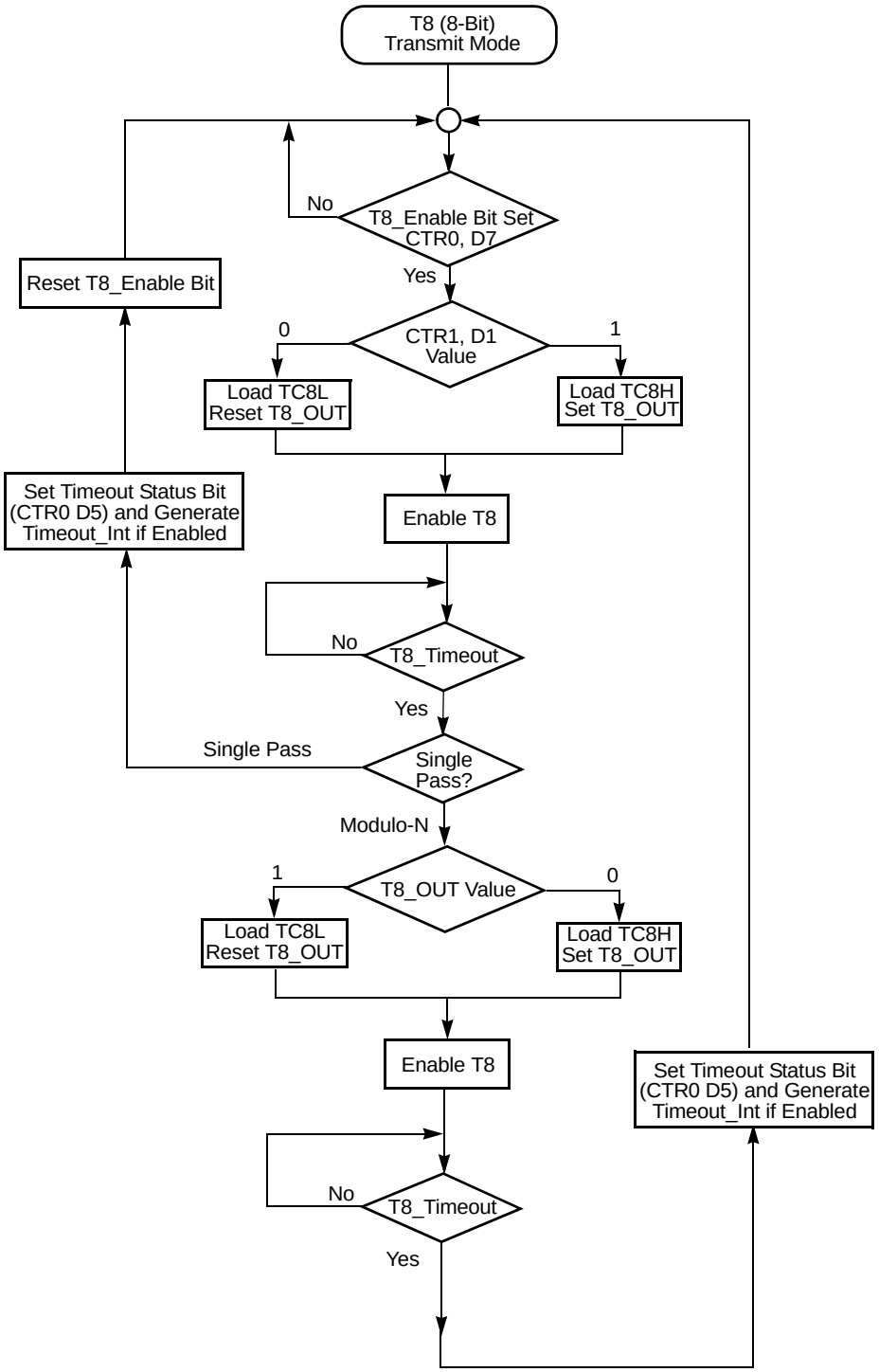


Figure 19. Transmit Mode Flowchart

Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.

Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.

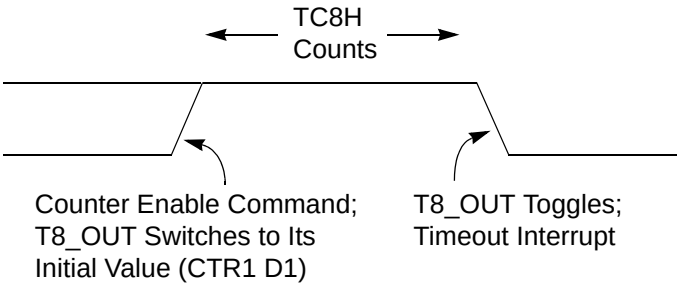


Figure 21. T8_OUT in Single-Pass Mode

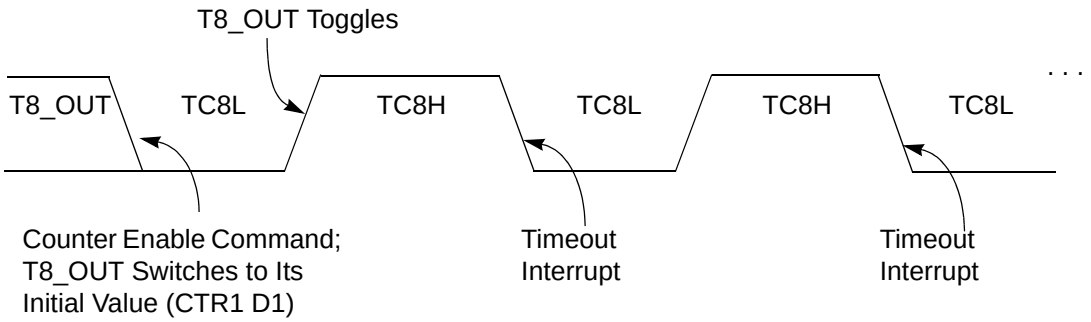


Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFEH. Transition from 0 to FFFFH is not a timeout condition.

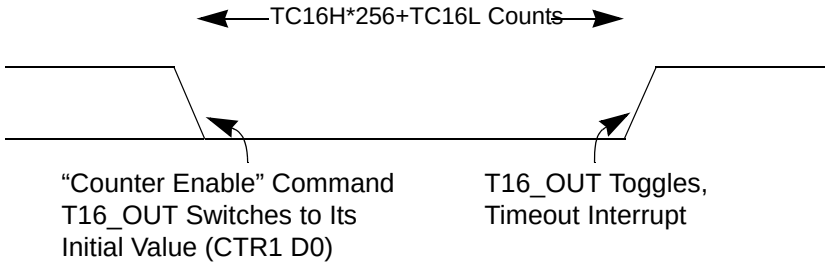


Figure 26. T16_OUT in Single-Pass Mode

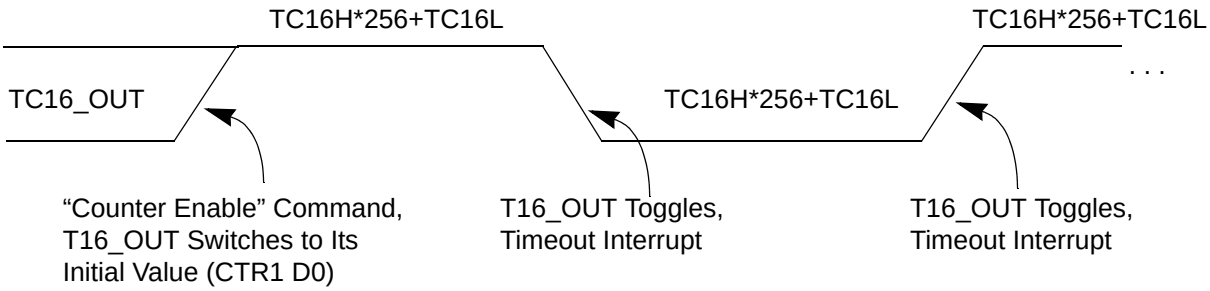


Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

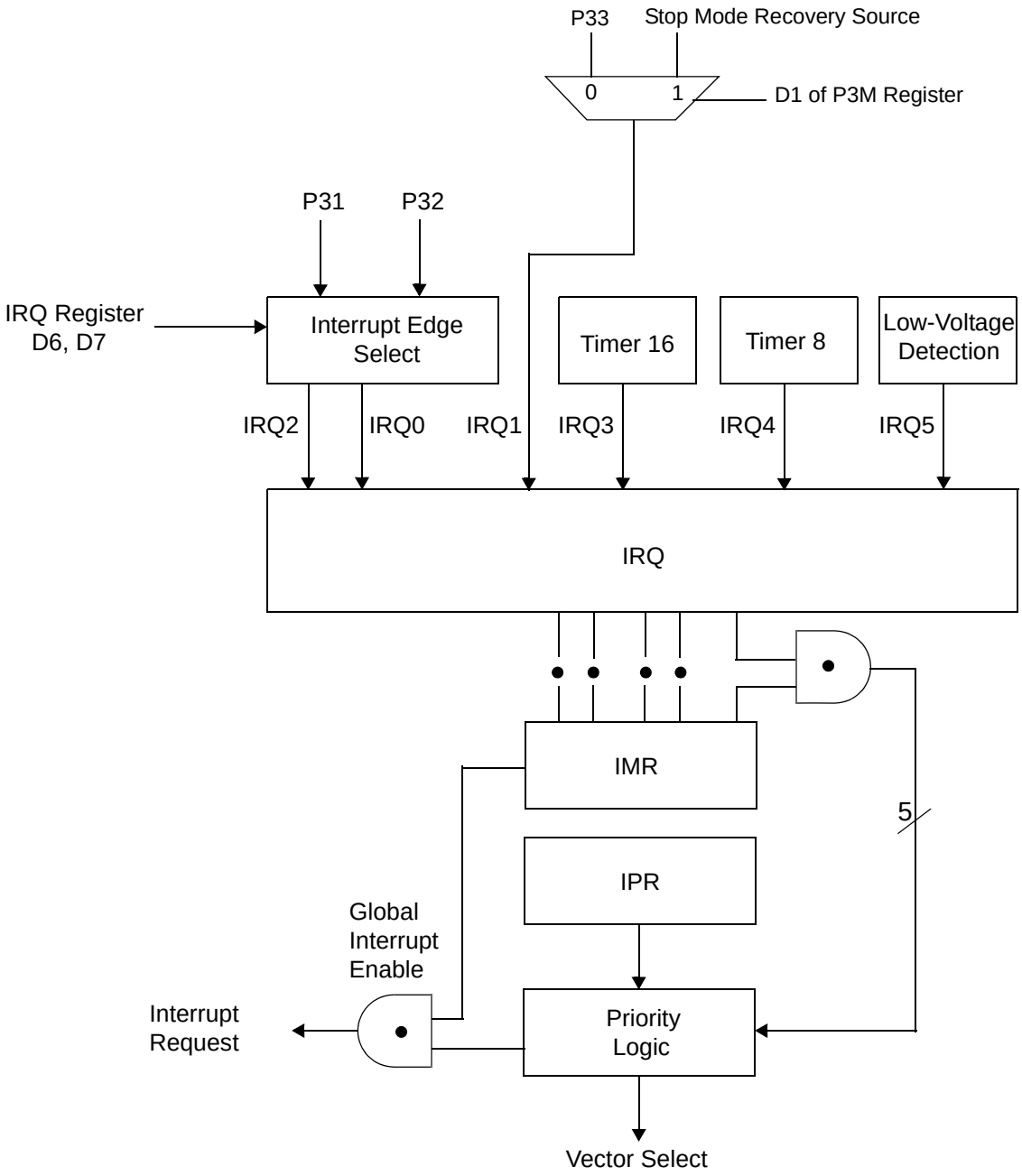


Figure 30. Interrupt Block Diagram

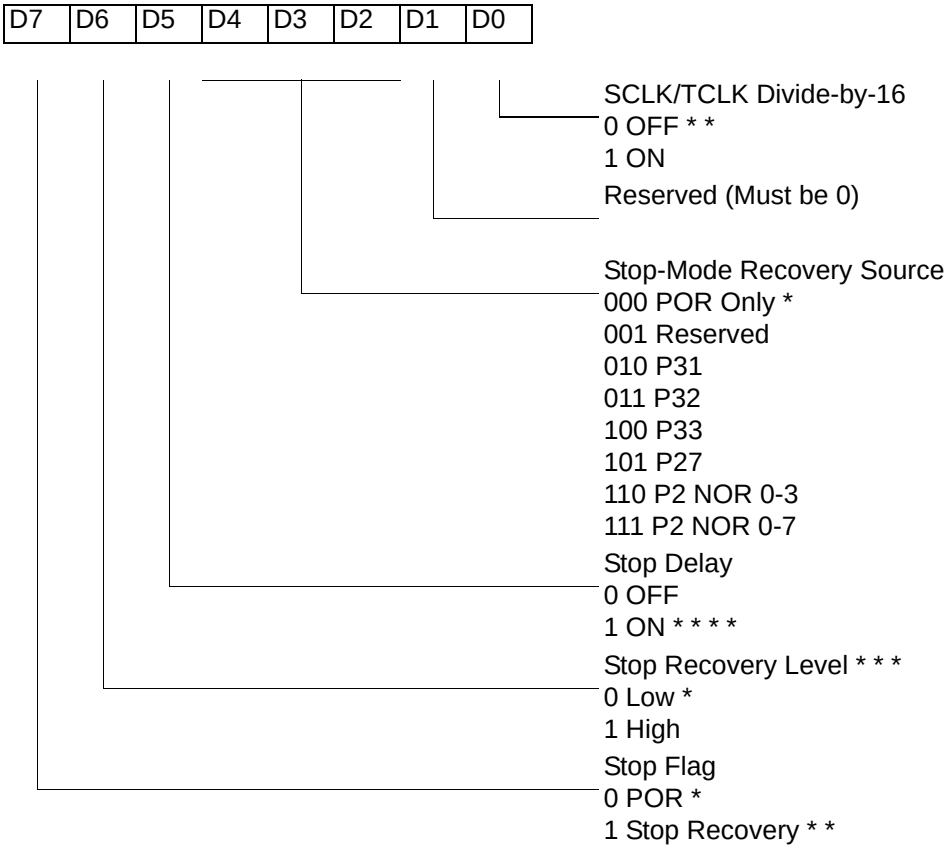
Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset
* * Default setting after Reset and Stop Mode Recovery
* * * At the XOR gate input
* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

Low-Voltage Detection Register—LVD(D)0Ch

Note: Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	-----2--	R	1 0*	HVD flag set HVD flag reset
	------1-	R	1 0*	LVD flag set LVD flag reset
	-------0	R/W	1 0*	Enable VD Disable VD

***Default after POR

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

Notes: If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

CTR2(0D)02H

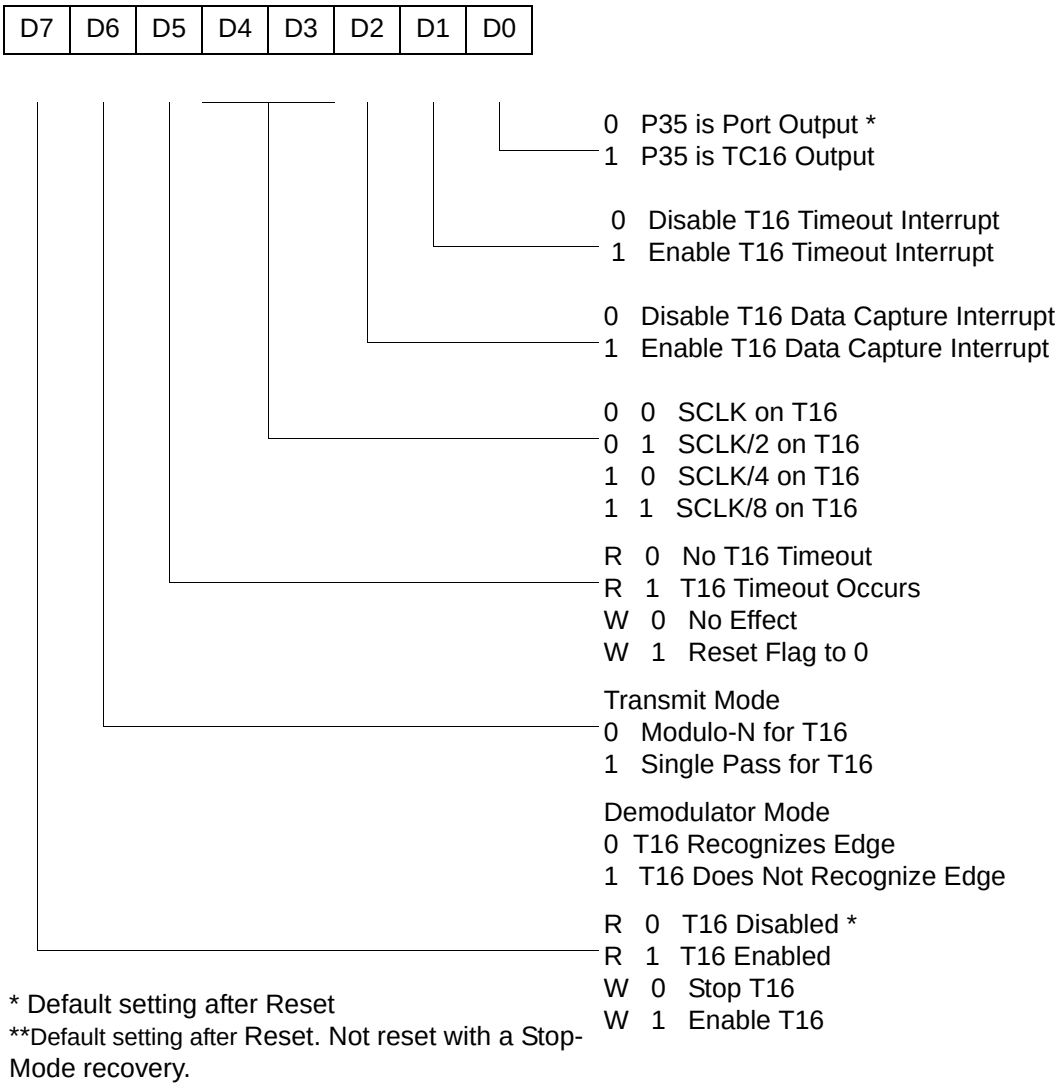
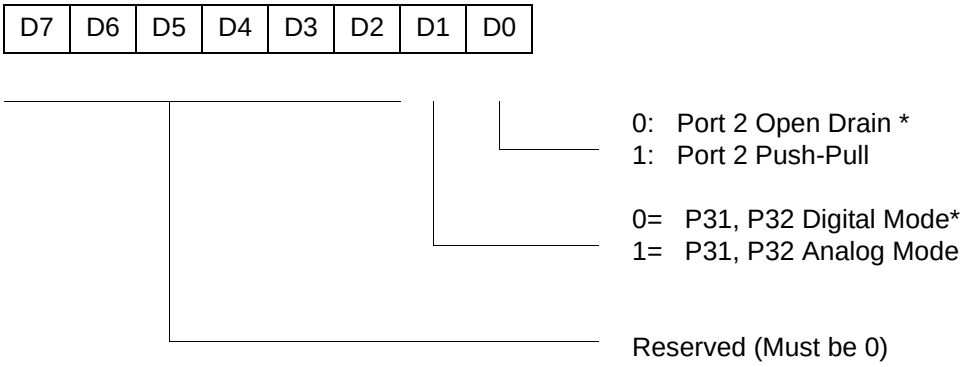


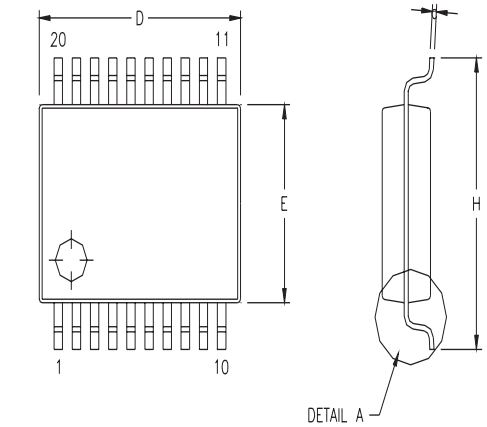
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

R247 P3M(F7H)

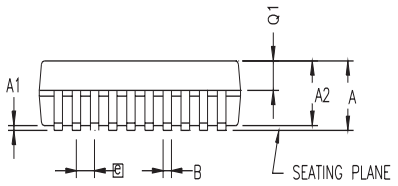


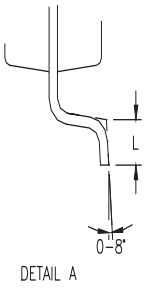
* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)



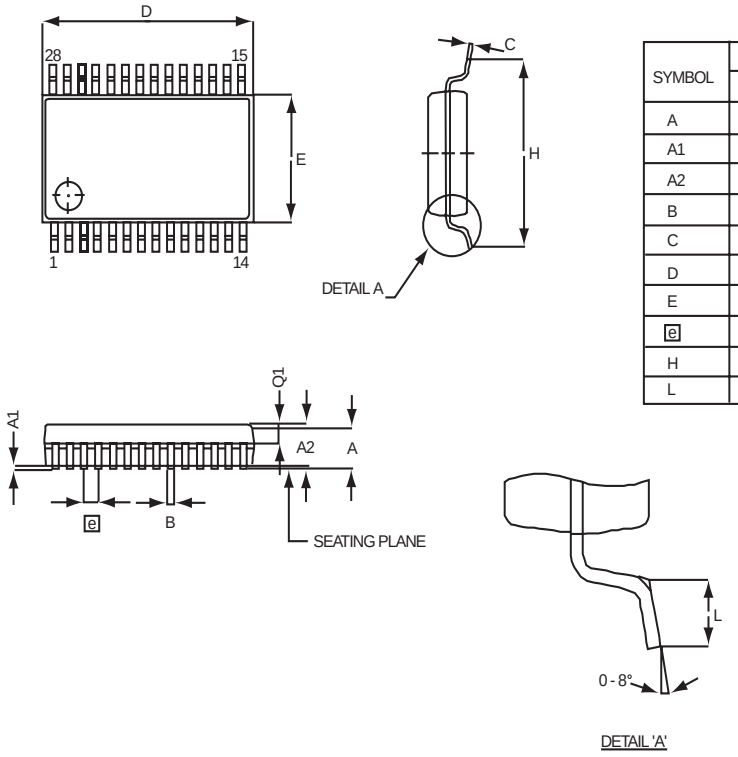
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032





CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

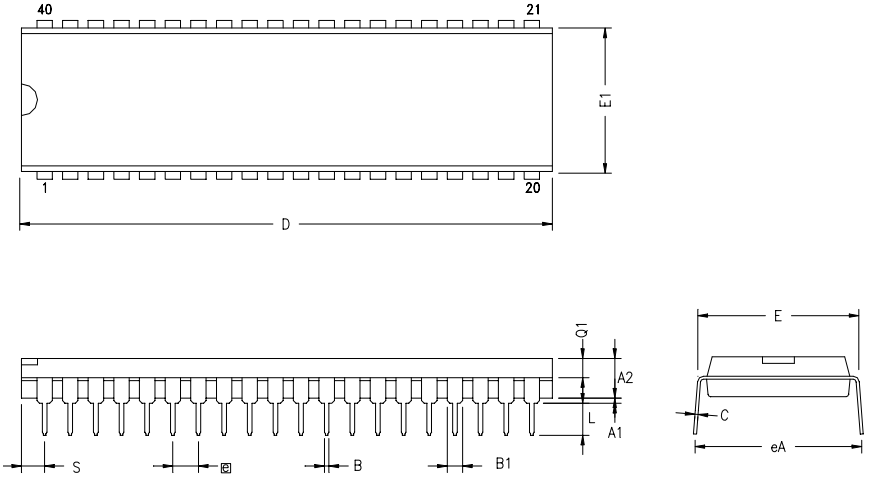
Figure 61. 20-Pin SSOP Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
B	0.25		0.38	0.010		0.015
C	0.09	–	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.402	0.407
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

CONTROLLING DIMENSIONS: MM
LEADS ARE COPLANAR WITHIN .004 INCHES.

Figure 65. 28-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 66. 40-Pin PDIP Package Diagram